

A Secure Dynamically Programmable Gate Array Based on Ferroelectric Memory

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The field programmable gate array (FPGA) market is expanding because FPGAs enable faster development times and lower development costs than mask programmable gate arrays (MPGAs).¹⁾ However, the conventional SRAM-based FPGA requires off-chip, non-volatile PROMs to store configuration data, which increases the total device cost and the board area. To provide a low-cost solution for field programmable devices, we have developed a non-volatile, 8-context, dynamically programmable gate array (DPGA^{note)}) using ferroelectric RAM (FeRAM) technology. The developed configuration memory, which consists of a SRAM-based 6-transistor/4-ferroelectric-capacitor cell, has an access time comparable to that of a standard SRAM. It also has a non-destructive read operation and a stable data recall scheme. In addition, the contents of the configuration memory are securely protected. We have fabricated a prototype DPGA that combines 0.35 μm CMOS and FeRAM technologies. Using this device, we have executed the Data Encryption Standard (DES) functions at up to 51 MHz at 3.3 V. We confirmed that the minimum non-volatile operating voltage is 1.5 V.

1. Introduction

Since conventional field programmable gate arrays (FPGAs) require additional PROM, the total cost and required board area increase. FPGA vendors and users have been requesting a non-volatile memory technology to realize single-chip, non-volatile FPGAs. Chips containing FPGAs and non-volatile data storage memory can be fabricated using floating-gate, non-volatile memories such as EEPROMs and flash memories. However, their write cycles are inferior to those of standard CMOS devices and, compared to the standard CMOS technology, the number of additional masks

required to fabricate an embedded non-volatile memory is typically larger than six.²⁾ On the other hand, FeRAM technology can be used to fabricate a non-volatile storage device that is completely compatible with standard CMOS specifications and design reusability. The number of additional masks needed to make ferroelectric capacitors on a standard CMOS can be reduced to two by improvements in fabrication technology.³⁾

Table 1 compares some of the characteristics of FeRAM with two conventional non-volatile memories: EEPROM and Flash. In addition to being compatible with the standard CMOS process, FeRAM outperforms the other two memories in terms of the program time, program voltage, and program energy. In FeRAMs, since the program voltage is the power supply voltage of the logic circuit, on-chip, high-voltage generator circuits can be eliminated.

note) A DPGA has multiple banks of configuration memory for various functions and can dynamically change its logic function. The number of available logic gates per unit area in a DPGA is superior to that in a conventional FPGA.

Table 1
Comparison of non-volatile memory characteristics.

Characteristics	EEPROM	Flash	FeRAM
Read access time	150 ns	50 ns	85 ns
Program time	2 ms	2 ms	85 ns
Program voltage	18 V	12 V	3.3 V
Program energy	2 mJ	8 mJ	0.1 nJ
Program endurance	10^6	10^6	10^{10}
CMOS process compatibility	Restricted	Restricted	Good

In addition to the increase in total cost and board area mentioned above, conventional FPGAs have a lower logic-density (the number of available logic gates per unit area) than MPGA. A dynamically programmable gate array can improve the number of available logic gates by implementing multiple banks of configuration memory and changing the number of banks of configuration memory (called the “context” in this paper) during logic operation.⁴⁾⁻⁶⁾ Since the area occupied by the configuration memory is typically 10% of the entire FPGA, the number of available logic gates can be doubled using two-sets of configuration memory while incurring an area overhead of only 10%.⁷⁾

The above considerations indicate that the cost of mass-produced FPGAs can be minimized by using a combination of FeRAM and a multi-context scheme. This paper explores how FeRAM circuits can be optimally implemented in a non-volatile DPGA.

2. Architecture

Figure 1 shows the hierarchical structure of a prototype FeRAM-based DPGA, and **Table 2** summarizes its primary architecture. The elemental logic block is organized with a 4-input look-up table (LUT), a flip-flop, and multiplexers for input selection. The subarray consists of 4×4 elemental logic blocks, a bounded-subarray-style local interconnection,⁷⁾ and a configuration memory controller. The middle array is formed by 2×2 subarrays connected with a NEWS network

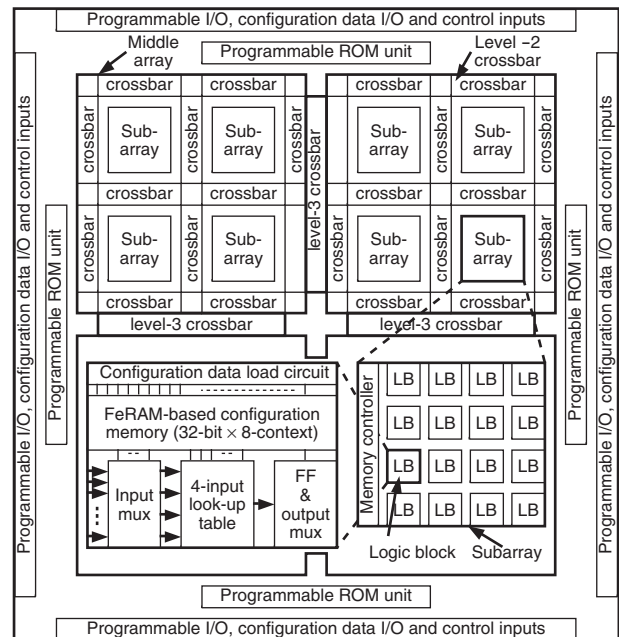


Figure 1
Hierarchical structure of prototype FeRAM-based DPGA.

of level-2 crossbars. The level-2 crossbar consists of eight 16-to-1 multiplexers, and crossbar selection control is encoded within the multiplexer to reduce the size of the configuration memory.⁸⁾ The entire chip is organized by symmetrical 2×2 middle arrays connected with level-3 crossbars. The level-3 crossbars contain sixteen 16-to-1 multiplexers and enable selection of the global interconnections along the length of the logic block array. These global interconnections are supplied to the level-2 interconnections in the form of a higher-level NEWS network, resulting in a tree structure (pyramid architecture).

Table 2
Summary of primary architecture.

Type of logic block	4-input look-up table with FF
Number of logic blocks	256
Number of contexts	8
Programmable logic hierarchy	1st: logic block (4-LUT)
	2nd: subarray (4×4 LB)
	3rd: middle array (2×2 subarray)
	4th: top (2×2 middle array)
Programmable interconnect hierarchy	Level-1: bounded subarray
	Level-2: multiplexer-type crossbar (NEWS network)
	Level-3: multiplexer-type crossbar (NEWS pyramid network)
Programmable ROM unit	Configuration memory based
Configuration data load	Multipath serial inputs (Background programming)
Number of I/O pins	72
Logic gates	29 K

Four 512-bit programmable ROMs having the same structure as the configuration memory are placed on each side of the symmetrical array.

The DPGA described in this paper has eight contexts, and the equivalent logic gate count is calculated to be 29 K. The system gate count becomes 68 K when 20% of the total LUTs are used as local memory.⁹⁾ The total capacity of the 8-context configuration memory is 92 K bits.

Figure 2 shows the structure of the configuration memory when its outputs are connected to an LUT. The 8-context configuration data is stored in an 8-row FeRAM array controlled by the corresponding wordline (WL) and the plateline (PL), which is a common control line for ferroelectric capacitors. The output buffers store the configuration data for the currently operating function and enable background configuration programming by isolating bitline signals from its outputs. The bit streams of the configuration data are supplied from the shift register and programmed through the write amplifier using the write enable signal (WE) and PL.

CMD[0:2] specifies one of the fundamental

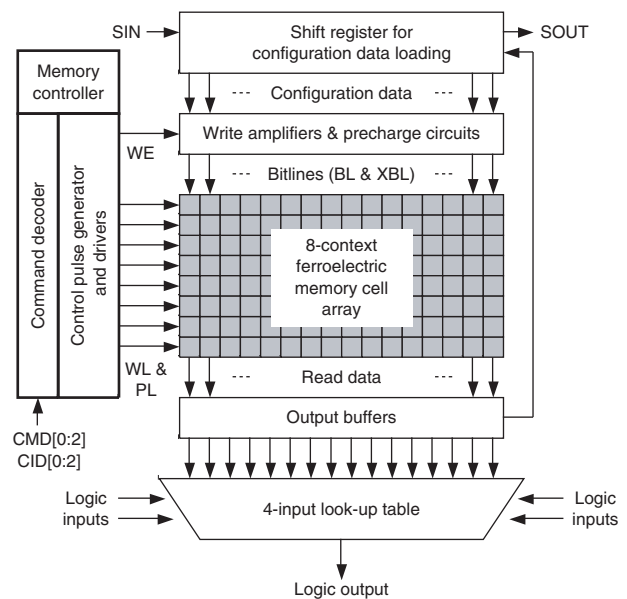


Figure 2
Structure and control of configuration memory.

configuration memory operations, configuration data transfer from SIN to SOUT, CID change for the logic function change, background configuration programming, configuration data recall, power-off, and several test modes. The recall command initiates a read-out sequence from non-volatile ferroelectric capacitors to the corresponding memory cells after power-on. The power-off command protects the contents of the configuration memory in the power supply ramp-down period. The recall and power-off commands are generated according to a signal from a voltage detector. The context can be changed in a single clock cycle, and the overall latency of the CID change from assertion of the internal signal is six clock cycles.

The contents of the non-volatile configuration memory must be securely protected from malicious read-out and overwriting. **Figure 3** shows bit streams associated with the configuration data program and read. The input bit stream consists of the synchronizing word, Program or Read command, security ID, configuration data (if any), and a CRC (Cyclic Redundancy Check) code to detect communication errors. The total 1K-bit security ID for each user is programmed

Operation	Input/output	Data stream				
Configuration data program	SINx input	Sync word	Command	Security ID	Configuration data (2944 bits)	CRC
Configuration data read	SINx input	Sync word	Command	Security ID	CRC	
	SOUTx output	Sync word	Configuration data (2944 bits)		CRC	

Figure 3
Bit streams for configuration data programming.

in a specific region of the configuration memory after device tests. If the security ID in the bit stream does not match the one stored in the configuration memory, the Program and Read operations will be prohibited. The information stored in the FeRAM-based configuration memory has enough tamper-resistance to prevent destructive and non-destructive analyses.

3. Ferroelectric configuration memory

Conventional FeRAM products utilize the 2-transistor/2-capacitor (2T2C) memory cell shown in **Figure 4** to keep the memory cell small and maintain a high reliability.¹⁰⁾ In this memory cell, two ferroelectric capacitors, FC1 and FC2, are held at the two opposing polarization points on the ferroelectric hysteresis loop shown in **Figure 5**. When FC1 is in the “0” state (because of the application of a positive voltage), FC2 is in the “1” state (because of the application of a negative voltage). In the read operation, the switching charge difference between the memory capacitors (C0, C1) generates a voltage difference, V_{sig} , between the bitlines. Then, this voltage difference is amplified to the full rail-to-rail voltage by a differential sense amplifier. The typical value of V_{sig} for a 2T2C cell is 600 mV,¹¹⁾ which is much larger than that of a DRAM.

The drawbacks of conventional FeRAM are that 1) their read cycle is longer than 80 ns due to the destructive read and subsequent restore peri-

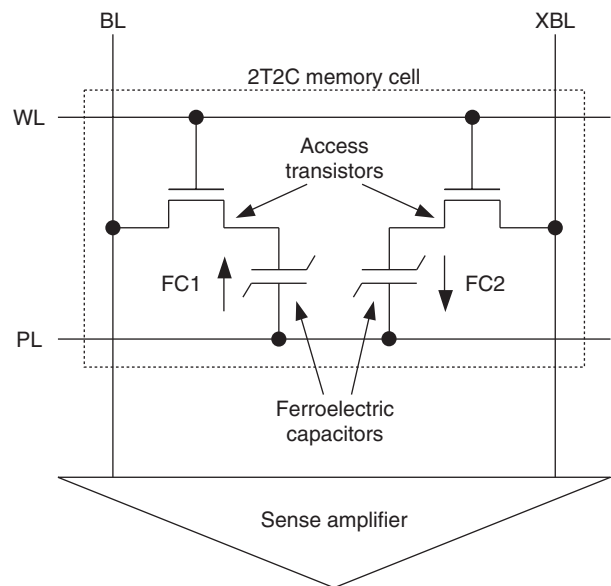


Figure 4
Conventional 2T2C FeRAM cell.

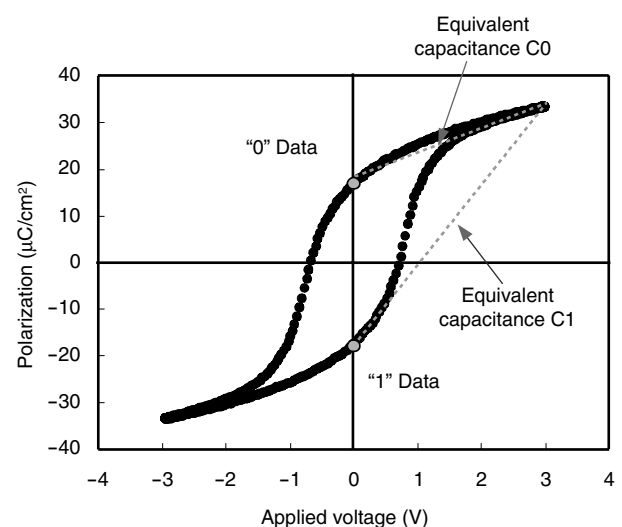


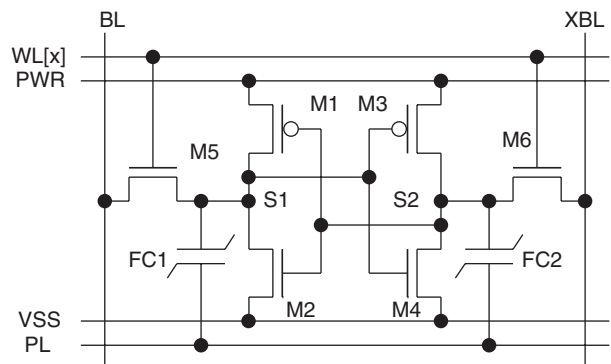
Figure 5
Ferroelectric hysteresis loop of 0.35 μm FeRAM cell.

od and 2) the destructive read and material-wear-out that occur in these devices limit the guaranteed maximum number of read and program cycles to 1×10^{10} . The memory cell shown in Figure 4 is suitable for applications in smart cards¹²⁾ and FPGAs since it has a small memory-cell geometry and the number of read access cycles to its non-volatile memory is rather small because it has limited system requirements. On the other hand, the DPGA requires a read access time of less than 10 ns to cope with higher clock frequencies and also requires non-destructive reading to accommodate frequent CID changes.

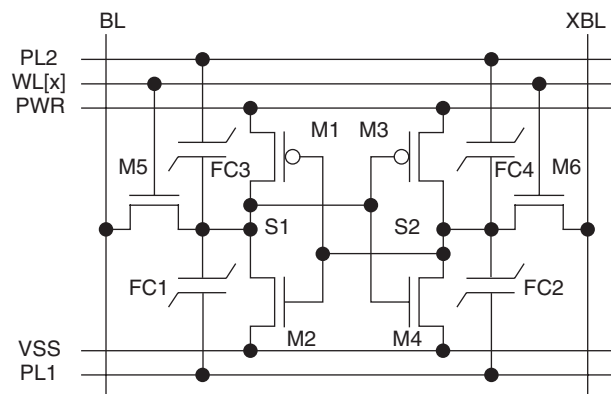
The previously reported non-volatile SRAM¹³⁾ shown in **Figure 6 (a)** can achieve a read access time comparable to that of a SRAM cell, and the read operation becomes non-destructive when the voltage across the ferroelectric capacitors, FC1 and FC2, remains constant during the read operation. The memory cell size can be made the same as that of conventional SRAM by stacking ferroelectric capacitors above the cell's transistors.¹³⁾ However, in this cell structure, the recall operation turns out to be unstable; this is discussed later in this section. We have therefore recently developed the 6-transistor/4-capacitor (6T4C) cell shown in **Figure 6 (b)** to improve the data recall characteristics. The four capacitors are controlled by two platelines: PL1 and PL2.

Table 3 summarizes the operations and associated control signals for the previous and the newly developed ferroelectric SRAM cells. The command decoder in the memory controller shown in Figure 2 generates the sequential sets of oper-

ations shown in Table 3 from CMD[0:2]. For example, when the command/CID generator issues the CID change command, the command decoder generates the Read operation and the subsequent Normal (standby) operation. CID[0:2] specifies the selected pair of wordline and plateline. The



(a) Conventional cell



(b) Stable data recall cell

Figure 6
Ferroelectric SRAM-based configuration memory cells.

Table 3
Operations and associated control signals for ferroelectric SRAM cells.

Operation	PWR	BL	WL[x]	PL for Figure 6 (a)	PL1 & PL2 for Figure 6 (b)
Normal	On	Pre-charged	Low	Vdd/2	Vdd/2
Program	On	Program data	High	High → Low	High → Low
Read	On	Read data	High	Vdd/2	Vdd/2
Recall	Off → On	Pre-charged	Low	Low	PL2: Low PL1: Low → High
Power-off	On → Off	Pre-charged	Low	Vdd/2 → Low	Vdd/2 → Low

Program and Read operations are the same as in a conventional SRAM except for the plateline control. Platelines PL, PL1, and PL2 are set at half V_{dd} in Normal and Read operations to mitigate the effect of imprint in the ferroelectric material.¹³⁾ This imprint occurs due to DC-voltage and temperature stresses and causes a horizontal shift of the ferroelectric hysteresis loop that makes it harder to switch the state of the device.¹¹⁾

The most important operation in Table 3 is Recall, since the entire 92 K bits of configuration data in this prototype DPGA must be properly regenerated from the ferroelectric capacitors to the corresponding cross-coupled SRAM cell in a single sequence. In the conventional data recall operation employed for the 6T2C cell, PWR is applied to the cell array while PL is set to low. On the other hand, in the 6T4C cell, PL1 is initially driven from low to high while PL2 is kept low and then PWR is applied to the cell.

Figure 7 shows the results of a SPICE simulation of data recall performance at points S1 and S2 in the conventional cell (S1(a) and S2(a)) and in our new cell (S1(b) and S2(b)) under the worst-case 3σ process variation of transistor characteristics. M1 and M4 in Figure 6 have a fast corner model, while M2 and M3 have a slow corner model. The conventional cell fails to recall; however, our new cell operates correctly over a

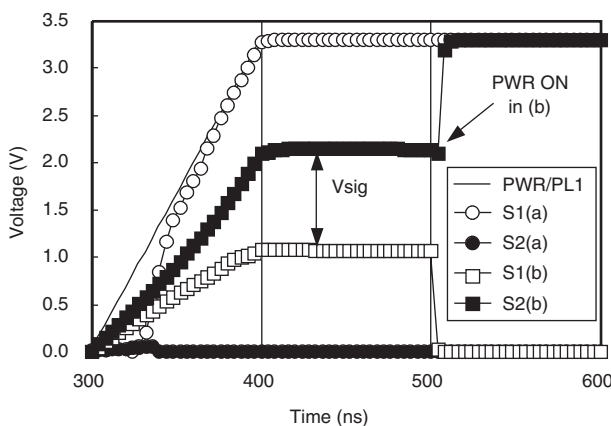


Figure 7
Simulation results of data recall operations.

wide range of transistor imbalance. In the conventional cell, the SRAM cell begins to latch when the voltages across FC1 and FC2 are near the 0.5 V threshold voltage of M2 and M4. Therefore, the difference in the equivalent capacitances of FC1 and FC2 between 0 to 0.5 V is fairly small. In the new cell, the voltage applied to the ferroelectric capacitors is about one or two thirds of V_{dd} , which means that there is a large difference in capacitance between the “1” and “0” states.

Table 4 summarizes the characteristics of a conventional FeRAM cell and the 6T4C cell shown in Figure 6 (b).

4. Logic block circuit and benchmark

Figure 8 shows a schematic diagram of the elemental logic block circuit. The 2-to-1 multi-

Table 4

Comparison of conventional FeRAM and employed memory cell characteristics.

	Conventional FeRAM	Employed memory cell
Cell structure	DRAM-based	SRAM-based
Memory cell	1T1C/2T2C	6T4C
Read scheme	Destructive	Non-destructive
Read access endurance	1×10^{10}	Unlimited
Read access time	85 ns	4 ns
Program endurance	1×10^{10}	1×10^{10}
Program time	85 ns	50 ns
Recall operation	Not necessary	Necessary

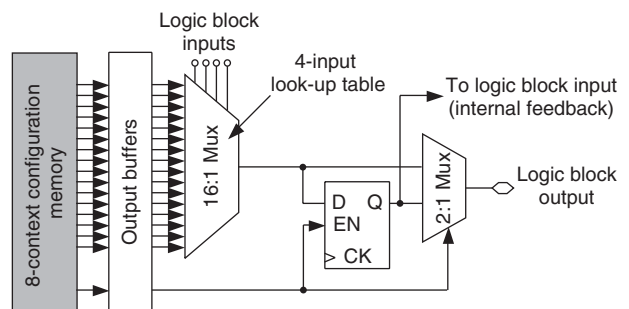


Figure 8
Elemental logic block circuit.

plexer selects outputs from the LUT or the flip-flop. The latched signal is supplied to the output by enabling the flip-flop in one context. On the other hand, when the unlatched signal is selected in another context, the flip-flop is disabled and can store an intermediate result of the previous operation. Consequently, combination logic operation by the LUT and the previous data storage by the flip-flop are executed simultaneously in one logic block for the multi-context scheme.

To evaluate this circuit, we implemented the Data Encryption Standard (DES) encryption/decryption function¹⁴⁾ using six contexts of the prototype DPGA. The proper implementation was validated by standard, known-answer tests.¹⁵⁾ **Figure 9** shows the mapping result of the third context. Key and intermediate results of expansion permutation were stored in the flip-flops around the center region. Moreover, a combinational logic function operating as the substitution-box was implemented on the LUTs in the same region. The logic block circuit shown in Figure 8 can improve

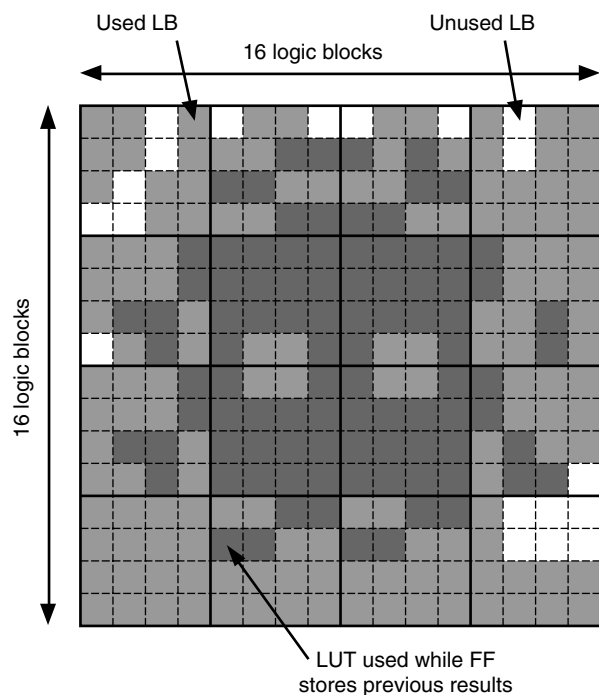


Figure 9
Example of DES mapping.

the logic density for the multi-context scheme with the minimum area overhead.

5. Chip design

A prototype non-volatile and secure DPGA has been designed that uses a 0.35 μm triple-layer metal CMOS technology and a 3.3 V embedded FeRAM technology.¹⁶⁾ **Figure 10** shows a die micrograph of the prototype DPGA. The die size is 10.4 mm $\times$ 10.4 mm. This device contains 184 blocks of 64-bit/8-context configuration memory arranged in an array, and a 64-bit configuration memory is used to configure two logic blocks.

Table 5 summarizes the results of a simulation of nominal performance for the primary DPGA circuit elements. According to these results,

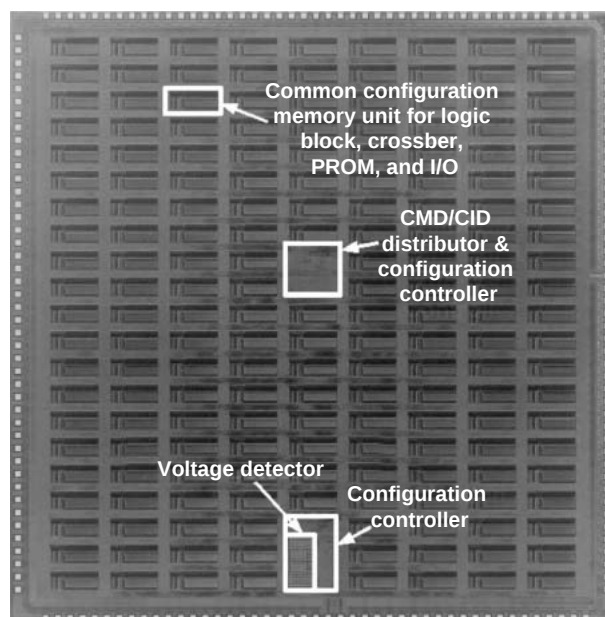


Figure 10
Die micrograph of prototype FeRAM-based DPGA.

Table 5
Nominal simulation results for primary circuit operations.

Path	Delay (ns)
CLK $\rightarrow$ Configuration memory output stable	2.0
Crossbar in $\rightarrow$ Crossbar out	0.7
LUT in $\rightarrow$ LUT out	0.4
Logic block in $\rightarrow$ Logic block out	1.3

the maximum operating frequency of a series connection of three LUTs and three crossbars is 125 MHz. The maximum frequency of configuration memory programming is 40 MHz and is mainly determined by the RC delay of the plateline.

6. Experimental results

The delays of the logic block and crossbar were evaluated by connecting them in series to configure inverter chains of various lengths. The measurements at 3.3 V and room temperature show delays of 2.3 ns and 2.4 ns for the logic block and crossbar, respectively. The differences between these measurements and the simulation results shown in Table 5 arise from the interconnection delay. The measured delays are comparable to those in an FPGA product fabricated with a 0.35 μm technology.¹⁷⁾ Based on these measurements, the maximum operating frequency of a series connection of three LUTs and three crossbars is 62.1 MHz.

Figure 11 shows a shmoo plot of the DES operation at room temperature. The measured maximum operating frequency is 51 MHz at 3.3 V. This value matches well with a delay simulation including a back-annotated interconnection delay, which indicates 50 MHz operation under the same conditions. In addition, a simple path delay calculation of the DES implementation gives an operating frequency of 54.1 MHz, since the critical path consists of a series connection of three LUTs and four crossbars. The measured power consumption of the DES operation is 282 mW at 20 MHz and room temperature.

We calculated that when the configuration memory is subjected to typical operating stresses, its minimum non-volatile operating voltage will be 1.5 V. This is the lowest operating voltage ever reported in a PZT-based ferroelectric memory.

7. Conclusion

This paper described the application of a non-volatile, ferroelectric memory technology in low-cost field programmable devices and the tech-

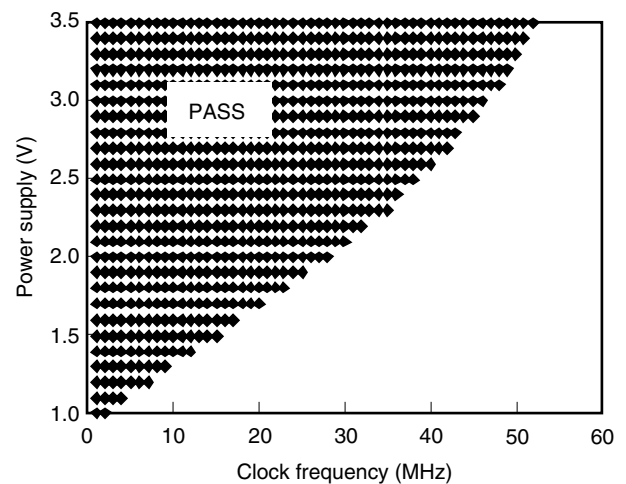


Figure 11
Shmoo plot of DES implementation at room temperature.

nology's multi-context scheme. We have developed a prototype, non-volatile 8-context DPGA with a secure protection function for configuration data that is fabricated using 0.35 μm CMOS and FeRAM technologies. The new DPGA uses a SRAM-based 6T4C memory cell that performs fast, non-destructive reading and stable recall. The read speed of this cell is much faster than that of conventional 1T1C/2T2C cells and is comparable to that of a standard SRAM cell. The 1.5 V non-volatile memory characteristics of this cell are superior to those of other conventional PZT-based 1T1C/2T2C cells because of the large recall margin. We used this cell to implement a DES encryption/decryption function and obtained results comparable to those obtained with standard CMOS technology. Non-volatile DPGA can be used to increase the logic gate counts in scaled technologies, and it will be used more and more in the already large and still growing field of communications.

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