Integration of High-Performance Transistors, High-Density SRAMs, and 10-level Copper Interconnects into a 90 nm CMOS Technology

● Satoshi Nakai ● Tsutomu Hosoda ● Yoshihiro Takao

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This paper presents a 40 nm-gate-length transistor, an ultra-high-density 6T SRAM cell, 10-level Cu interconnects, and very-low-k (VLK) dielectrics for high-performance microprocessor applications. The key process features are 1) 193 nm lithography with a phase shift mask (PSM) and optical proximity correction (OPC) that enables us to fabricate a 40 nm-long gate and a sub-1 μm² SRAM cell, 2) a unique transistor feature called a sidewall-notched gate that enables optimal pocket implant placement and suppresses variations of the notch width much better than a poly-notched gate structure, 3) a 1.1 nm-thick nitrided oxide to achieve a high drive current and a reduced thermal budget to suppress boron penetration, and 4) an SiC-capped Cu/SiLK™ structure in 0.28 μm-pitch Metal 1-4 layers that realizes a k_{eff} of 3.0.[1)]

1. Introduction

As CMOS technology is scaled down to the 90 nm generation, the full integration of high-performance devices, multilevel Cu interconnects with low-k dielectrics, and high-density SRAMs will become a major challenge. Transistors having 65 to 45 nm gate lengths for 90 nm technologies for high-performance applications have been reported,[2)-9)] and we have achieved 40 nm-gate-length transistors for a 90 nm technology. Moreover, we have fabricated 10 levels of Cu interconnects, which is the largest number of Cu layers among reported technologies, and for intermediate layers we have applied an SiC-capped Cu/SiLK™ structure which realizes a k_{eff} of 3.0.

2. FEOL integration

By using a notched gate, we can achieve an optimal pocket implant placement, and in particular, suppress the channel impurity concentration.[10),11)] However, variations in the notch width of the poly-notched gate (conventional notched gate) are difficult to control so that they match the manufacturability criteria. We have therefore developed a new notched gate structure called the sidewall-notched gate. The sidewall-notched gate is formed as shown in **Figure 1**. After gate formation, a thin CVD-oxide and CVD-nitride are deposited (Step A). Then, the nitride is dry etched (Step B) and the oxide is wet etched (Step C). **Figure 2** shows a cross-sectional TEM photograph of the sidewall-notched gate. This method provides good controllability of the notch width because it is defined by the thicknesses of the CVD films. **Figures 3 (a)** and **(b)** show the threshold voltage as a function of gate length for sidewall-notched transistors and poly-notched transistors, respectively. These figures clearly demonstrate that the sidewall-notched gate structure suppresses variations in the threshold voltage better than the poly-notched structure. **Figure 4** shows the threshold voltage as a function of gate length for sidewall-notched transistors and con-

ventional (notchless) transistors. Because of the advantages that can be gained by using a notched gate, we propose a 40 nm transistor with a sidewall-notched structure.

We use a 1.1 nm-thick, nitrided oxide for the gate insulator to achieve a high drive current. This particular nitrided oxide was selected from among other experimental ones we developed because it had the best nitrogen profile. **Figure 5** shows the nitrogen profiles of this nitrided oxide (Type B) and a typical example (Type A) of the other experimental nitrided oxides. Type B is much better than Type A in terms of nMOS drivability, as is clearly shown in **Figure 6**. Also, although Type B increases the boron penetration in pMOS, we suppressed the penetration by using

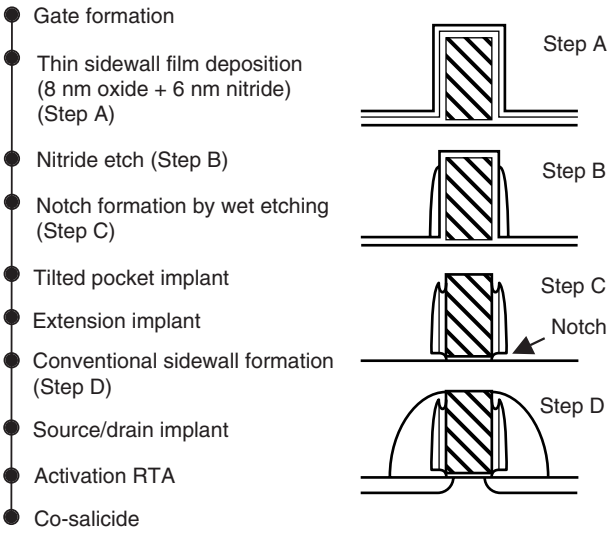

Figure 1
Sidewall-notched transistor fabrication.

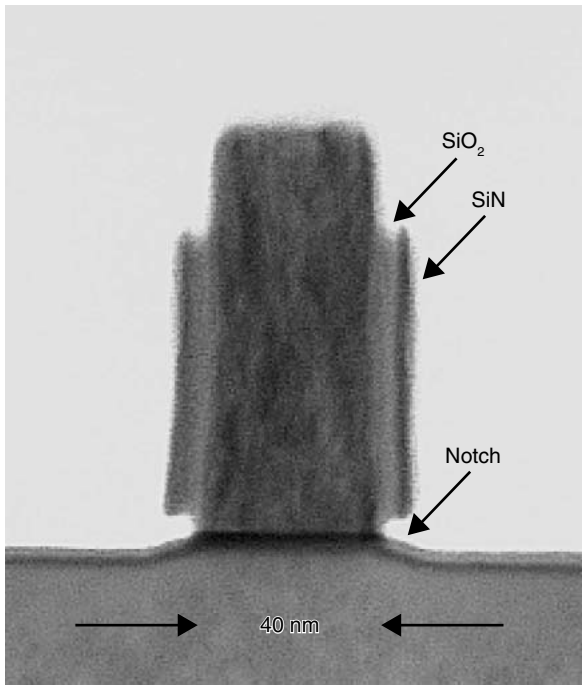

Figure 2
Cross-sectional TEM photograph of sidewall-notched transistor.

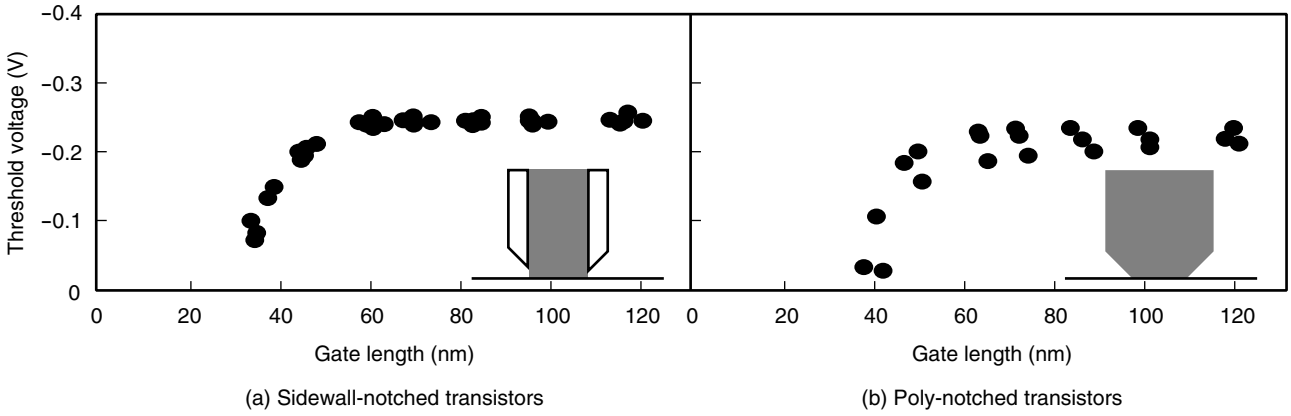

Figure 3
Threshold voltage as a function of gate length (pMOS). Sidewall-notched gate structure suppresses variations of threshold voltage.

a lower temperature activation anneal. **Figure 7** shows the threshold voltage distributions under the annealing conditions of this technology and those of the 130 nm-node technology.[12] **Figure 8** shows Ioff-Ion plots for a supply voltage of 1.0 V. At an off-current of 100 nA/μm, the on-current is 890 μA/μm for nMOS and 380 μA/μm for pMOS. At an off-current of 300 nA/μm, the on-current is 960 μA/μm for nMOS and 435 μA/μm for pMOS.

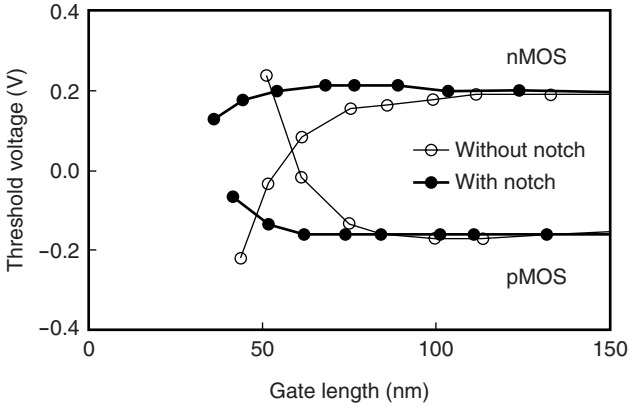

Figure 4
Improved roll-off characteristics of transistors with sidewall-notched gate electrode.

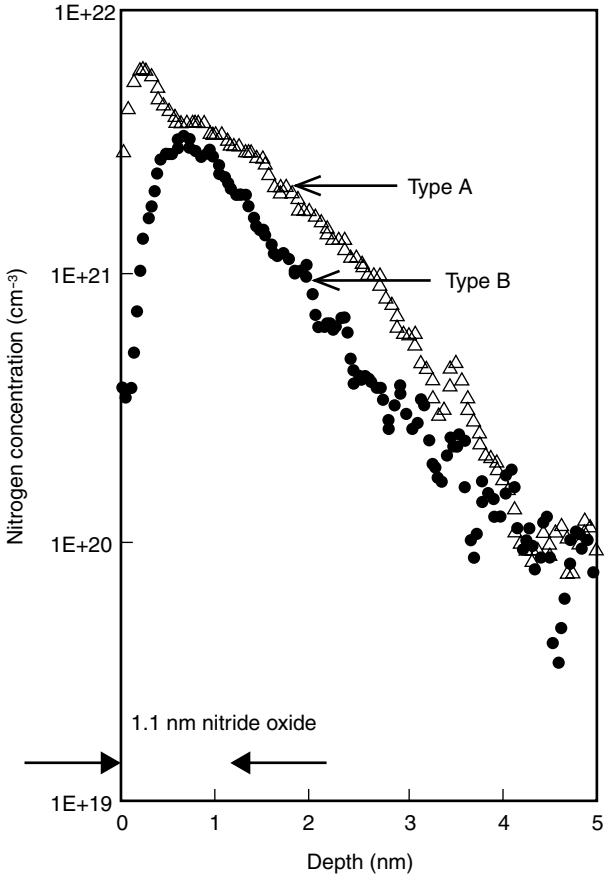

Figure 5
Nitrogen profile in nitrided oxide and substrate.

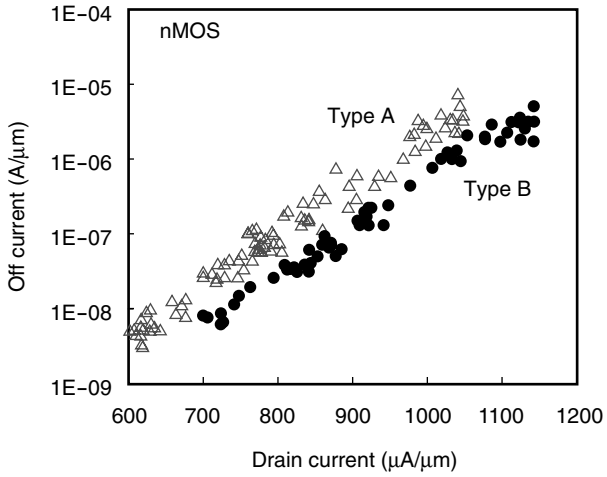

Figure 6
Ioff-Ion plots for nMOS when supply voltage is 1.0 V. See Figure 5 for Type A and B.

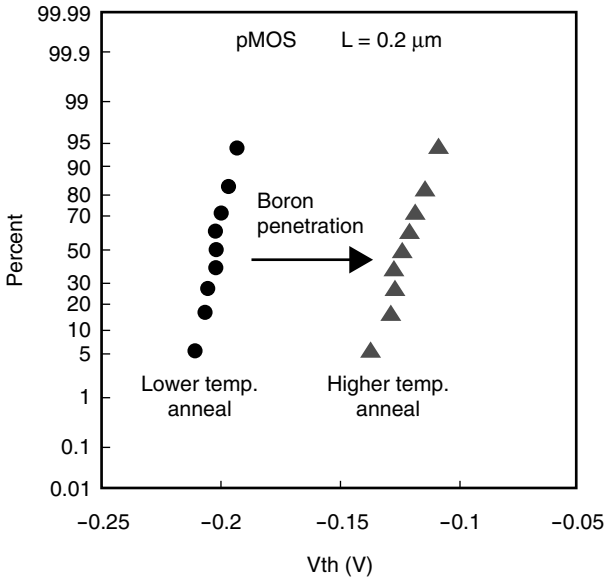

Figure 7
Threshold voltage distributions. At the higher temperature anneal, threshold voltage varies for the boron penetration.

A 40 nm gate length is achieved with 193 nm lithography. In addition, by using OPC and local interconnects (LIs), we have fabricated a sub-1 μm² SRAM cell (0.999 μm²). **Figures 9 (a)** and **(b)** show SEM photographs of an array of these SRAM cells.

3. BEOL integration

The interconnect scheme consists of four layers of Cu/SiLK™ (k = 2.65), four layers of Cu/SiOC, two layers of Cu/USG, and an Al top layer with a W plug (**Figure 10**). The design rules and inter-level dielectrics of this scheme are summarized in **Table 1**. We optimized the dielectric stacks of each layer to achieve excellent electrical properties, mechanical strength, and reliability.

For Metal 1-4 (intermediate layers), a dielectric stack consisting of SiLK™ with an SiC barrier and an SiO_2/SiC dual hard mask are used in a dual damascene scheme.[13] The line pattern is etched in the SiO_2 hard mask using ArF resist. The hole pattern is made by an ArF tri-level resist process to pre-planarize the trench hard-mask steps. Rule-based OPC and simulation-based OPC are adopted for the line and via lithography, respectively (**Figure 11**). SiLK™ trenches are etched using patterned SiO_2 hard masks. Cu electroplating and low-pressure Cu CMP is tuned to prevent dishing and erosion, as shown in **Figure 12**. Dishing and erosion are both controlled within 30 nm. The 4 M via chain resistance

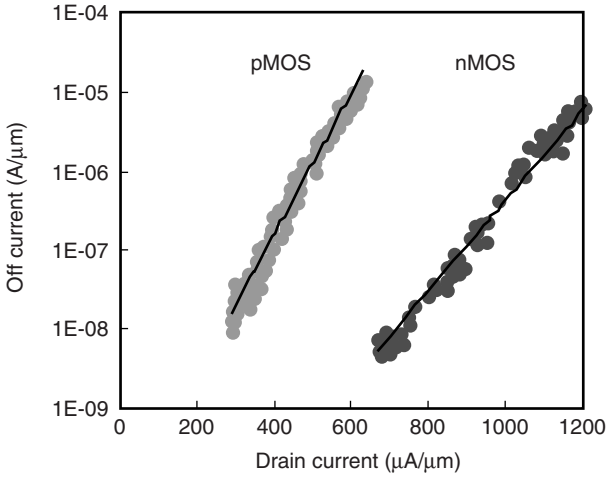

Figure 8
Ioff-Ion plots when supply voltage is 1.0 V.

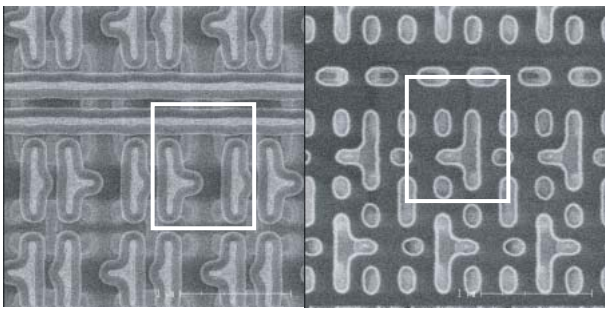

Figure 9
SEM photographs of high-density SRAM cell array.
Cell size is 0.9 × 1.11 μm² (< 1 μm²).

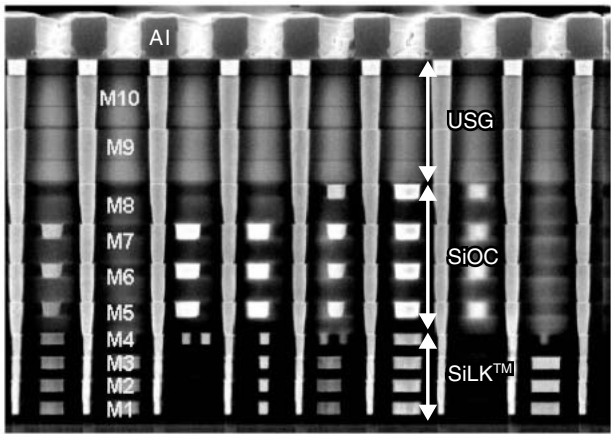

Figure 10
SEM image of 11 layers of interconnects.

Table 1
Key design rules.

Layer	Line (nm)	Space (nm)	Metal/ILD
Active	140	140	-----
Poly	40	220	-----
L.I.	120	160	-----
Metal 1-4	140	140	Cu/SiLK™
Metal 5-8	280	280	Cu/SiOC
Metal 9-10	420	420	Cu/USG

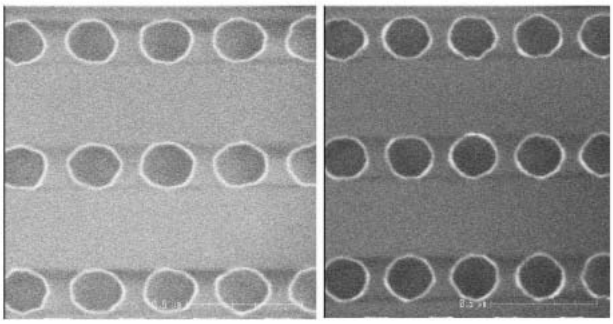

Figure 11
Effects of OPC in via patterning. Via shape is corrected from oval to circular by simulation-based OPC.

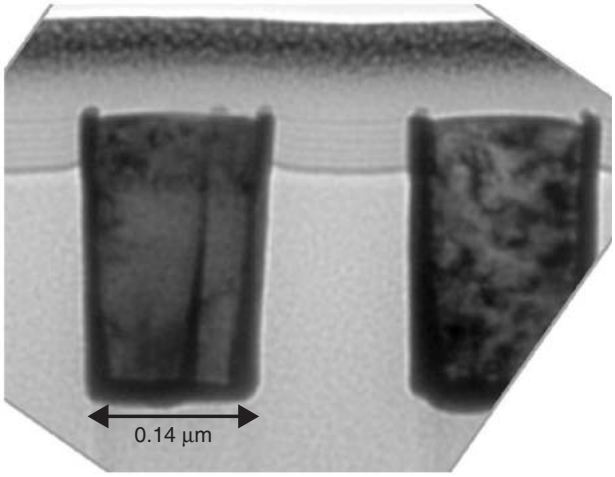

Figure 12
Cu electroplating structure without dishing and erosion.

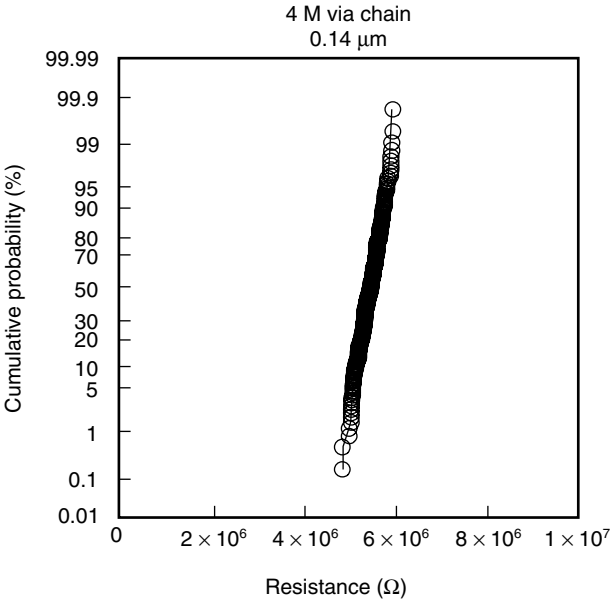

Figure 13
Via chain resistance of intermediate layer.

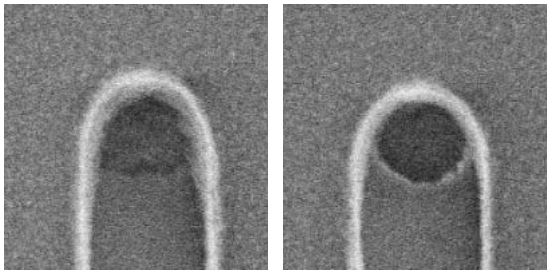

Figure 14
Line pattern resist at top of via.

distribution is ±9%, and the yield is 100%, as shown in **Figure 13**. This structure provides a k_{eff} of 3.0.

For Metal 5-8 (semi-global layers), a dielectric stack consisting of SiOC is used in a dual damascene scheme. Pre-planarization of the dielectric by CMP can be eliminated because of the low roughness at the lower layer. Vias and lines are produced by KrF lithography. The critical issue in integration is resist poisoning caused by N-H species. To prevent such poisoning, a newly developed wet cleaning scheme is applied (**Figure 14**). Metallization and Cu CMP are the same as for intermediate layers. The 1.35 M via chain resistance distribution is ±13%, and the yield is 100% (**Figure 15**).

For Metal 9-10 (global layers), a dielectric stack consisting of ARL-SiN and USG with an SiC barrier and ESL are used in a dual damascene scheme. The 270 K via chain resistance distribution is ±8%, and the yield is 100% (**Figure 16**). We use the Al top metal layer for bonding pads, bump pads, fuses, and wiring as an interface layer for realizing SIPs (Systems In a Package). One of the main issues in low-k, integrated multilevel metallization is the mechanical strength during assembly processes such as dic-

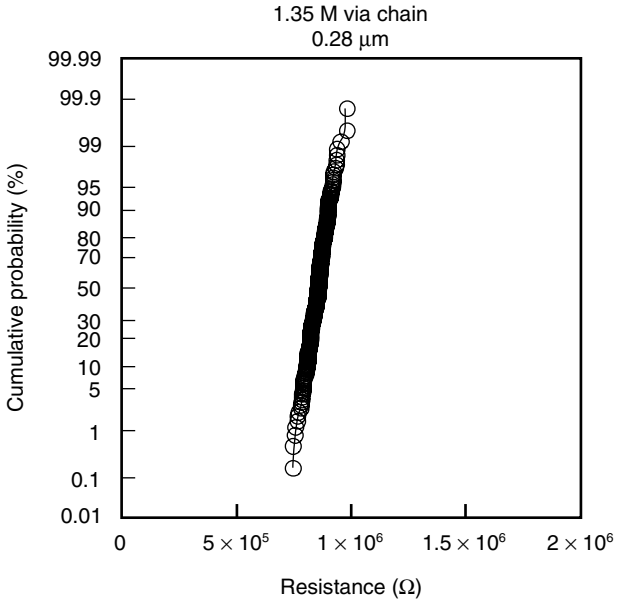

Figure 15
Via chain resistance of semi-global layer.

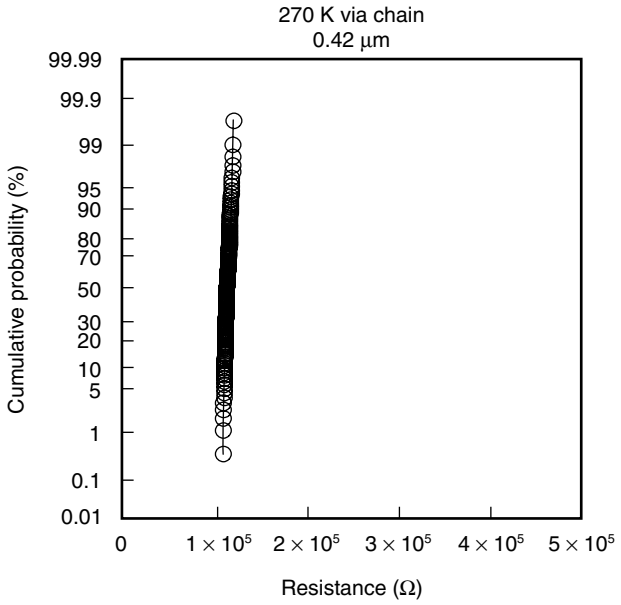

Figure 16
Via chain resistance of global layer.

ing, wire bonding, and bump connection of flip-chip packages. Generally, low-k materials have a poor mechanical strength compared to USG and FSG. **Figure 17** shows the results of wire bonding shear tests for samples with and without global layers. The figure shows that the USG global layer and Al wiring layer reduce the damage to the low-k layers.

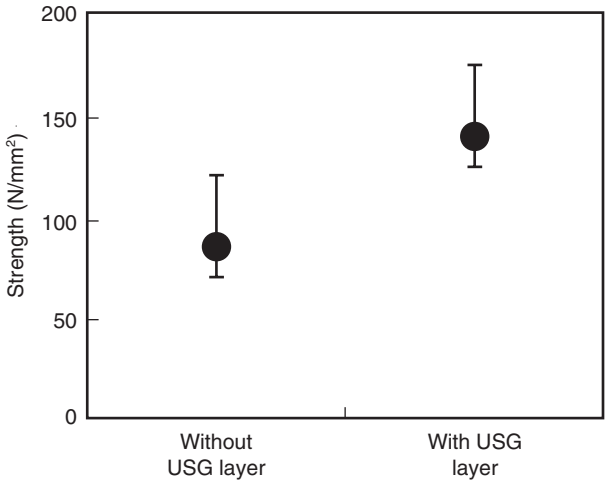

Figure 17
Results of wire bonding shear test.

To investigate the reliability of 12-layer interconnects (LI, 10-level Cu, and top Al), we performed a high-temperature storage (HTS) test and EM test on a via chain structure. In the HTS, as shown in **Figure 18**, there were no failures in any of the narrow-line or wide-line linked via layers after storage for 1000 hours at 200°C. **Figure 19** shows some EM results for the intermediate layer via chain. From measurements, we obtained an activation energy of 0.81 eV and a current coefficient of 1.33. The calculated maximum current density is over 5E5 A/cm^2 at 110°C.

4. Conclusion

We have developed a high-performance, 90 nm CMOS technology. By using 193 nm lithography with a PSM and OPC, we have fabricated a 40 nm-long gate and a 0.999 μm^2 SRAM cell. A transistor with a sidewall-notched gate suppresses variations in threshold voltage much better than a poly-notched one. At an off-current of 100 nA/μm, the on-current is 890 μA/μm for nMOS and 380 μA/μm for pMOS. At an off-current of 300 nA/μm, the on-current is 960 μA/μm for nMOS and 435 μA/μm for pMOS. We realized a Cu/SiLK™ structure using 193 nm lithography.

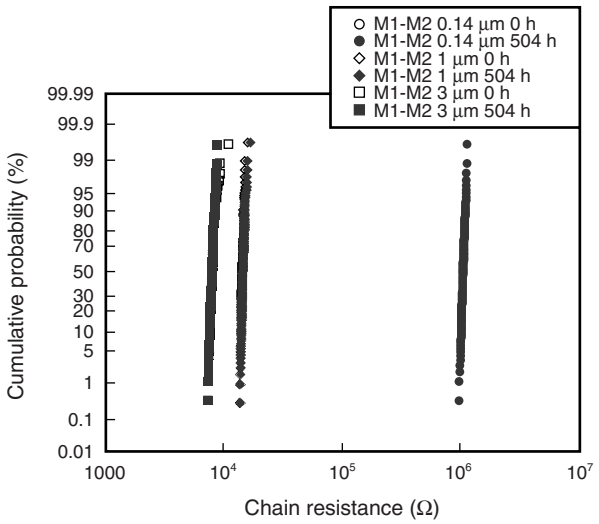

Figure 18
(a) HTS test results of M1-M2 via chain.

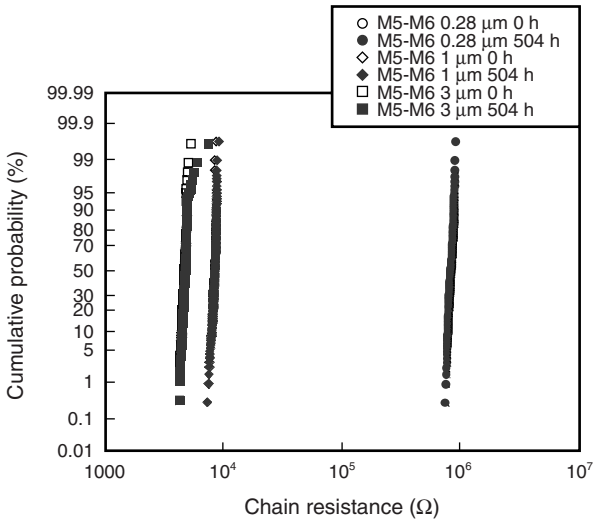

Figure 18
(b) HTS test results of M5-M6 via chain.

By using SiC as a cap film, we obtained a k_{eff} of 3.0. We also realized highly reliable, 10-level Cu interconnects.

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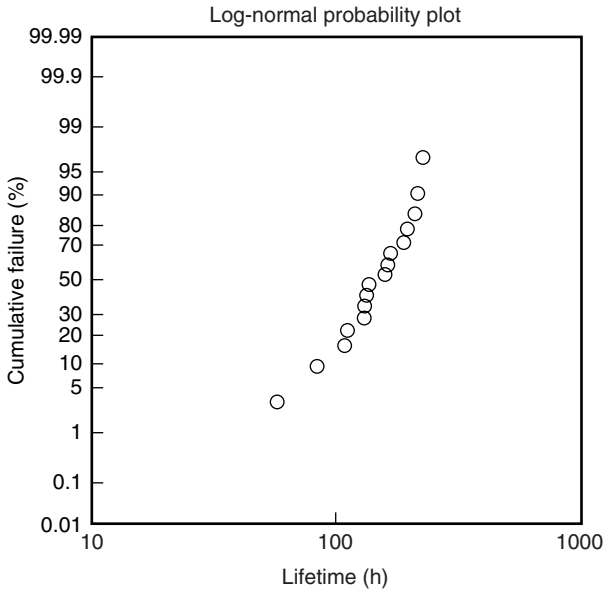

Figure 19
EM results of M1-M2 via chain.
(Tj = 275°C, J = 2.1E6 A/cm²)

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Satoshi Nakai received the B.S. degree in Physics from Waseda University, Tokyo, Japan in 1984 and the M.S. and Ph.D. degrees in Nuclear Science from Tohoku University, Sendai, Japan in 1986 and 1989, respectively. He joined Fujitsu Limited, Kawasaki, Japan in 1989, where he has been engaged in device modeling, reliability, and process integration. He is a member of the Japan Society of Applied Physics.

Tsutomu Hosoda received the B.S. degree in Physics from Okayama University, Okayama, Japan in 1987. He joined Fujitsu Limited, Kawasaki, Japan in 1987, where he has been engaged in back-end of line technology development.

Yoshihiro Takao received the B.S. and M.S. degrees in Electronics from Osaka Prefecture University, Osaka, Japan in 1984 and 1986, respectively. He joined Fujitsu Limited, Kawasaki, Japan in 1986, where he has been studying SOI technology and developing 180 nm and 130 nm CMOS technologies. His current interests include the development of 90 nm CMOS technology. He is a member of the Japan Society of Applied Physics.