# Transistor Design for 90 nm-Generation and Beyond

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**In this paper, we review recent trends in MOSFET scaling such as the aggressive scaling of gate length, the decrease in on-current with scaling, and the increased demand for a variety of transistor types for use in a wide range of target products. To keep up with these trends, there are many device and process issues that need to be resolved. We have categorized these issues and developed new technologies for 90 nm-node transistors. We have fabricated a 90 nm-node transistor with a high on-current and a 40 nm gate length, which is the shortest gate length reported so far for 90 nm transistors. To continue performance improvement for the 65 nm node, it will be necessary to introduce new materials such as high-k gate insulators and breakthrough technologies such as laser annealing. In this paper, we also describe the potentials of these new technologies.**

## 1. Introduction

### 1.1 Aggressive scaling of gate length

The gate length of high-performance MOSFETs has been aggressively scaled year by year because of a strong requirement for constant improvement of circuit performance. The history of the International Technology Roadmap for Semiconductors (ITRS) demonstrates how the gate length of high-performance MOSFETs was scaled in the past and was required to set the pace for scaling in the future. **Figure 1** shows the required first production years for new gate lengths as indicated in the 1994 to 2001 versions of the ITRS.[1] The figure shows a big change between the 2000 and 2001 versions. For example, for the 50 nm gate length, there is a three-year advance from the 1994 version to the 2000 version. On the other hand, there is a five-year advance from the 2000 version to the latest 2001 version.

This radical requirement may be due to a reduction in the pace of performance enhancement by device scaling. Because it has become difficult to further improve transistor performance by advancing the technology node, the gate length has being scaled aggressively. However, this approach has also accelerated scaling in related transistor parameters such as gate oxide thickness, junction

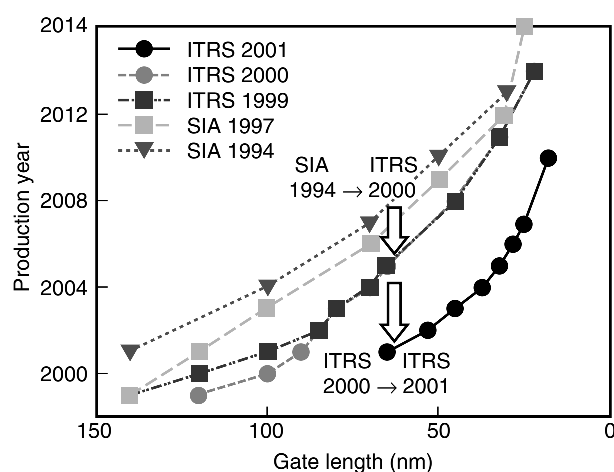


Figure 1
Required first production year of high-performance MOSFETs according to the International Technology Roadmap for Semiconductors (ITRS).

depth, and channel impurity concentration. In other words, the development of overall front-end of line (FEOL) technologies needs to be accelerated and the development term needs to be shortened. Therefore, under these circumstances it is important to choose optimum technologies based on the schedule, performance, and cost.[2)]

## 1.2 Decrease in on-current with scaling

As mentioned above, the aggressive scaling in gate length is due to a reduction in the rate of performance enhancement that can be achieved by device scaling only. The main reason for the reduction is the decrease in on-current that has occurred with the scaling. **Figure 2** shows on-current, gate oxide thickness, and power supply voltage data that has been collected from recent papers presented at major conferences as a function of the target technology node. The off-current is chosen for each node according to 2001 ITRS. We can see from the figure that the on-current reached a peak of over 1000 μA/μm at a node of around 130 nm and then rapidly decreased. There are many factors which influence the current degradation, and we will discuss them later. Two important parameters, gate oxide thickness and power supply voltage, have a strong influence on the decrease in on-current. Until the 130 nm node, gate oxide thickness could be over-scaled and sufficient performance could be achieved through gate overdrive, $V_{dd}$-$V_{th}$ ($V_{dd}$: power supply voltage, $V_{th}$: threshold voltage). However, this approach contributed to the rapid increase in on-current. After the 130 nm node, scaling of these parameters has been difficult due to an increase in direct tunneling through the gate oxide, the existence of an inversion layer thickness, depletion in a poly-Si gate, manufacturability of an ultra-thin film, reliability issues, an increase of sub-threshold leakage, and so on. Because of the on-current trend shown in Figure 2, scaling in gate length must be advanced to achieve the required yearly improvement of circuit performance. Scaling in gate length effectively reduces the gate capacitance, which improves the CV/I metric (C: gate capacitance, V: power supply voltage, I: on-current). This is why there is now a lot of discussion about CV/I in papers on technology nodes. Figure 2 also shows the requirement of on-current from the 2001 ITRS. The difference between the requirement and reported values is larger today than it has ever been, and a possible solution to this problem will be discussed later.

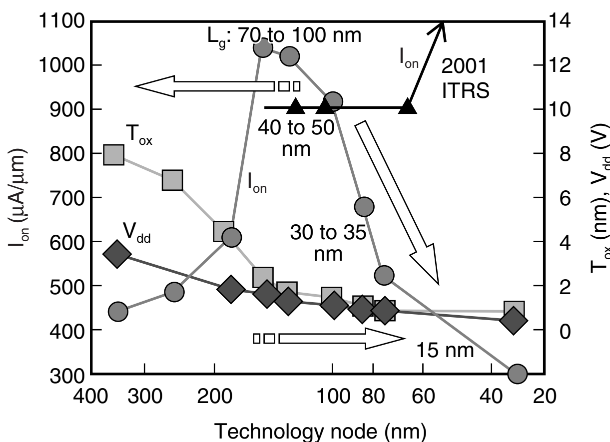


Figure 2
Collected on-current ($I_{on}$), physical gate oxide thickness ($T_{ox}$), and power supply voltage ($V_{dd}$) data from recent papers presented at major conferences as a function of target technology node.

## 1.3 Increased variety of transistor types for a wide range of target products

To satisfy the requirement for a wide range of target products, the transistors used in those products must have varying characteristics. Two of the important parameters are speed and power consumption (**Figure 3**), and another important parameter is the noise margin. To set these parameters to the required levels, different types of transistors should be prepared in a chip or system integration by using multiple threshold voltages, multiple gate oxide thicknesses, multiple gate lengths, and multiple power supply voltages. Process and device engineers need to develop adjustable technologies for single chips and system integrations. These technology de-

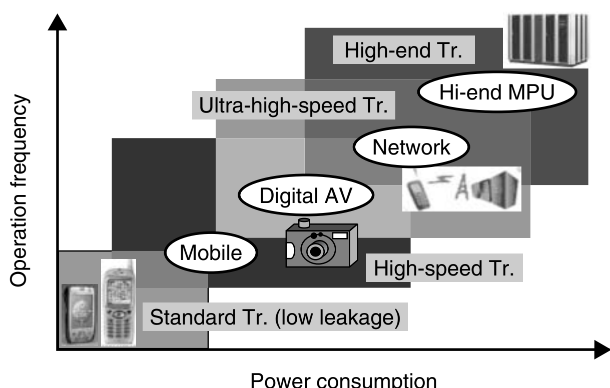


Figure 3
Variation of target products and their transistor types as a function of operation frequency and power consumption.

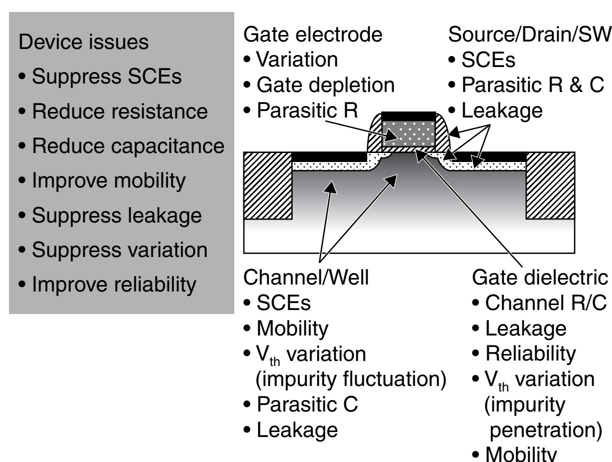


Figure 4
Device issues for sub-90 nm generations assigned to various parts of MOSFETs.

velopments become more and more difficult in terms of cost and time due to the shorter development terms. The business models used to solve these problems advocate the creation of alliances with competitors and the creation of consortiums to obtain more resources at lower cost. The business models, however, must clarify how each chip maker is to make a profit. In this paper, we describe our method of Technology Computer Aided Design (TCAD) for developing a variety of transistor types during a limited period.

## 2. Device and process issues for MOS scaling beyond the 90 nm generation

### 2.1 Device issues

Device issues are classified as follows: suppression of short-channel effects (SCEs), reduction of resistance and capacitance, improvement of carrier mobility, suppression of leakage and variations of electrical characteristics, and improvement of reliability. These issues are assigned to various parts of MOSFETs as shown in **Figure 4**. Since the scaling theory requires that the channel impurity concentration be increased and the supply voltage be reduced generation by generation, we have to avoid a trade-off between immunity to SCEs and a low threshold voltage. Continued scaling is expected to yield devices that have higher speeds. To realize these higher speed devices, we have to increase the drive current (by reducing the channel and parasitic resistance) and reduce the channel and parasitic capacitances. We must realize not only a reduction of parasitic resistances such as the contact and extension resistances, but also a reduction of the carrier mobility due to the increased channel impurity and a minimization of depletion in the gate electrode. Channel capacitance can be reduced by the aggressive scaling of gate length. Other capacitive elements such as overlapped capacitances and junction capacitances can only be moderately or inversely scaled. The importance of these factors increases as the gate length is scaled. For low-power operation, the various leakage currents such as gate oxide tunneling, junction leakage, and gate-induced drain leakage (GIDL) should be suppressed. As the transistor dimensions are scaled, the effect of impurity atoms on the threshold voltage increases. This causes variations in threshold voltage due to the statistical fluctuations in the number and positions of impurity atoms. We must study how the channel engineering that is performed to suppress SCEs affects this variation. Because of the increasing capacity of embedded SRAMs, narrow channel effects should

be suppressed from the viewpoints of power consumption, speed performance, and noise margin.

### 2.2 Process issues

Process issues originate from the device issues mentioned above, but are more process oriented. Gate patterning is critical due to the aggressive scaling in gate length. Higher doping, grain size control, and less deactivation are keys to suppressing gate depletion. A low-temperature salicide process and post-salicide process are necessary to avoid deactivation not only in poly-Si gates but also source/drain contact regions. A shallow junction with a low sheet resistance and abrupt lateral profile is a key for reducing parasitic resistance and capacitance and suppressing SCEs. Various stresses induced by substrates, isolations, side-walls, silicides, and cover films should be artificially controlled to enhance carrier mobility and reduce variations over transistor sizes. A channel impurity profile must be optimized two-dimensionally, not uniformly or one-dimensionally, to realize a low threshold voltage with sufficient immunity to SCEs, and a multi-$V_{th}$ scheme should be prepared. The substrate orientation, surface morphology before gate oxidation, and nitrogen profile in the gate oxide influence the carrier speed and reliability. A highly reliable multi-oxide process must be added without disturbing the channel profiles.

## 3. Device development method

Because of the shortened development period, aggressive scaling, the need for a variety of transistor types, and the other conditions mentioned above, we need to make more effective use of TCAD than ever before. TCAD with optimized process parameters for each generation has been used for predicting electrical characteristics with a variety of process conditions and device structures (**Figure 5**). After iterative calculations with varying process conditions, we attempt to fabricate structures with a limited number of conditions. However, these days, it is necessary to develop new technologies in a short time and achieve a year-by-year improvement in device performance. Also, with each new generation, the optimization of process parameters in TCAD is providing less and less benefits. We need to understand the transistors we fabricate and decide how to quickly improve their characteristics.

We have developed an inverse modeling methodology for this purpose. As shown in Figure 5, this methodology predicts impurity profiles, dimensions, and electrical parameters such as mobility, dielectric constants, and so on from the characteristic measurements of fabricated devices. Therefore, inverse modeling enables us to understand what we make. The methodology is especially effective when we introduce new materials, new dopants, and new effects such as mobility enhancement by artificially adding strain or new crystal orientations, for example, a (110) surface. However, when we use such materials and effects at an early stage of process and device development, it is difficult to use conventional TCAD to predict electrical characteristics without an extensive investigation of parameter values. Therefore, understanding what we make by inverse modeling is a powerful method of quickly developing new technologies.

**Figure 6** shows an example of inverse modeling $I_{on}$-$I_{off}$ characteristics with various power supply voltages. The characteristics obtained by inverse modeling coincide well with the measured ones. This means that the predicted impurity pro-

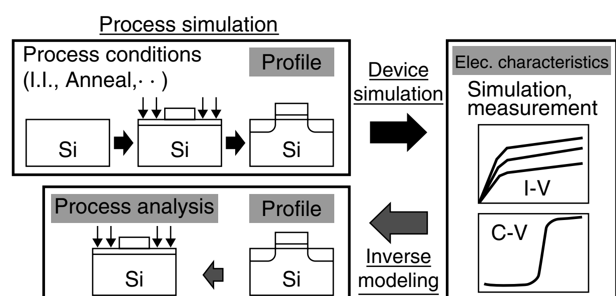


Figure 5
Flow of process simulation, device simulation, and inverse modeling.

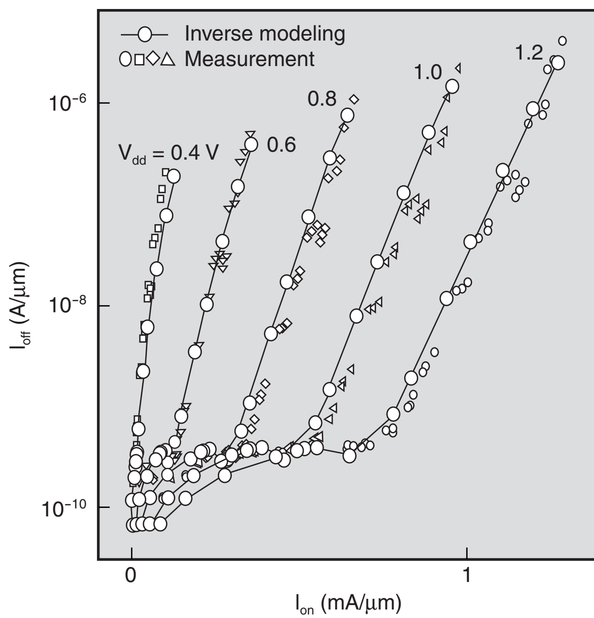


Figure 6
Measured and inverse modeled $I_{on}$-$I_{off}$ characteristics with various power supply voltages.

files, various dimensions, and electrical parameters can be correctly generated on a computer; in other words, we can understand what we make. By using this information, we can effectively approach our goal.

# 4. Development of 90 nm-node MOSFETs

We have integrated 90 nm MOSFETs by carefully considering the issues mentioned above. We have developed many new technologies, but in this paper we will focus on the technologies for increasing the on-current while suppressing SCEs.

The on-current is proportional to the carrier velocity, the inverse of the electrical gate oxide thickness, and the gate overdrive voltage. In order to increase the on-current, these parameters should be increased. By using new materials such as strained Si or SiGe, we can realize higher mobilities. However, for the 90 nm generation, these technologies are not sufficiently matured and we still need to do much research and development to understand, for example, the effects of defects on electrical characteristics and yield, thermal stability, gate oxide integrity, impurity diffusion, and salicide formation. For the 90 nm generation, we increased the carrier velocity by optimizing channel impurity profiles with tilted channel implantation[3),4)] and a notched gate structure.[5)-8)] Because we have to keep up with the aggressive gate length scaling, the increase in carrier velocity must be accompanied by a suppression of SCEs.

## 4.1 Tilted channel implantation (TCI)

A channel-impurity profile must be optimized two-dimensionally, not uniformly or one-dimensionally, to avoid a trade-off between immunity to SCEs and a low $V_{th}$. At gate lengths below which SCEs are severe, the channel-impurity concentration should be increased. This profile can be achieved with tilted channel ion implantation (TCI) after etching a poly-Si gate. Since the overlap of implanted impurities is larger for shorter gate lengths, the concentration of the channel impurities increases and the threshold voltage automatically becomes high, which results in $V_{th}$ characteristics that are only weakly dependent on the gate length.

In addition to the self-aligned channel doping by TCI, more precisely controlled channel profiles will be needed for the 90 nm generation. This is because the increase in channel-impurity concentration must be minimized to avoid a degradation of carrier mobility and to avoid increases in junction leakage and junction capacitance. It is necessary to make a lateral-channel profile with a high peak concentration and rapid decay by TCI. **Figure 7** shows simulated $V_{th}$ roll-off characteristics of transistors with three types of lateral-channel profiles. When the profile is loose and the peak concentration is low, the roll-off becomes poor (#1), but a simple increase in implantation dose causes large reverse SCEs (#3). A high peak concentration and a rapid decay such as that indicated by #2 is promising. Therefore, we have to modify the TCI design by using less diffusive atoms with a small dispersion in the as-

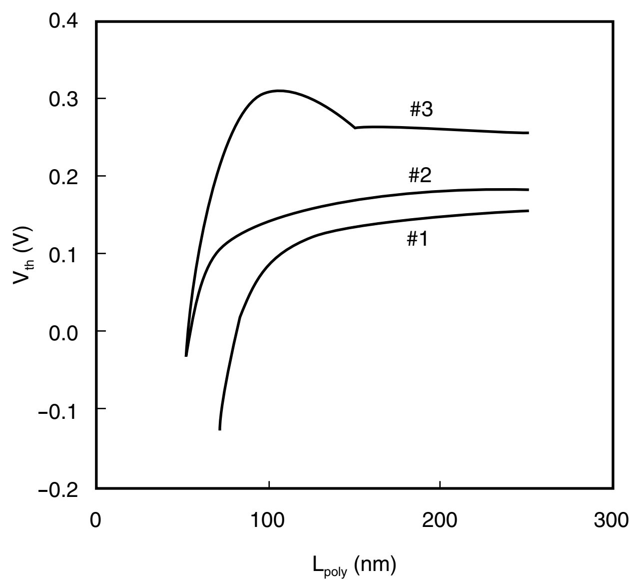


Figure 7 (a)
Simulated $V_{th}$ roll-off characteristics with three types of lateral-channel profiles.

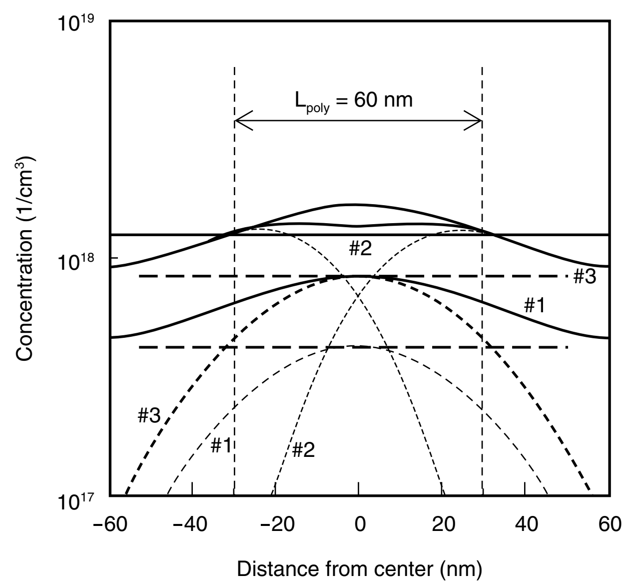


Figure 7 (b)
Three types of lateral-channel profiles for simulation. Solid lines denote the total concentration. Dashed lines denote the concentrations in the TCI components on either side of the gate electrode.

implanted profiles.

Indium is the most attractive p-type impurity because it has a lower diffusivity and heavier mass than boron. By using TCI with indium, we have attained a low threshold voltage and a strong immunity to SCEs. Due to the reduced SCEs, the transistors show a low output conductance. These characteristics also improve the RF performance of the transistor.[9)]

## 4.2 Notched gate structure

Although TCI with a steep lateral profile is effective for reducing channel impurity concentration at the channel center, the impurity concentration at the surface near the source/drain regions becomes high. Therefore, mobility is reduced due to impurity scattering, which becomes prominent at concentrations above $2 \times 10^{18}$ /cm$^3$. To overcome this problem, we have developed a notched gate. **Figure 8** shows schematic impurity profiles of the conventional structure and the notched structure. The notched gate enables us to achieve optimal TCI placement due to its two-dimensional structure, which results in a reduced channel impurity concentration at the surface near the source/drain regions. However, the notch length variation is large when we use a notched poly-Si gate and the structure does not meet manufacturability criteria. Therefore, we have developed a new notched gate structure called the sidewall-notched gate. In the new structure, the notch is formed at the sidewall and not at the poly-Si gate. As a result, we can tightly control the notch length because it is defined by the thickness of the CVD films.

Parasitic resistances such as the extension and contact resistances are suppressed by increasing the impurity concentration. Thanks to this sidewall notched gate structure, we can increase the extension impurity concentration without increasing SCEs.

## 4.3 Ultra-thin gate insulator

The basic way to increase the number of carriers and thereby increase the on-current in 90 nm nodes for high-performance transistors is to use an ultra-thin gate oxide of around 1 nm.

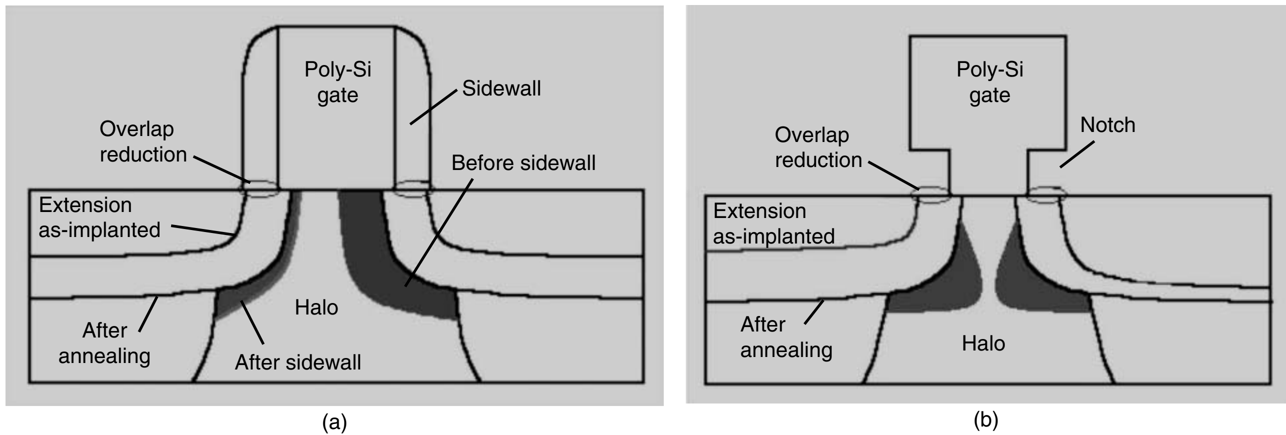


Figure 8
Schematic impurity profiles of conventional structure (a) and notched structure (b).

However, such a thin gate oxide is not a perfect insulator and a large amount of direct tunneling current flows through it, which causes power consumption and reliability problems. Another concern about an ultra-thin gate oxide is that it may be penetrated by impurities, which increases the threshold voltage variation and mobility degradation. A good solution to this problem is to use a thick, high-k gate insulator. However, we developed a nitrided silicon-oxide to overcome these issues. High-k materials, which will be discussed later, are not sufficiently matured at present and cannot be used in 90 nm nodes. We have used a nitrided silicon-oxide that is 1.1 nm thick and is satisfactory in terms of film thickness controllability, on-current requirement, and power consumption. We have optimized two kinds of nitrogen profiles in this film: Type A and Type B (**Figure 9**). Type B is much better than Type A in terms of nMOS drivability, as is clearly shown in **Figure 10**. However, Type B in pMOS is susceptive to boron penetration. We investigated the threshold voltage distribution of pMOS with different activation annealing temperatures. Lower temperature activation annealing is effective to suppress the boron penetration. The temperature should be carefully optimized so as not to increase parasitic resistance.

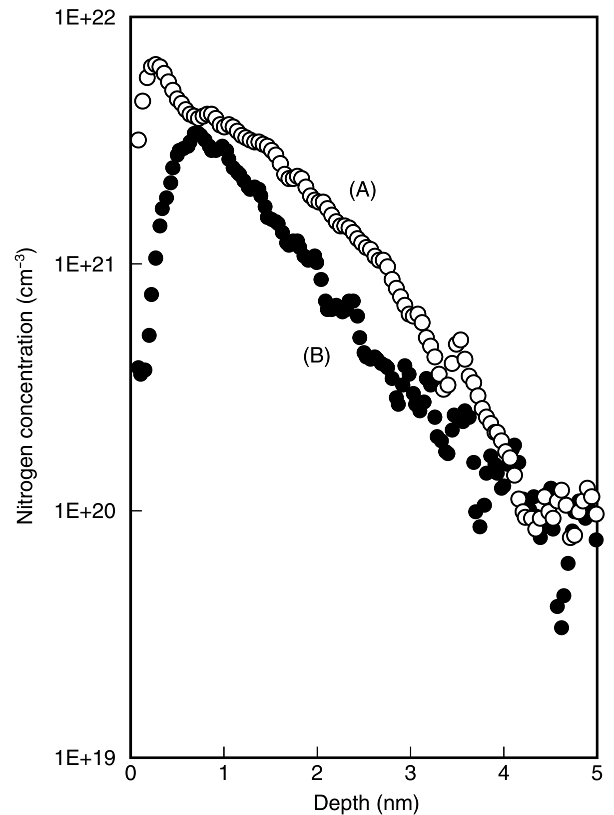


Figure 9
Two kinds of nitrogen profiles in gate oxide.

Not all the transistors in a circuit need to have high-performance. It is therefore important to use multiple gate-oxide thicknesses in applications where speed and power consumption are both important.

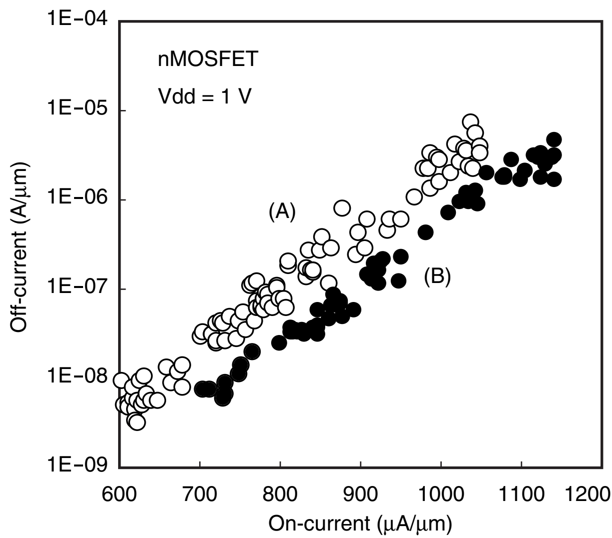


Figure 10
Relation between off-current and on-current with different nitrogen profiles in the gate oxide shown in Figure 9.

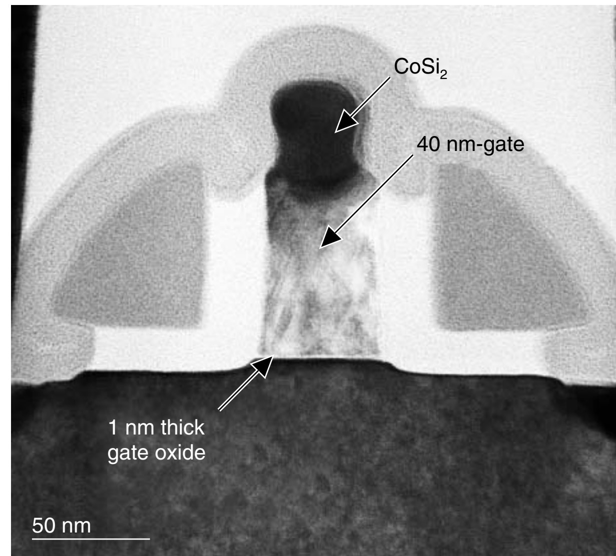


Figure 11 (a)
Cross section of 40 nm gate MOSFET.

### 4.4 Transistor performance

**Figure 11 (a)** shows a cross section of a 40-nm gate MOSFET. **Figure 11 (b)** shows the relation between the on-current and off-current of this device at a supply voltage of 1 V. At an off-current of 100 nA/μm, the on-currents are 890 μA/μm for nMOS and 380 μA/μm for pMOS. Among recently reported transistors for 90 nm nodes, our gate length is the shortest and also has a high on-current. According to the on-current and CV/I metric, our device has the highest performance.

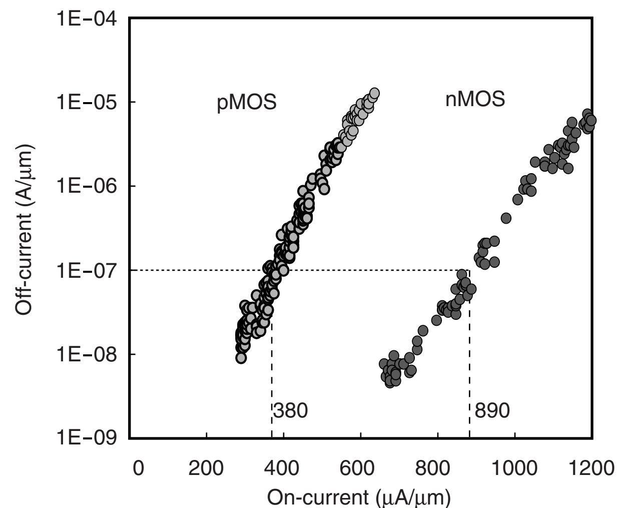


Figure 11 (b)
Relation between on-current and off-current at supply voltage of 1 V.

## 5. Variation in $V_{th}$ caused by channel engineering

In addition to process variations, the device characteristics of short-channel MOSFETs are seriously affected by statistical variations in the dopant number and position. This is serious because fluctuations cannot be suppressed by eliminating process variations. The channel-dopant distribution includes not only the number distribution but also the position distribution. As mentioned above, indium-TCI implantation forms a profile which is characterized by two-dimensionally optimized profiles Therefore, the TCI profile seems to be susceptible to $V_{th}$ fluctuations due to impurity-position variations. We studied how the profile affects the $V_{th}$ fluctuation by comparing the I-V measurements of a MOSFET under interchanged source/drain bias conditions.[10),11)] Asymmetrically placed channel

impurities produce different I-V characteristics for the forward (F) and reversed (R) bias conditions. Examples of measured Id-Vg data at Vd = 0.02 V and 1.2 V are shown in **Figure 12**. Although we can see no difference between the F and R conditions at Vd = 0.02 V, there is a large $V_{th}$ shift ($dV_{th}$) between them at Vd = 1.2 V. This is due to the statistical variation in channel-impurity positions.

We have investigated the effects of channel engineering on $dV_{th}$. We measured $dV_{th}$ with transistors fabricated under a variety of conditions for TCI and found that $dV_{th}$ increases with the TCI dose and energy. The large $dV_{th}$ under strong TCI conditions occurs because the region of the potential barrier is narrower under strong TCI conditions, resulting in a large dopant fluctuation.

## 6. Toward the 65 nm node

As mentioned above, our transistor design for 90 nm nodes is based on historical scaling and provides high performance. We will now look at how we can progress toward 65 nm nodes. Scaling in gate length continues, and we can even find several reports on transistors with a sub-30 nm gate length. However, as shown in Figure 2, the on-current is much smaller than that required by the ITRS. We therefore need a breakthrough in process technology or new materials and structures to meet the requirement for 65 nm nodes. The concept of the transistor roadmap beyond the sub-90 nm node is shown in **Figure 13**. The performance improvement achieved by conventional scaling becomes smaller, and the performance improvement achieved by new materials, new effects, and new structures becomes large. It will be harder to define the meaning of the term “technology node” beyond sub-90 nm nodes, and we need to continuously introduce new technologies.

In the next section, we present two breakthrough technologies: a gate oxide technology and a shallow junction technology.

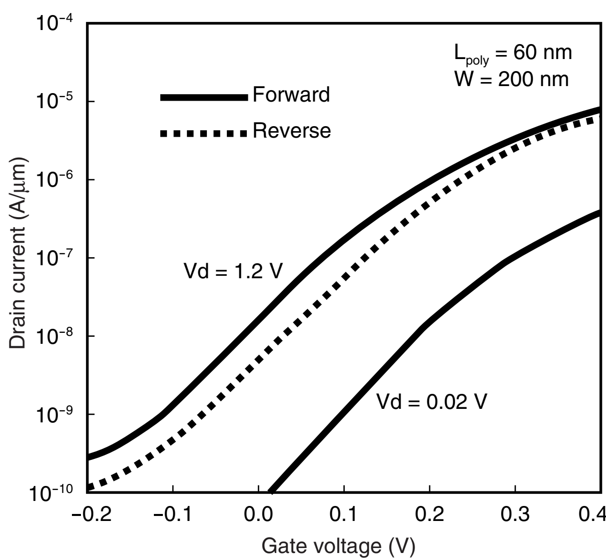


Figure 12
Measured Id-Vg characteristics at drain voltages of 0.02 V and 1.2 V under Forward and Reverse conditions.

### 6.1 High activation and shallow junction technologies

The drive current in a MOSFET can be increased by reducing the resistive elements, which can be divided into channel and parasitic parts. As mentioned above, the channel resistance is being aggressively reduced by scaling the gate length and the gate-insulator thickness. On the other hand, the parasitic resistance consists mainly of the contact resistance between the silicide and diffused regions and the resistance at extension regions.

Contact resistance increases with scaling. An

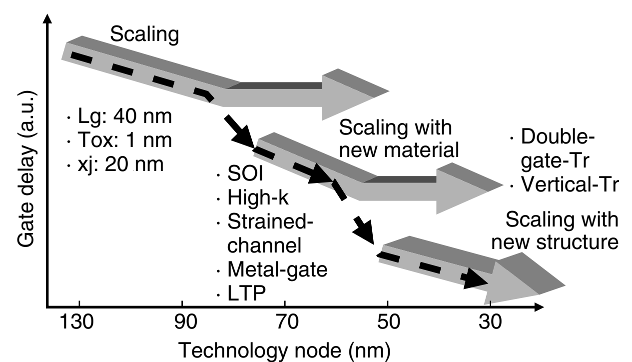


Figure 13
Concept of transistor roadmap beyond the 90 nm node.

increase in the electrically active impurity concentration is the most effective method of reducing the contact resistance. The traditional approach is to use a higher RTA temperature and a shorter RTA time. The ultimate type of RTA is laser annealing. We have developed a laser annealing process that reduces the contact resistance.[12] We achieved a very low contact resistivity of $4 \times 10^{-8}$ Ω·cm$^2$, which is five times lower than that achieved through conventional RTA. **Figure 14** shows the projected contact resistance of laser annealing and RTA devices as a function of the technology node, $L_D$. It is assumed that the distance of the silicided source/drain region is $2 \times L_D$ and the required contact resistance ($2 \times R_c$) is 10% of the channel resistance. Performance of devices fabricated using the RTA process will be limited by the contact resistance in the 0.1 μm generation. The laser annealing process extends device scaling by maintaining a low contact resistance down to 50 nm nodes.

The impurity profile at the source/drain extension region is the key to reducing the extension resistance and suppressing SCEs. The impurity profile must have a high surface concentration and

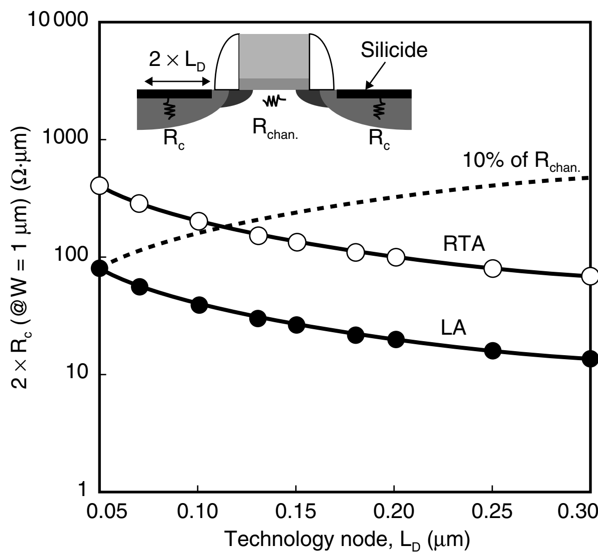


Figure 14
Projected contact resistance of laser annealed and RTA devices as a function of technology generation, $L_D$.

be laterally abrupt.[13] We have developed a laser annealing technology in which the extension junction depth, overlap, and sheet resistance are controlled by using a pre-amorphization extension region before laser annealing.[14] This enables us to design highly activated and abrupt box-like dopant profiles without inducing any short-channel deterioration. Compared to the conventional RTA technique, this technique enabled us to fabricate higher drive current, 45 nm pMOSFETs with the same $V_{th}$-rolloff and a 13% improvement in drivability. Also, as shown in **Figure 15 (a)** and **(b)**, with this technology we achieved the sheet resistance and profile abruptness required for the 65 nm node of the 2001 ITRS.

## 6.2 High-k gate dielectric

Frontier work on transistors with a high-k gate insulator was first reported in 1997 at the Symposium on VLSI Technology.[15] At the symposium, there was only one paper on high-k; however, in 2002, there were four sessions on high-k and a total of 17 high-k papers were presented. This increase in interest in high-k occurred because, according to the 2001 ITRS, high-k dielectrics will be first required for low leakage current applications in 2005. Recently, there has been much interest in hafnium dioxide ($HfO_2$) due to its thermodynamic stability in a poly-Si gate, its high dielectric constant, and its high band gap. High-k materials must have process compatibility with the conventional CMOS process, which means that they must be able to withstand the high-temperature process.

We introduced a thin interfacial layer between the Si substrate and $HfO_2$, which effectively improves thermal stability. We used a 3 nm, $HfO_2$ gate dielectric and fabricated 55 nm-gate-length CMOS devices with low off-state currents and high inversion capacitances.[16] The CMOS fabrication process includes dual-doped poly-Si gates, high-temperature annealing ≥ 1000°C, cobalt silicide, extensions, and pocket implants. The $HfO_2$ film was deposited by ALD. In **Figure 16**, we

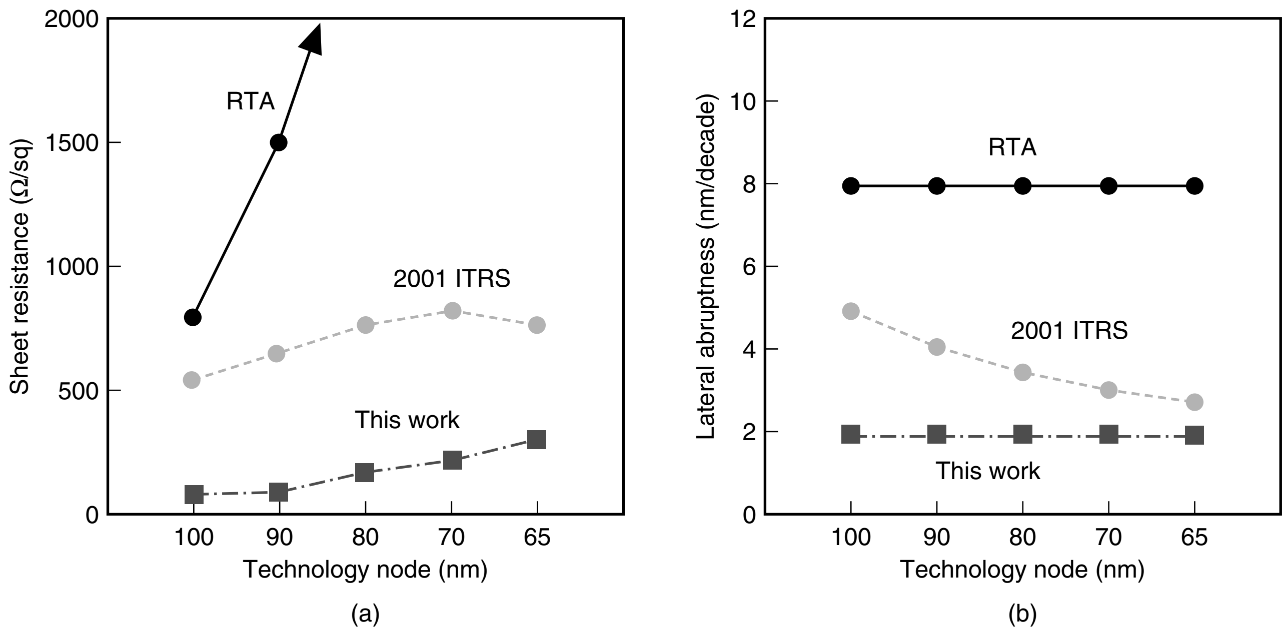


Figure 15
Comparison of sheet resistance and lateral abruptness.

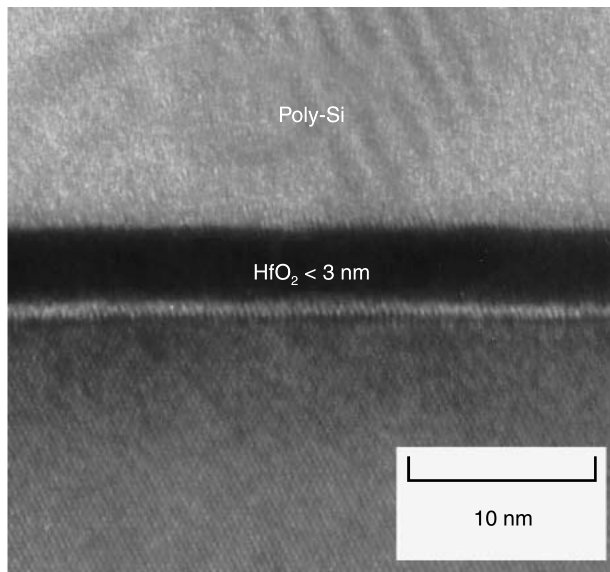


Figure 16
Cross-sectional TEM photograph of ultra-thin (< 3 nm) $HfO_2$.

show a cross-sectional TEM photograph of an ultra-thin (< 3 nm) $HfO_2$ film with very good uniformity. A very thin (less than 0.5 nm) interfacial layer is visible at the silicon substrate-$HfO_2$ interface.

The electrical oxide thickness of the $HfO_2$ film is approximately 1.4 nm, as estimated from the accumulation capacitance. High-temperature annealing provides good suppression of gate depletion and also makes it possible to achieve 1.4 nm $HfO_2$ devices. **Figure 17** shows that a reduction in gate leakage current of more than three orders of magnitude is achieved using $HfO_2$ as compared to a reference $SiO_2$ gate dielectric. **Figure 18** shows the well-behaved drain current-gate voltage characteristics for 55 nm MOSFETs. These MOSFETs have an off-state current of 25 pA/μm.

## 7. Conclusions

In this paper, we reviewed recent trends in MOSFET scaling and related issues. Although the issues are becoming more difficult to resolve as the gate length is scaled down, high-performance has been realized in 90 nm nodes through precise optimization of the channel impurity profile, a notched gate structure, and an ultra-thin gate insulator of 1.1 nm. However, for 65 nm nodes and beyond, it seems difficult to perform conventional scaling without degrading performance. For 65 nm nodes, to continue performance improvement it will be necessary to

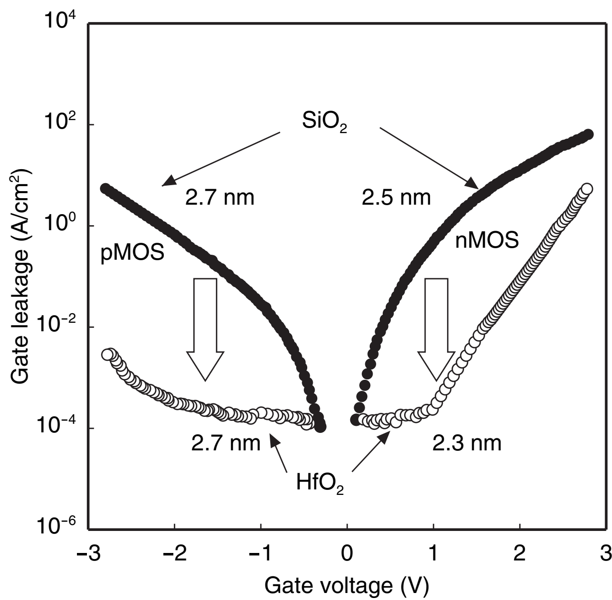


Figure 17
Gate leakage characteristics of $HfO_2$ and $SiO_2$ with nearly the same electrical oxide thickness.

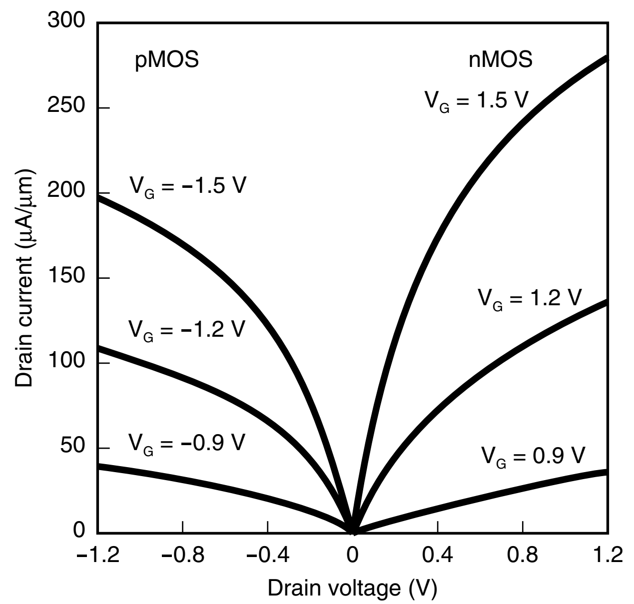


Figure 18
Drain current-drain voltage characteristics for 55 nm MOSFETs.

introduce new materials such as high-k gate insulators and breakthrough technologies such as laser annealing. After the 65 nm node, it will be harder to define the meaning of the term "technology node," and a variety of new materials, effects, and structures will be introduced to achieve a balance between performance, cost, and development time. In other words, different types of nodes will be developed to meet the special needs of each application. The time for the introduction of new nodes therefore depends on the application, so there will be less need for a definition of technology nodes by the ITRS.

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