Research and Development of Advanced CMOS Technologies

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Advanced CMOS technologies will be very important keys for increasing system performance in the coming information society. To meet market requirements, Fujitsu is continuously making developments in leading-edge CMOS technologies and supplying them to captive systems as well as to outside consumers. This paper describes the current status of Fujitsu's R&D for next-generation CMOS and beyond.

1. Introduction

Semiconductor technologies are becoming increasingly important in the developing information society, with higher and higher value being added to electronic systems. The global market of semiconductor products has increased by approximately 17% every year over the last 20 years, which is much higher than the average yearly electronics market increase of 9%. Semiconductor products already account for 20% of the total value of all electronic products. So far, two products–microprocessors (MPUs) and dynamic random access memories (DRAMs)–have been the main drivers of the markets and mobile and digital-consumer products have been the secondary drivers. CMOS technologies will surely continue to be the core technologies in these products.

Fujitsu has recently established a new development center for advanced CMOS technologies in Akiruno, which is a suburb of Tokyo. One of the missions of the Center is to research and develop globally competitive CMOS technologies, especially internal high-end system applications, in cooperation with Fujitsu's information and communication system groups as well as Fujitsu Laboratories Ltd.

This special issue of the FUJITSU SCIENTIFIC & TECHNICAL JOURNAL covers the current status of CMOS research and development in Fujitsu Ltd. and Fujitsu Laboratories Ltd.

2. System requirements and markets

The main semiconductor technology drivers at Fujitsu have been high-performance computers, mainframe computers, high-end servers, and supercomputers. **Figure 1** shows several types

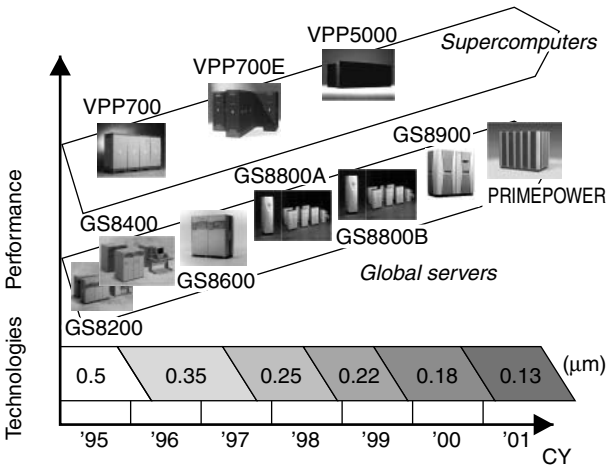

Figure 1
Fujitsu's high-end systems and semiconductor technologies.

of the platform supercomputers and global servers that Fujitsu has produced since 1995. These units originally used bipolar technologies and then switched to CMOS technologies in the late 90s because of their superior performance. A continuous increase in system performance has been achieved in step with the progress achieved in CMOS technologies. Our latest range of global servers is the PRIMEPOWER range, which uses 180 nm CMOS technologies.

In addition to the above-mentioned internal applications, the semiconductor business group is responsible for supplying the CMOS devices that form the cores of products in the rapidly expanding markets for networks, mobile communications, and home digital-consumer products. The R&D groups in Fujitsu's Akiruno Technology Center closely study the market requirements and then decide which technological issues Fujitsu should investigate. The Center also develops the infrastructures of LSI production lines such as those for CIM (Computer Integrated Manufacturing) systems to achieve a quick turnaround time (TAT) (**Figure 2**).

Figure 3 shows how technology has developed since 1970 and a technology projection for up to 2015. As can be seen, the number of transistors on a chip has increased by 3 orders of magnitude every 15 years. Currently, we can integrate one billion transistors on a silicon chip.

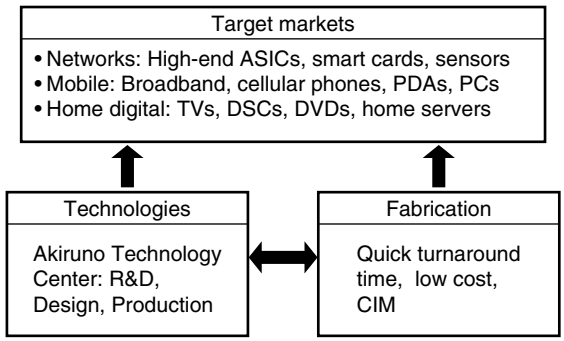

Figure 2
The mission of the Akiruno Technology Center and target markets.

DRAM was the technology driver until the middle 80s, when mainframe computers, calculators, video recorders, and other equipment required a large amount of DRAM as well as various kinds of LSIs. The key factors in productivity were fine lithography and dry processes for higher circuit packaging densities. Then, personal computers that used high-performance LSIs became the main products and system performance depended on high-speed MPUs. Higher performance chips with more sophisticated functions were produced by using new chip architectures and new circuit designs. Interconnection and planarization technologies became key technologies for reducing signal delay and increasing circuit densities. In the next 15 years, most of the discrete logic and memory of equipment will be realized using a System-on-a-Chip (SOC). The architecture and design for embedded logic/memory and the system verification will become important for adding value to chips. Also, it will become essential to reuse intellectual property (IP) to reduce the cost of design.

Figure 4 shows an example of an SOC for a portable data assistant (PDA). The device contains a CPU and two DSPs and has various functions for the communications, pen-input, voice-recognition, display, and smart-card interfaces.

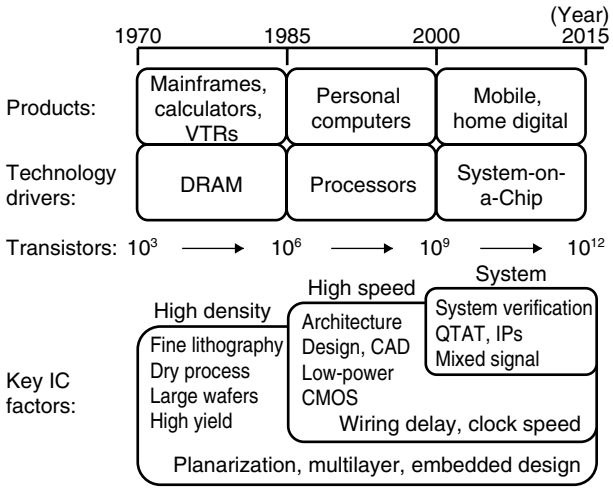

Figure 3
Product trend, technology drivers, and key IC factors.

3. Technology direction

Every year, the committee of the International Technology Roadmap for Semiconductors (ITRS) publishes a summary of projected technology trends. **Figure 5** reproduces a graph that appeared in ITRS 2001 showing how gate length has been reduced and how it might continue in the future.[1] The minimum mask length is now 130 nm for the most advanced chips under production and will be decreased in 2003 to 90 nm for the next generation and then to 65 nm in 2005 and 45 nm in 2007. From this figure, we can see that the rate of reduction in gate length has fallen over the last three years and is approaching a limit. We are aggressively reducing the gate length of our high-end MOS transistors to achieve the highest performance from the same structure. The CS100 and CS200 transistors have, respectively, 40 nm and 28 nm gate lengths. The process for the CS100 presents various technological challenges,[2] some of which are described elsewhere in this special issue.

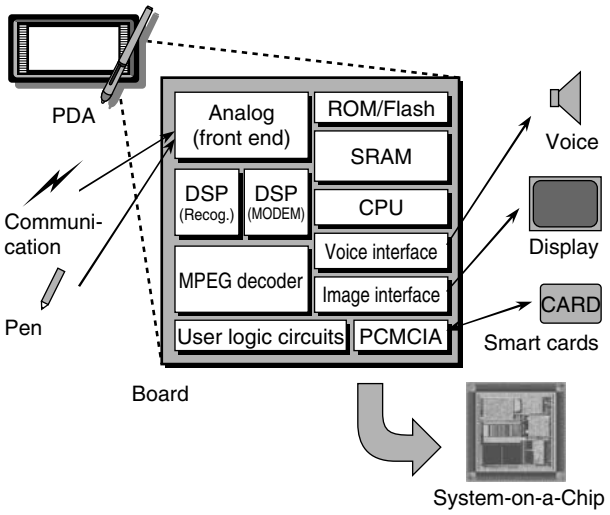

Figure 4
Example of a System-on-a-Chip (SOC) that includes functions for a human interface and processors.

The signal delay on a chip consists of the gate delay and the wiring delay. **Figure 6** shows how progress in transistor design has decreased the gate delay of MOS transistors. This progress has basically continued according to a scaling rule. However, the wiring delay cannot be further reduced simply by reducing the transistor scale, because such a reduction also increases the stray capacitances of the wiring and electrodes. To increase chip performance, it is necessary to use Cu wiring, which has a low resistance, and a low-k

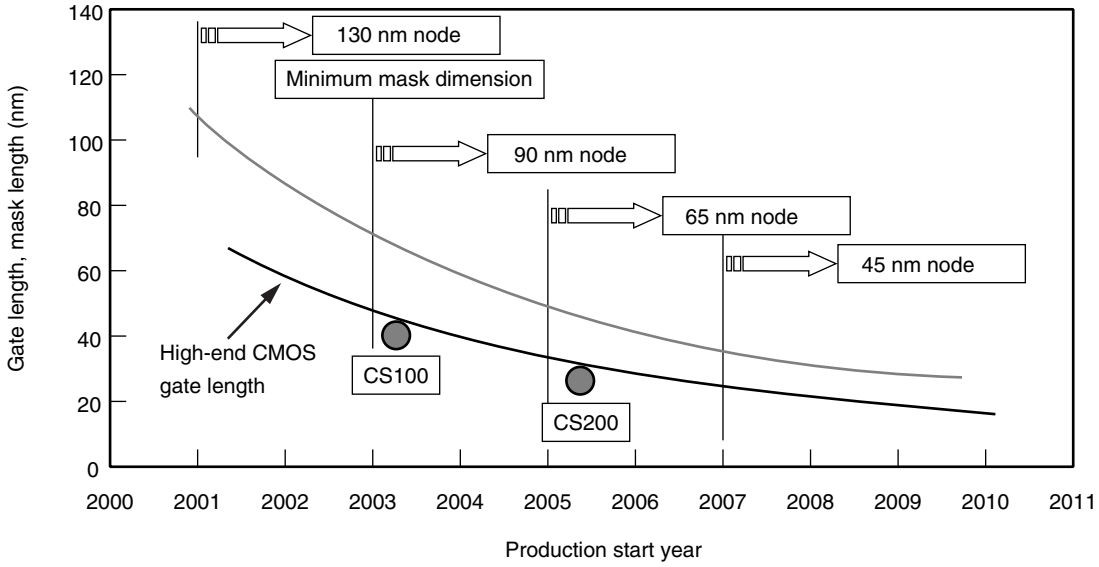

Figure 5
Trends of minimum mask dimension and CMOS gate length.

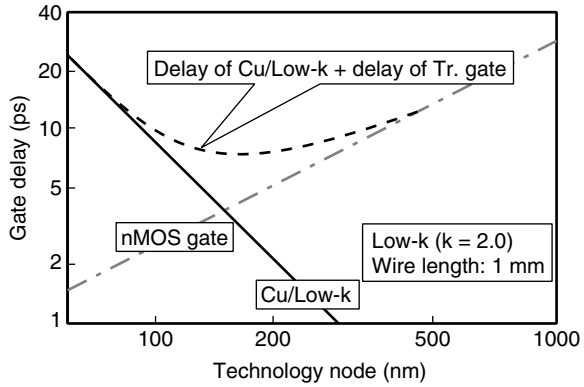

Figure 6
Signal delays of CMOS chips achieved by progress in structure design.

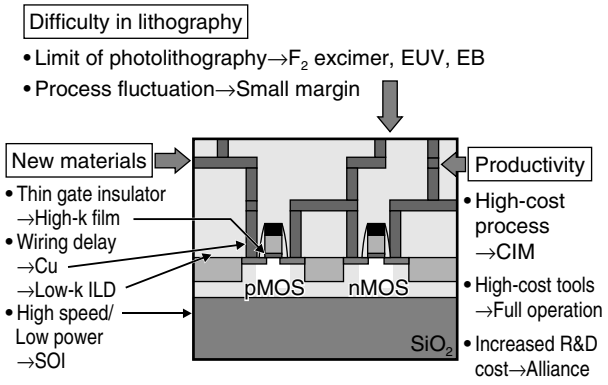

Figure 7
Key development factors of next-generation CMOS and beyond.

dielectric interlayer. As shown in Figure 6, signal delays as small as around 7 picoseconds can be achieved when 1 mm Cu wiring and a low-k dielectric layer are used in a 180 nm MOS transistor. Further reductions can be achieved by using even shorter wiring lengths and even smaller structures.

4. The main CMOS technology issues

Figure 7 shows a cross-sectional diagram of a CMOS LSI. The main issues for next-generation devices are fine line patterning, new materials, and chip productivity. Conventional optical lithography is reaching its limit, and the candidate replacements are electron beam and extreme-ultra violet lithography. However, to make the transition to these new technologies, various problems will need to be overcome, for example, how to reduce the process variations that occur when finer patterns are used.

The next increase in performance will be achieved through the introduction of new materials. In addition to the previously mentioned Cu wiring and low-k dielectrics, we will need to replace the conventional SiON gate dielectrics with high-k materials to suppress leakage in MOS gates. Also, we can reduce capacitances and thereby increase device speeds and reduce power consumption by employing silicon on insulator (SOI) technology.

Use of these new technologies will inevitably lead to an initial increase in production costs, so it will be important to implement advanced process control, fault detection, and fault classification systems. Also, new algorithms and diagnostics will need to be developed before these systems can be effectively implemented in a fabrication plant's CIM system. Once these systems have been implemented, we will be able to start full-scale operation of process equipment and therefore reduce production costs. One way to prevent an increase in R&D costs is to cooperate with consortia.

Figure 8 shows a possible scenario for MOS development. For the 90 nm CS100, a careful scaling design, short channel, thin gate insulator, and shallow junction are fundamental requirements. Although we are reaching the optimization limits of these parameters, new materials will enable further increases in MOS performance. SOI, high-k gate insulators, metal gates, and strained silicon channels will be used in the next-generation 65 nm structures.[3] The ultimate MOS transistor may be a double-gate device with a fine gate structure. Fujitsu proposed a fundamental process and structure in 1994[4),5)] and intends to use it to produce structures in the 45 nm realm and even finer

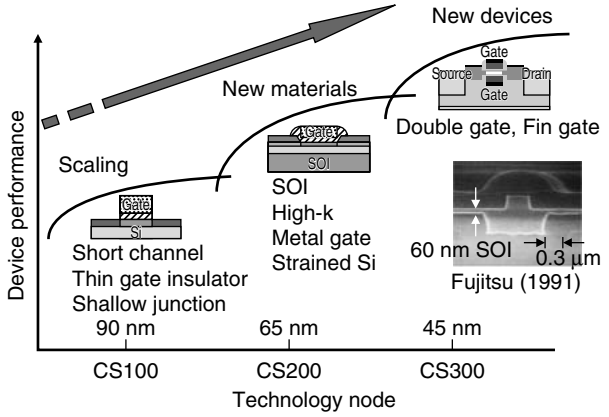

Figure 8
Increase in CMOS device performance.

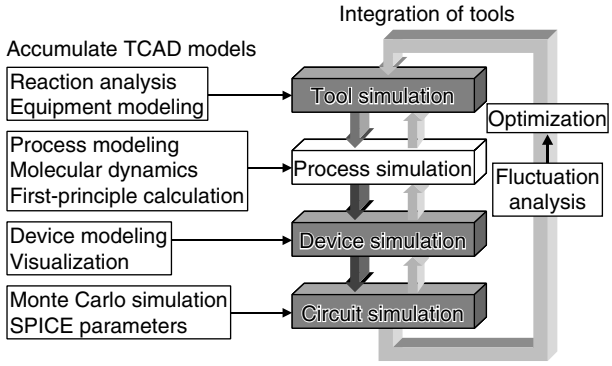

Figure 9
How we are developing our simulation system.

structures. However, the process requires further improvements, for example, a self-alignment technique for both gates.

Finally, simulation will become more and more important when developing new technologies. **Figure 9** shows how we are developing our simulation system. Fluctuation analysis, characteristics optimization, and reliability analysis are done by integrating the simulation tools for circuit design and device processes. Improvements in technology CAD (TCAD) models are necessary. We need to develop accurate device and process models based on observations of material phenomena. We are investigating molecular dynamics, first-principle calculations, and Monte Carlo simulations to support various models for process simulation. Also, we are paying more attention to soft error simulation, because of its increasing influence on device reliability. (Soft error simulation is useful for reducing TAT and the cost of device development.)

5. Conclusion

Advanced CMOS technology is a key for increasing system performance. Fujitsu continues to meet market requirements by developing leading-edge CMOS technologies and then applying them in internal systems and providing them to its customers. This special issue covers the current status of R&D for the next and future generations of CMOS devices.

References

1) International Technology Roadmap for Semiconductors (2001 Edition), jointly sponsored by EECMA, JEITA, KSIA, TSIA, and SIA.
2) S. Nakai, Y. Takao, K. Sugiyama, H. Ohta, A. Yamanoue, Y. Iriyama, R. Nanjyo, S. Sekino, et al.: A 100nm CMOS Technology with Sidewall-Notched 40nm Transistors and SiC-Capped Cu-Low-K Interconnects for High-Performance Microprocessor Application. Symp. on VLSI Tech., Digest of Tech. Papers, p.66-67 (2002).
3) M. Shima, T. Ueno, T. Kumise, H. Shido, Y. Sakuma, and S. Nakamura: <100> Channel Strained SiGe pMOSFET with Enhanced Hole Mobility and Lower Parasitic Resistance. Symp. on VLSI Tech., Digest of Tech. Papers, p.94-95 (2002).
4) T. Tanaka, K. Suzuki, H. Horie, and T. Sugii: Ultra-fast Low-power Operation of p-n Double Gate SOI MOSFETs. Symp. on VLSI Tech., Digest of Tech. Papers, p.11-12 (1994).
5) K. Suzuki, Y. Tosaka, T. Tanaka, A. Satoh, and T. Sugii: Scaling Theory for Vth Controlled n-p Double Gate SOI MOSFETs. Ext. Abs. of Int. Conf. Solid-State Devices and Materials, p.274-276 (1994).

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