Preface
Special Issue on Advanced Silicon Device Technologies

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We have now entered the 21st century and can see that many of the electronic appliances and systems around us are installed with organically interconnected computers that form a worldwide network. Thanks to the incredible pace of technological progress, we are steadily proceeding to the Ubiquitous Network Society, in which this worldwide network can be used by anyone, anytime, and anywhere. The key requirements for CMOS to realize the Ubiquitous Network Society are to increase the operation speed and integration scale and also reduce the power consumption.

Up to the deep-submicron devices, these requirements have been met mainly by the continuous efforts of device size scaling. However, when the device size is reduced to below 0.1 micron, new materials and new device structures as well as more advanced device scaling technologies will become essential. When we scale down even further to 0.01 micron devices, we are destined to encounter the physical limits of CMOS, and to be sure where these limits are we will need to use more sophisticated simulation technologies.

This special issue on Advanced Silicon Device Technologies describes the results of recent research on the performance and reliability of the next and future generations of CMOS devices, key process technologies, and simulation technologies that support further development of CMOS.

The first section contains nine papers about CMOS device performance and reliability improvements that have been achieved by using state-of-the-art technologies. The first two papers review advanced transistor fabrication technology and transistor design for the next and future generations of CMOS. The next three papers describe integration and device fabrication technologies that have mainly been developed to obtain higher performance and reliability and lower operation power in

90 nm CMOS. These are followed by a paper on a Dynamically Programmable Gate Array with Ferroelectric Memory Technology and a paper on Process and Device Technology for 0.13 µm FCRAM. The remaining two papers in this section present some novel device structures for logic and memory that address the requirement for a lower device operation voltage.

In the next section, we present two papers on process technologies for overcoming the reliability and scaling limits of CMOS. The first of these papers is on Reliability Improvement in Deep-Submicron nMOSFETs by Deuterium, and the second is on High-k Gate Dielectrics for Advanced CMOS for gate lengths below 0.05 micron.

In the last section, we cover some advanced simulation technologies for CMOS. The papers in this section include descriptions of simulations we have conducted that enable a precise understanding of phenomena that occur during device fabrication and operation and an atomic-scale understanding of the materials used for sub-0.1 micron CMOS. By using the results of these simulations, we can control device fabrication processes more precisely and also correctly predict the scaling limits of CMOS.

We hope that this special issue will help readers grasp the various technical aspects of Silicon Device Technologies and use our CMOS devices to find and develop new technology application areas.