Advanced Device Technologies for IMT-2000 Systems

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In IMT-2000, the deployment of advanced device technology is the key factor for achieving various system requirements, for example, increasing the number of subscribers, high-speed transmission, efficient usage of battery power, and expanding the functionality.
In this paper, we introduce our achievements in the development of advanced devices such as high-power GaAs FETs, small-volume SAW filters, and low-power baseband devices and in the development of a mobile multimedia platform.

1. Introduction

The mobile system has made remarkable progress over the last 20 years. It is widely acknowledged that the rapid expansion of mobile communications has been due mainly to the remarkable progress in the related component technologies. Actually, a technology-integrated system such as a mobile system cannot be realized without advanced devices. This is furthermore the case in IMT-2000, which requires extraordinarily advanced features such as high-power radio transmission and complex modulation-demodulation processing to achieve wideband transmission within a limited radio band. Application functions, including signal processing, are also becoming more complex to provide feature-rich services to customers.

Fujitsu has been making great efforts in the components area and has provided advanced component solutions, some of which are now in widespread use around the world. We have developed many new devices for IMT-2000 and have contributed to the system's realization on the base station side and on the terminal side.

This paper introduces some of the new IMT-2000 devices Fujitsu has developed and discusses some related topics. As can be seen from **Figure 1**, which shows the block diagram of an IMT-2000 mobile phone handset, IMT-2000 is a complex system that requires devices for applications ranging from radio interfaces that operate in the GHz band to application software for terminals. Therefore, we will discuss them in the following sections by classifying the technologies and system areas.

In Section 2, we describe some high-power GaAs FETs for high-power radio transmission; and in Section 3, we describe some SAW filters, which are key components for achieving 2 GHz level filtering. Then, in Section 4, we discuss some baseband CMOS device solutions. Finally, in Section 5, we introduce a variety of chips for the applications area.

2. High-power GaAs FET

Compared to previous systems, IMT-2000 requires power amplifiers with higher output power and better linearity. We have successfully demonstrated a device capable of handling 300 W,[1)] and a 240 W device is being developed for mass

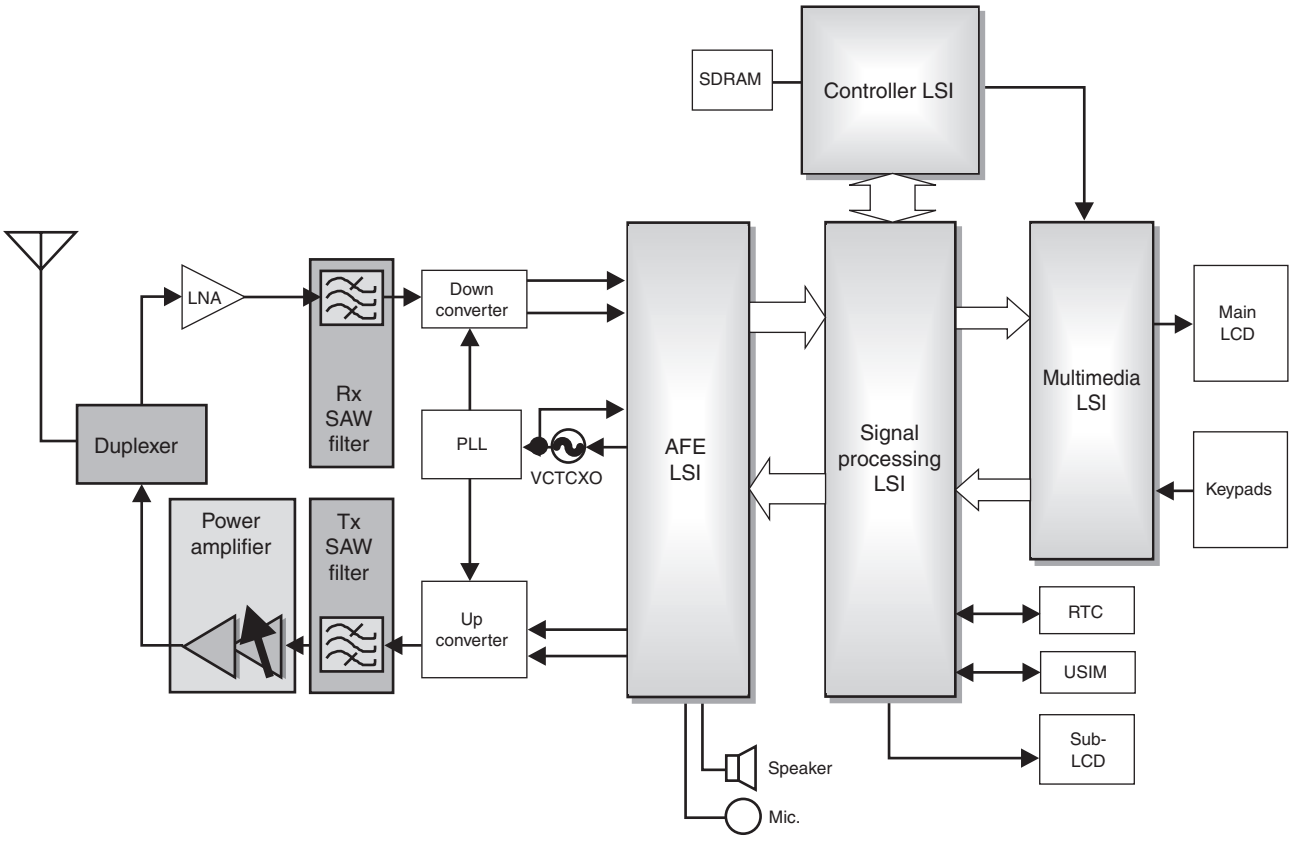

Figure 1
System block diagram of IMT-2000 mobile phone handset.

production. In this section, we describe a 60 W FET device with high linearity and low thermal resistance and a 240 W assembly of four of these 60 W devices.

2.1 Device structure

A GaAs epi-base MESFET structure was adopted for the high-power FET. The device consists of an Si doped GaAs channel layer, an AlGaAs schottky layer, and a GaAs cap layer with a WSi/Au T-shaped gate and Au/Ge/Ni/Au alloyed ohmic contacts. All active areas are covered with SiN passivation.

There are two key points for realizing high-power and high-linearity GaAs FET devices for IMT-2000 applications:

1) High transconductance (g_m): Based on Volterra series analysis, the 3rd order intermodulation distortion (IM3) ratio was found to be directly related to g_m, so increasing g_m can be a very effective method for improving linearity.[2] We therefore adopted a highly doped, thin-channel FET structure to improve both the power-added-efficiency (PAE) and the linearity.
2) Low thermal resistance (R_{th}): The thermal design is a very critical issue for high-power devices. The unit gate width (W_{gu}) and gate-to-gate length (L_{gg}) were optimized after considering the trade-off relationship between RF gain characteristics and thermal resistance and the need to keep the width within the limits of a practical device. In addition, a plated-heat-sink (PHS) structure was adopted to optimize thermal transfer. The GaAs wafer is thinned to 28 µm and plated on the rear with 30 µm of gold.

Figure 2 shows a photograph of the 60 W output device used in the 240 W assembly. The device consists of 14 cells with 16 gate fingers with

a W_{gu} of 870 µm, so the total gate width (W_{gt}) is 195 mm. The overall size is 4.0 × 1.4 mm.

2.2 Power performance

Figure 3 shows a photograph of the 240 W push-pull power FET. The package is 34.0 × 17.4 mm. A pair of 60 W output devices is combined with an in-phase divider and combiner, and two of these combinations are assembled in a package and used in a push-pull configuration. The optimum impedance of each device port was estimated from load-pull measurements.

Figure 4 shows the measured output power and power-added efficiency (PAE) of the 240 W push-pull FET at 2.14 GHz. A saturation power of 53.8 dBm (240 W) is achieved with a linear gain of 12.0 dB and a PAE of 50%.

Figure 5 shows the adjacent channel leakage power ratio (ACPR) as measured using an IMT-2000 modulation signal. An ACPR level of –36 dBc is achieved with a PAE of 24%.

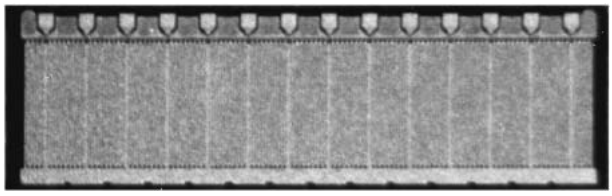

Figure 2
Photograph of 60 W output device.

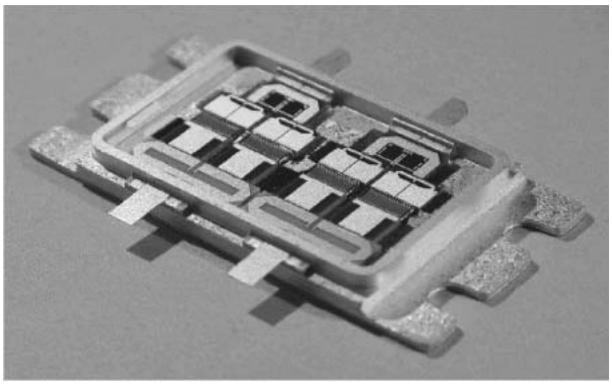

Figure 3
Top view of 240 W push-pull FET.

2.3 Reliability

The devices used for infrastructure applications, for example, in a base station system, must also be highly reliable. A high-temperature operation test was performed to estimate the mean time to failure (MTTF) of the device. The definition of MTTF is given below.

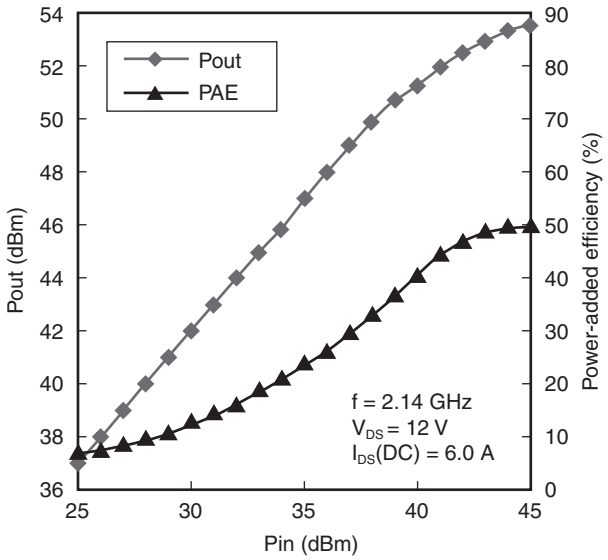

Figure 4
Output power and power-added efficiency versus input power. f = 2.14 GHz, V_{DS} = 12 V, I_{DS} (DC) = 6.0 A.

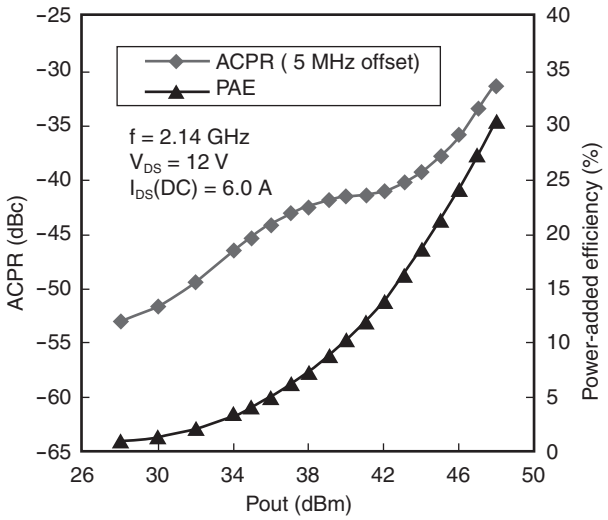

Figure 5
ACPR and power-added efficiency versus output power. f = 2.14 GHz, V_{DS} = 12 V, I_{DS} (DC) = 6.0 A.

MTTF = T/r

T: total test time (test time × test quantity)

r: number of failures

The test was conducted with 10 W devices. The channel temperature (T_{ch}) was set to 220°C. Failure was defined as a reduction in power or gain of more than 0.5 dB. The test showed no failure up to 9600 hours.

To estimate the MTTF at the expected operating channel temperature, we assumed that the activation energy (E_a) was 1.79 eV, which was extracted from a test conducted for GaAs FETs made by a similar process. **Figure 6** shows the Arrhenius plot of the estimated MTTF. The solid line shows the test results of the similar devices and their extrapolation and indicates the expected upper bound of the MTTF. The dotted line shows the MTTF extrapolated from an MTTF of 9600 hours at T_{ch} = 220°C and indicates the lower bound. The estimated MTTF is at least 6.6×10^5 hours at T_{ch} = 175°C. The wafer process and assembly lines for these high-power FETs are basically the same as those used for space-application devices, hence their high reliability.

3. SAW filters

We have developed several excellent, small-size, low-loss RF-band SAW filters that are suitable for IMT-2000. In general, SAW filters have several superior features compared to dielectric filters and multi-layer LC filters: that is, they are small and have a steep skirt. IMT-2000 cellular phone systems need band-pass filters that operate around 2 GHz and have a wide bandwidth of 60 MHz and low-loss. In order to satisfy these IMT-2000 specifications, we enhanced our original design of ladder type SAW filters to realize the high-frequency and low-loss requirements.

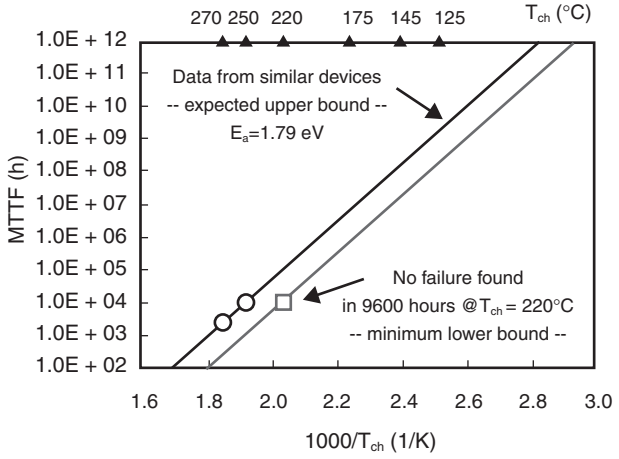

Figure 6
Estimated MTTF versus T_{ch}.

3.1 Design

Figure 7 shows the nominal structure of the ladder type SAW filters we developed.[3] Two kinds of one-port SAW resonators having slightly different resonance frequencies (a series-arm SAW resonator and a shunt-arm SAW resonator) are connected in a ladder structure. Also, several inductance elements (L_1 to L_3) are embedded in a small ceramic package so that the rejection band level can be adjusted. Compared to conventional SAW filter designs, this design has many advantages, for example, lower loss, wider bandwidth, and better high-power durability.

The following technologies were developed for high-frequency operation.

1) For impedance matching at the input and output ports, the capacitances of the series resonators (Cos) and shunt resonators (Cop) are designed to roughly satisfy the following relationship:

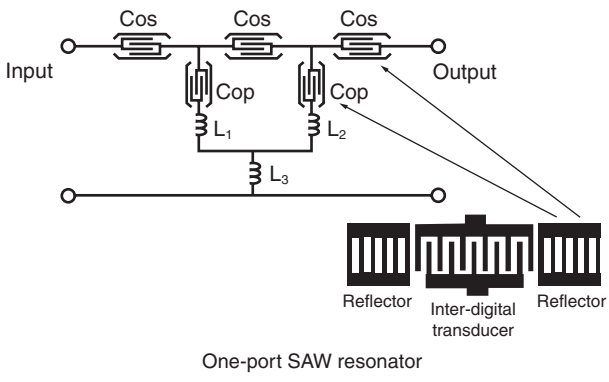

Figure 7
Ladder type SAW filter.

$$Cos \cdot Cop = 1/(2\pi\ fo \cdot R)^2 \quad (1),$$

where fo is the center frequency and R is the line impedance.

2) To delineate fine inter-digital transducers with a 0.5 µm rule, we developed a fine pattern process with a high production yield and reproducibility by using an i-line stepper and reactive ion etching.

3.2 Characteristics

Figure 8 shows the S_{21} characteristics of a Tx inter-stage filter with a pass band of 1920 to 1980 MHz and a rejection band of 2110 to 2170 MHz. The insertion loss in the pass band is less than 2.5 dB, and the attenuation of the rejection band is higher than 35 dB. Figure 8 also shows the S_{21} characteristics of an Rx inter-stage filter with a pass band of 2110 to 2170 MHz and a rejection band of 1920 to 1980 MHz. The insertion loss of this filter in the pass band is less than 3 dB, and the attenuation in the rejection band is higher than 30 dB.

These filters are mounted in a small 2.5 × 2.0 × 1.0 mm ceramic package (**Figure 9**). Compared with current dielectric filters of the same specifications, these Tx and Rx SAW filters take up less than 1/10 the volume and have insertion losses that are 1 dB lower. These characteristics make these new filters suitable for use in IMT-2000 handsets.

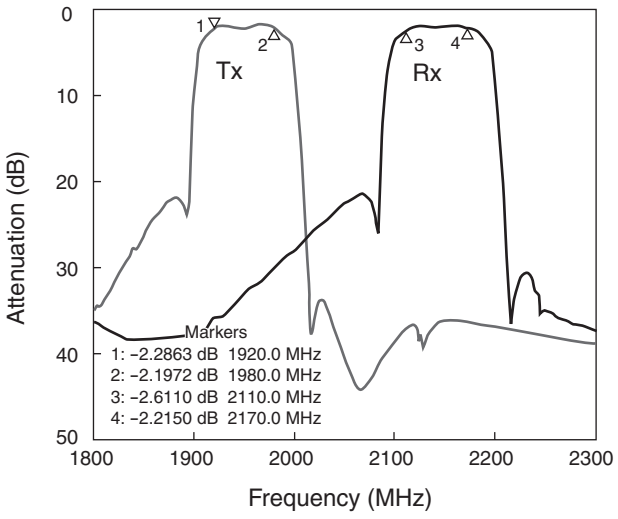

Figure 8
S_{21} characteristics of IMT-2000 filters.

4. Baseband devices

This section describes three LSI chips we have developed for baseband functions in IMT-2000: an analog front end LSI, a signal processing LSI, and a controller LSI. These devices perform all of the functions needed in an IMT-2000 system.

4.1 Analog front end

In this section, we introduce a new analog front end (AFE) LSI for handsets (**Table 1**). This new LSI can reduce the total area and cost because it integrates the modem analog front end and audio circuits.

4.1.1 AFE structure

Figure 10 shows the block diagram of the AFE LSI. The LSI (**Figure 11**) consists of a Tx block, an Rx block, an AIU (Audio Interface Unit), a TCXO control block, a system clock generator, and monitor ADCs.

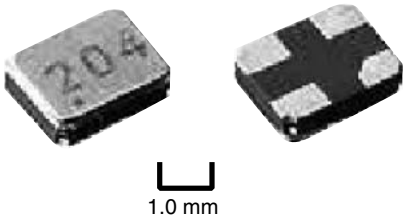

Figure 9
SAW filters mounted in 2.5 × 2 mm packages.

Table 1
Abstract of AFE LSI.

	AFE LSI
Technology	0.25 µm double-polysilicon CMOS
Package	FBGA144

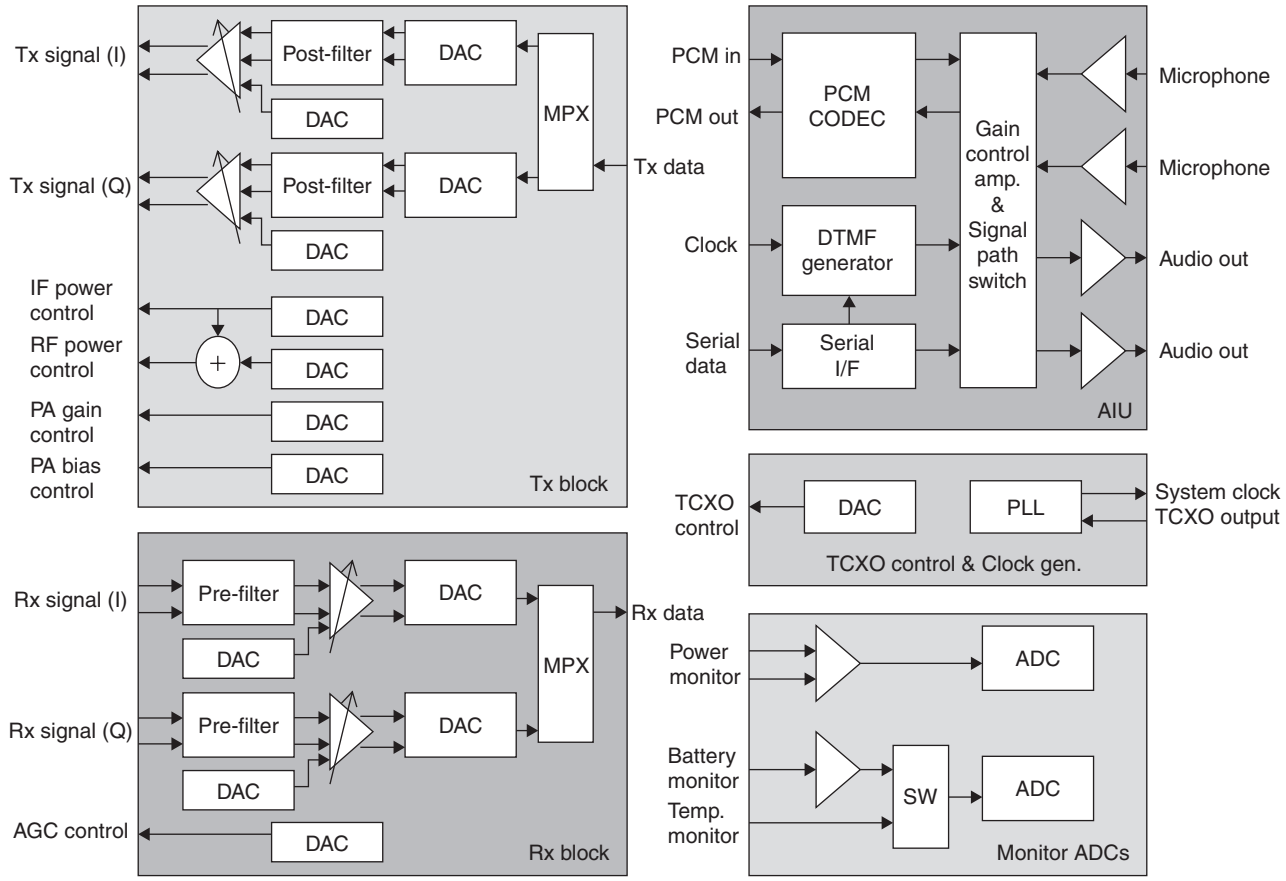

Figure 10
Block diagram of AFE LSI.

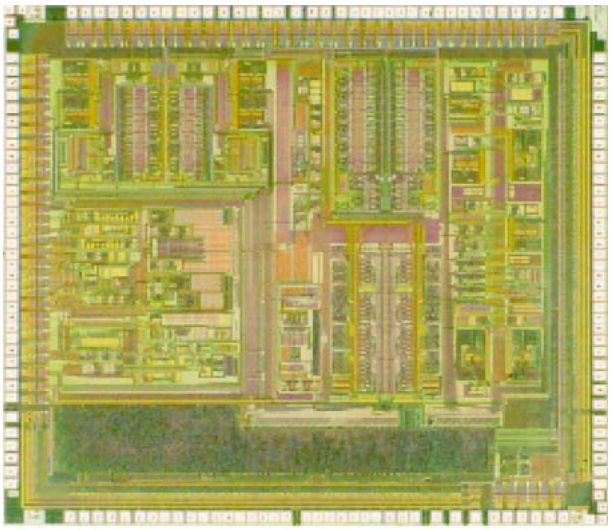

Figure 11
AFE LSI.

1) Tx block: The DACs generate differential transmit I/Q signals from the digital data from the signal processing LSI. The I/Q signals go through post-filters (LPFs), and their magnification balance is adjusted by electronic gain control amplifiers for output to the RF LSI. The offset voltage of the Tx output is adjusted by setting the control register with the DAC outputs. The Tx block also includes other DACs for IF/RF power control, offset of the RF power control signal, and RF power amp gain/bias control.
2) Rx block: The differential I/Q signals of the Rx input from the RF LSI go through pre-filters (LPFs), and their I/Q magnification balance is adjusted by electronic gain control amplifiers. The offset voltage of the I/Q signals is adjusted by setting the control reg-

ister with the DAC outputs. The ADCs convert the received I/Q signals and send digital data to the signal processing LSI. The Rx block also includes a DAC that generates the Rx AGC voltage as directed by the signal processing LSI.

3) AIU: The AIU (Audio Interface Unit) contains a PCM CODEC, two microphone amplifiers, two audio output amplifiers, a DTMF generator, and gain control amplifiers. The DTMF generator is used to generate utility tone. The signal path switch and gain control amplifiers are controlled by a digital input from a serial interface.
4) TCXO control: The AFE LSI has a DAC for TCXO frequency control.
5) System clock generator: The TCXO output clock is input to a PLL block through a buffer amplifier, and the PLL generates a system clock for the signal processing LSI and controller LSI.
6) Monitor ADCs: The AFE LSI has two 8-bit ADCs. The ADCs are used for battery voltage/temperature monitoring and power monitoring.

4.1.2 Circuit design

We used some new circuit design techniques for the components of the AFE LSI.

1) Low-pass filters: The low-pass filters for an IMT-2000 AFE need to be continuous filters because of their high cutoff frequency. The specified cutoff frequency for the Tx and Rx filters is 4.4 MHz and 1.95 MHz, respectively. Generally, to reduce power consumption, continuous high-cutoff-frequency filters are made using Gm-C type filters.
   However, the Gm-C type filter has a narrow dynamic range, which makes it unsuitable for a wide dynamic range system like IMT-2000. Therefore, we developed a new operational amplifier to achieve a wide dynamic range using an RC filter. The power consumption of the operational amplifier was made comparable to that of the amplifier of a Gm-C type filter, which is below 300 µA.
   Because the cutoff frequency of continuous filters varies slightly from filter to filter, we added an automatic cutoff frequency tuning circuit that locks the cutoff frequency to within ±12% of the correct value. The circuit achieves this within 5 ms after switch-on.
2) Tx I/Q DAC: This is a 15.36 Msps DAC optimized for low power consumption. The DAC is a current steering type with a differential output and consumes only 1 mA per channel.
3) Rx I/Q ADC: This is a 15.36 Msps ADC with a pipeline structure. It consumes only 2 mA per channel thanks to the use of a new operational amplifier that is optimized for low power consumption.
4) PLL: The PLL generates a system clock of about 60 MHz from the 13 MHz TCXO output, which means that the multiplier rate is as high as 1536. Therefore, each component of the PLL (phase detector, charge pump, and VCO) must be highly accurate to meet the system's jitter requirements. We achieved a low phase jitter by reducing the noise coupling between the analog and digital parts.

4.1.3 Performance

Figure 12 shows the combined frequency response of the Tx filter and DAC as measured after automatic tuning. The measured cutoff frequency at 3 dB below the DC gain is 4.4 MHz.

Figure 13 shows the measured integrated non-linearity (INL) of the Tx path through the Tx DAC, LPF, and electrical gain control amplifier. The INL is almost within ±1 LSB of the Tx DAC, which is sufficient for system requirements.

Figure 14 shows the measured INL of the Rx path through the gain control amplifier, LPF, and Rx ADC. The INL is almost within ±1 LSB of the Rx ADC, which is sufficient for system requirements.

We measured the phase jitter of the system

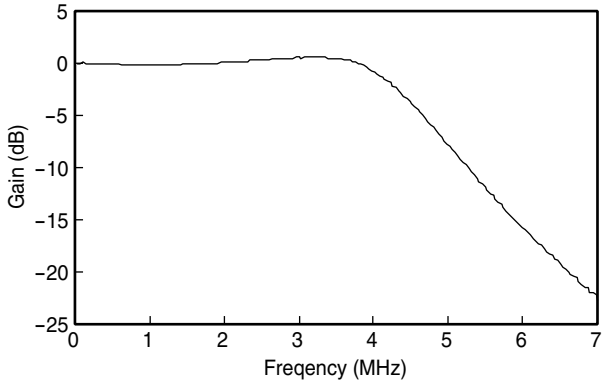

Figure 12
Frequency response of Tx filter.

clock generated from the PLL to be less than 1.0 radian.

4.1.4 System application

The AFE is used in an IMT-2000 handset in combination with an RF, signal processing, and controller LSI. **Figure 15** shows the block diagram of a super heterodyne RF LSI. A DAC in the AFE generates a TCXO control voltage according to an output from the signal processing LSI. The TCXO output frequency is used as a reference frequency for the RF synthesizer. It is also used by the PLL in the AFE to generate a system clock for the signal processing LSI.

Tx I/Q data is converted to a differential analog signal by built-in I/Q DACs, LPFs, and gain amplifiers. The Tx signal is supplied to the I/Q modulator to generate the IF signal. The IF/RF power and power amplifier bias are controlled by a voltage generated by DACs in the AFE according to outputs from the signal processing LSI.

Rx AGC is achieved by controlling the IF amplifier gain using a voltage generated by a DAC in the AFE according to an output from the signal processing LSI. The baseband signal from the I/Q demodulator is converted to Rx I/O data by built-in LPFs, gain amplifiers, and I/Q ADCs.

4.2 Digital baseband device

In this section, we describe a new signal processing LSI (**Figure 16**) and controller LSI

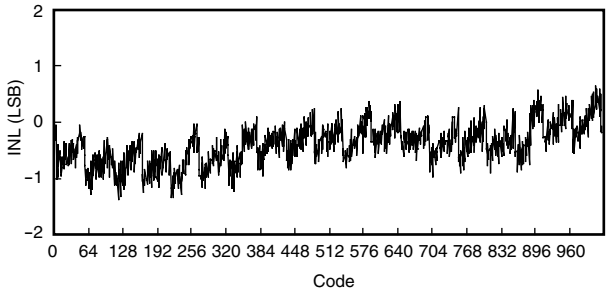

Figure 13
Measured Tx INL.

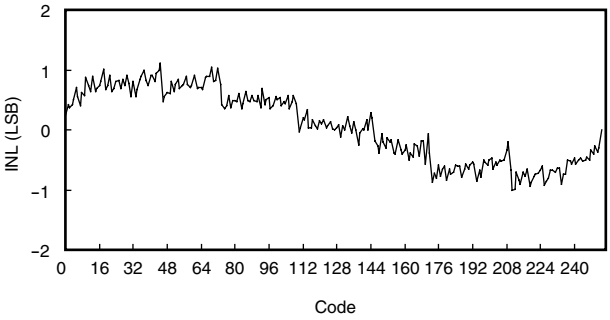

Figure 14
Measured Rx INL.

(**Figure 17**) we have developed. These devices feature low-power hardware, firmware, and software to achieve low-power operation and a low-leakage waiting mode. **Table 2** gives an overview of these two LSIs.

Our baseband chip-set has functions that can be categorized into three types: hardware engines, DSP firmware, and microprocessor firmware. These three types are arranged to form a hierarchy of optimized functional structures to achieve the performance needed for real-time processing of wireless communication.

4.2.1 Key features

These LSIs were developed to achieve all of the signal processing and control functions that are required in the lower protocol layers; that is, the physical layer (Layer 1) and the data link layer (Layer 2).

The hardware operates at low power and has a low leakage waiting mode. The low-power tech-

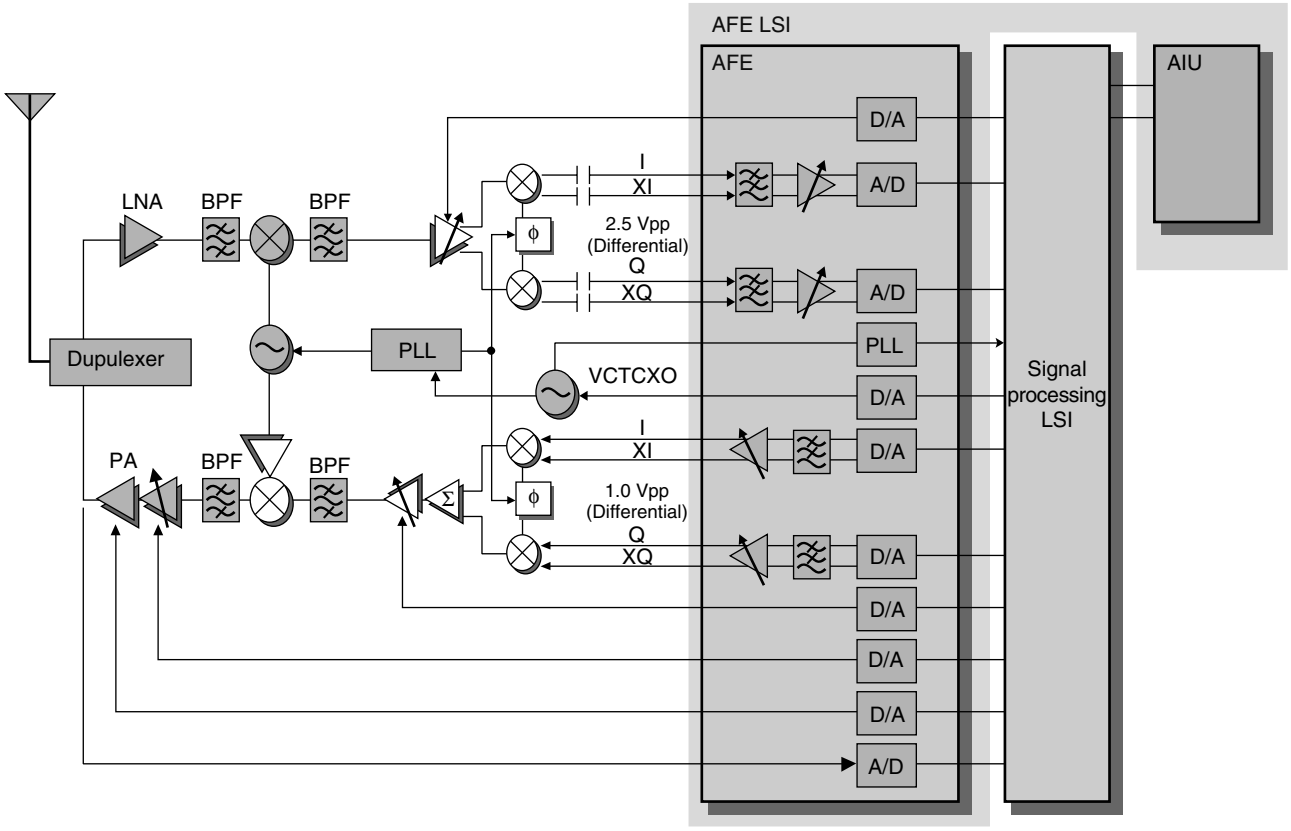

Figure 15
Block diagram of RF block with AFE.

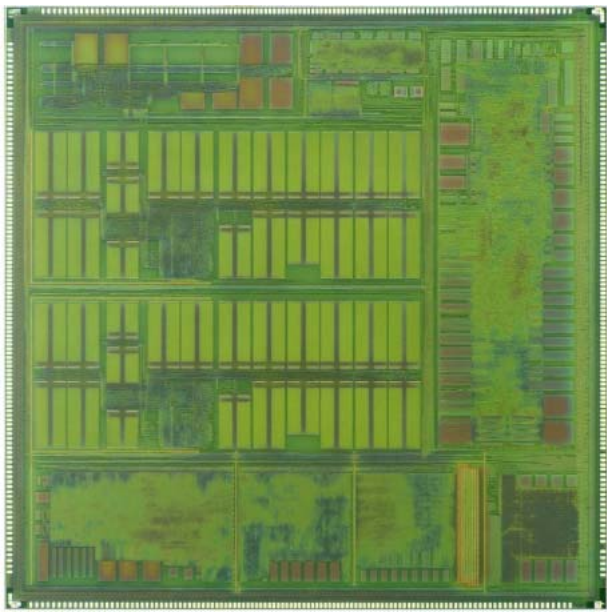

Figure 16
Signal processing LSI.

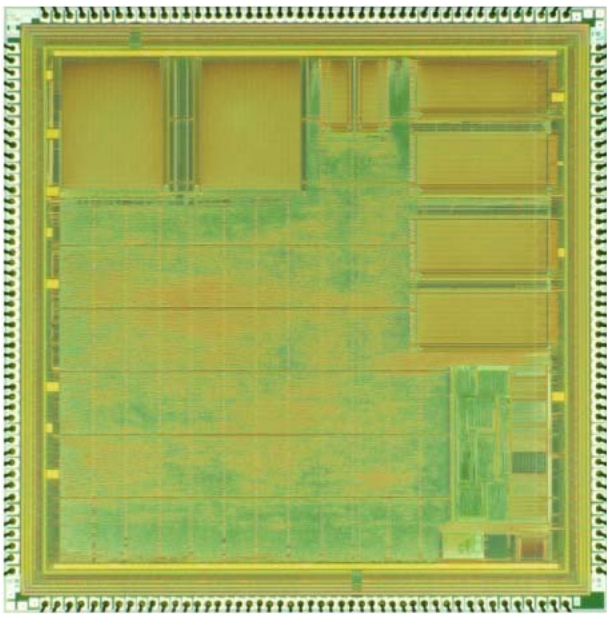

Figure 17
Controller LSI.

nology that was used to achieve this is described below.

The firmware of the DSP controls the hardware engines in real time. It operates during a data slot of about 660 µs. This DSP-based architecture provides flexibility for easy enhancement of specifications in the future.

The software of the control LSI's microprocessor parses commands for Layer 2, translates the commands to obtain the parameters for the DSP control sequences, and reports the results of the hardware engine's operation to Layer 2.

Table 2
Overview of signal processing and controller LSIs.

	Signal processing LSI	Controller LSI
Technology	0.18 µm CMOS	0.25 µm CMOS
Package	FBGA480	FBGA240

4.2.2 Functionality

On this SoC, we have implemented all of the required baseband functions, for example, the MODEM, channel CODEC, intermittent function, and external interfaces (e.g., for multimedia devices and USB) (**Figure 18**).

1) MODEM

The MODEM contains a 16-bit fixed point Fujitsu-proprietary DSP. The main functions of the MODEM are controlled by the DSP firmware and are as follows:

- Cell searching
- Path searching
- Demodulation/de-spreading
- Modulation.

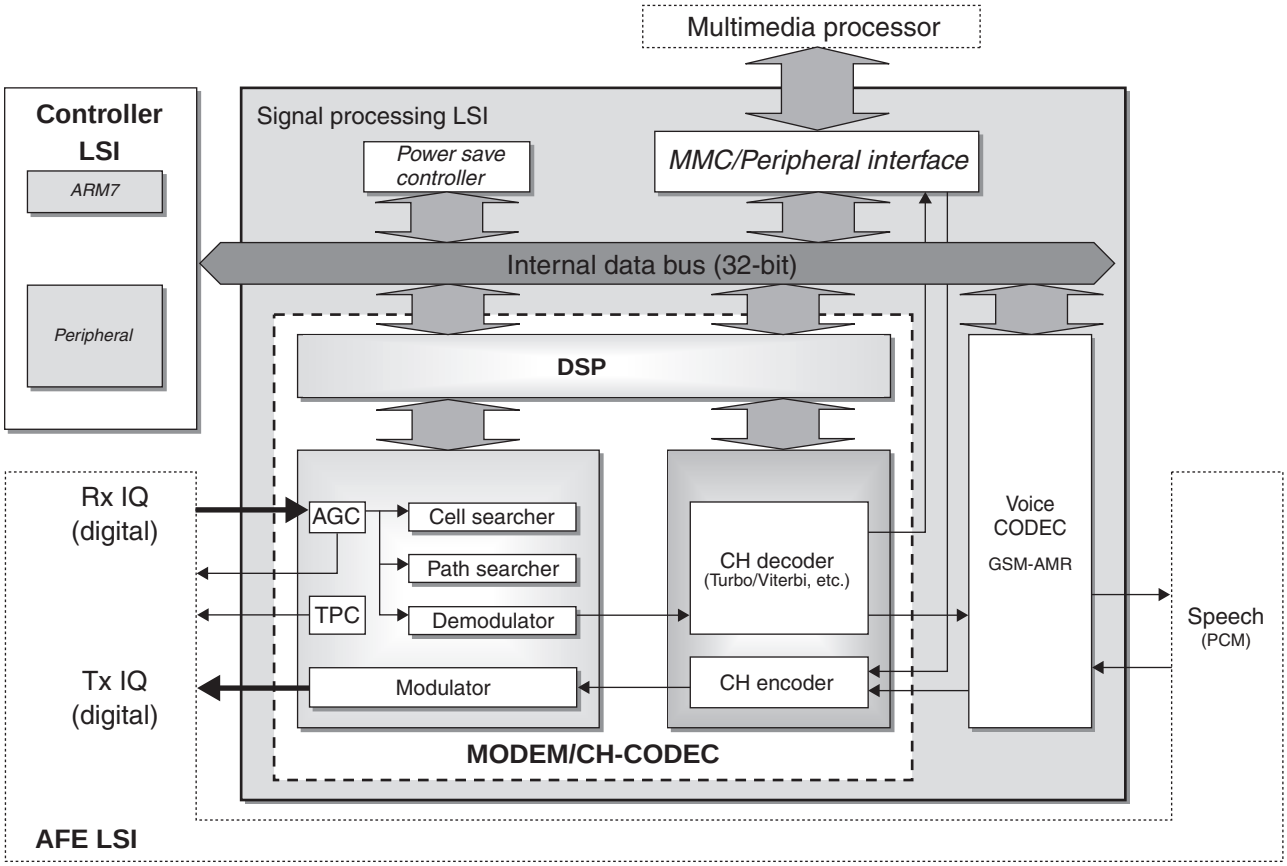

Figure 18
Block diagram of signal processing LSI.

2) Channel CODEC (CH-CODEC)

The CH-CODEC contains a 16-bit fixed point DSP. The main functions of this block are as follows:

– Rate matching
– Convolution encoding/Viterbi decoding
– Turbo encoding/decoding
– Interleaving/de-interleaving.

4.2.3 Low-power hardware technology

Low-power technology is the key for achieving a long operating time and standby time. We will now describe the hardware architecture and methodology for building a low-power device.

A gated clock and clock tree are used in the signal processing LSI to optimize the operation current. Also, a power supply control architecture is used to reduce the standby current.

1) Power supply control

To reduce the standby current, which is mainly transistor leakage current, we used a power supply control architecture to cut off the power supply from inoperative blocks in standby mode (**Figure 19**).

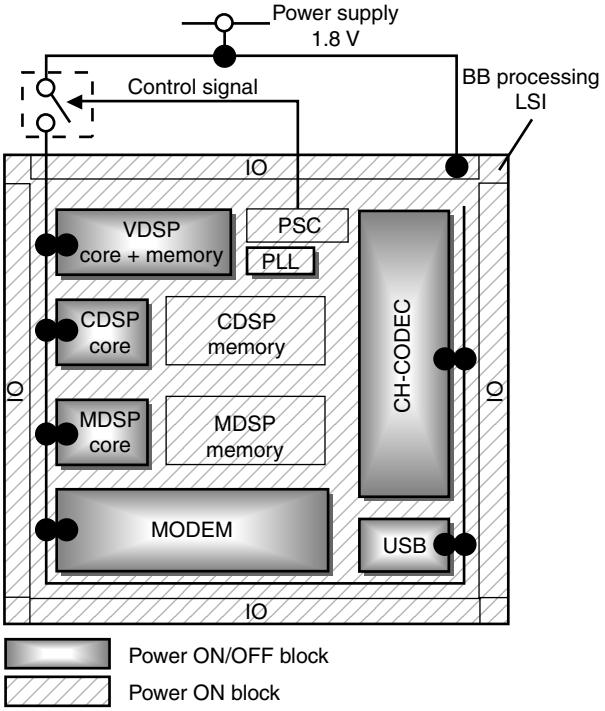

Figure 19
Power supply control architecture.

2) Gated clock

Two methods are used for inserting the gated clock.

One method is to remove the clock for each functional block when the block does not need to operate. This method eliminates the unnecessary power consumption caused by clock propagation in the block.

The other method is to insert a gated clock cell using control parameters optimized by a synthesis tool. The tool automatically chooses the appropriate net into which the gated clock cell is to be inserted (**Figure 20**).

3) Optimized clock tree

To reduce the clock tree power, we optimized the block separation to shorten the length of the clock line. We also optimized the clock buffer to minimize the power consumption in the clock line (**Figure 21**).

5. Mobile multimedia platform

In this section, we describe Fujitsu's activity in the Mobile Multimedia Platform (MMP), which contains dedicated hardware for delivering high-quality and high-performance AV codecs, graphics, JPEGs, and so on within a software framework (device drivers, OS, media libraries, basic applications, etc.).

Fujitsu aims to deliver the MMP as a de facto standard platform for multimedia applications for various mobile equipment, including 2.5G/3G digital cellular phones, PDAs, automotive equipment, and other kinds of consumer AV products. The MMP is based on an ARM926EJ-S CPU framework and delivers a uniquely specified, extremely low power operation scheme, including sophisticated clock distribution control and a dynamic clock gear up/down scheme.

We have already developed the first LSI product with the MMP architecture. **Figure 22** shows the block diagram of the new LSI, which is called the ARMEGA. The technological features of the ARMEGA include a 2D/3D graphics accelerator.

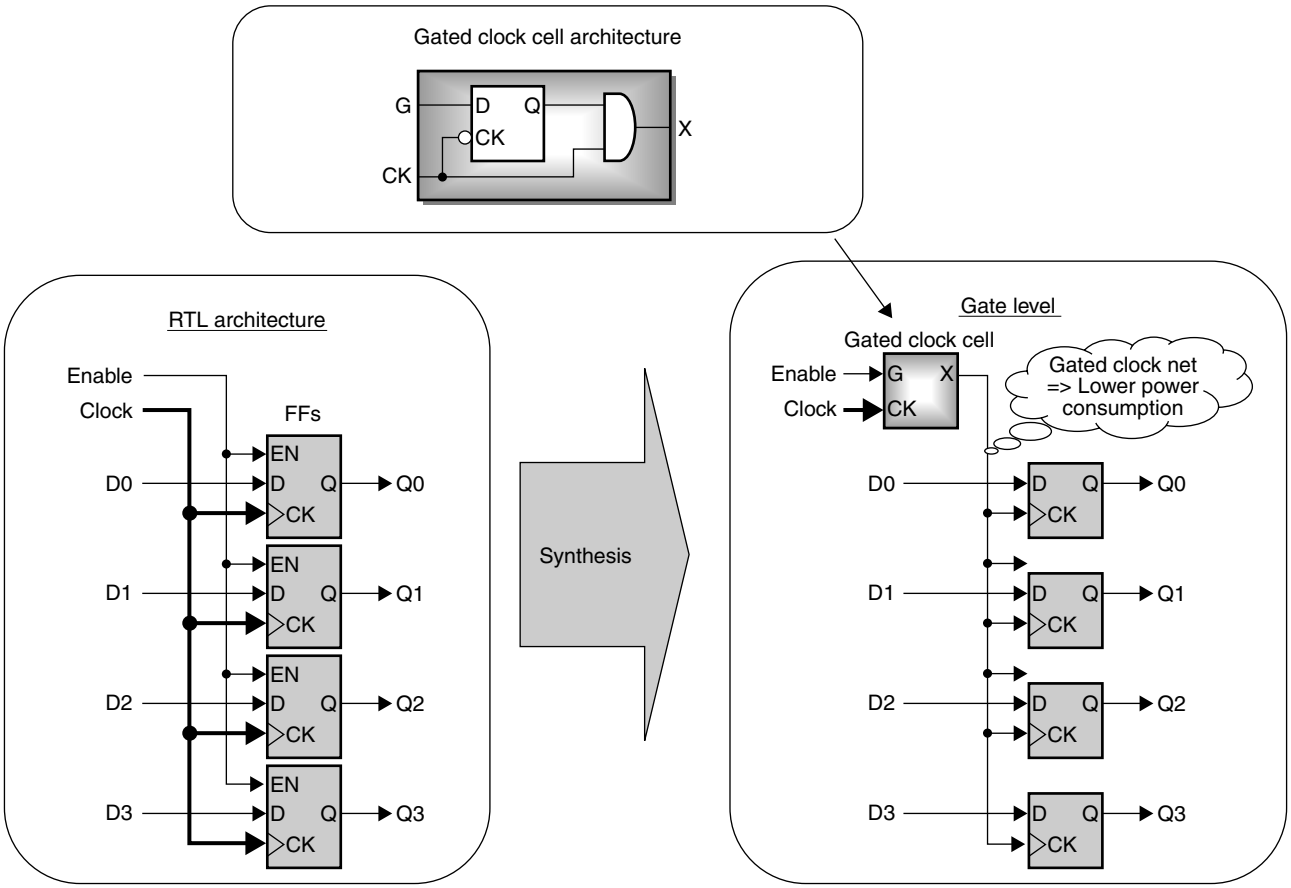

Figure 20
Gated clock.

In addition, we have developed an MPEG4 video codec that will be included in a future MMP based on the ARMEGA. These two key functional units are described in the next two sections.

5.1 MPEG4 video codec

Fujitsu has developed the world's lowest power dissipation MPEG4 video codec core that is capable of QCIF 15 fps full-duplex codec operation.[4] The new device consumes only 9 mW, and this extremely low power operation was realized by adopting dedicated hardware for scene-adaptive motion vector searching. Because of this hardware, the computational load was reduced to 1/20 of the load in a 4:1 sub-sampling algorithm, which is the type used in most existing hardware products. **Table 3** gives an overview of an LSI that implements the MPEG4 video codec core (this core is nicknamed OWEN). The die photo of this LSI is shown in **Figure 23**.

5.2 2D/3D graphics accelerator

We have developed a high-performance graphics accelerator that can execute most Java programs 30 to 50 times faster than a fully software-implemented equivalent running on an ordinary CPU.

The consistent high performance and low power consumption of this graphics accelerator has been achieved through 10 year's of experience with graphics and automotive navigation systems and by eliminating unnecessary sections from our previous 3D graphics controller LSIs and reconfiguring their rendering and display management. **Table 4** gives an overview of the core of this graphics accelerator.

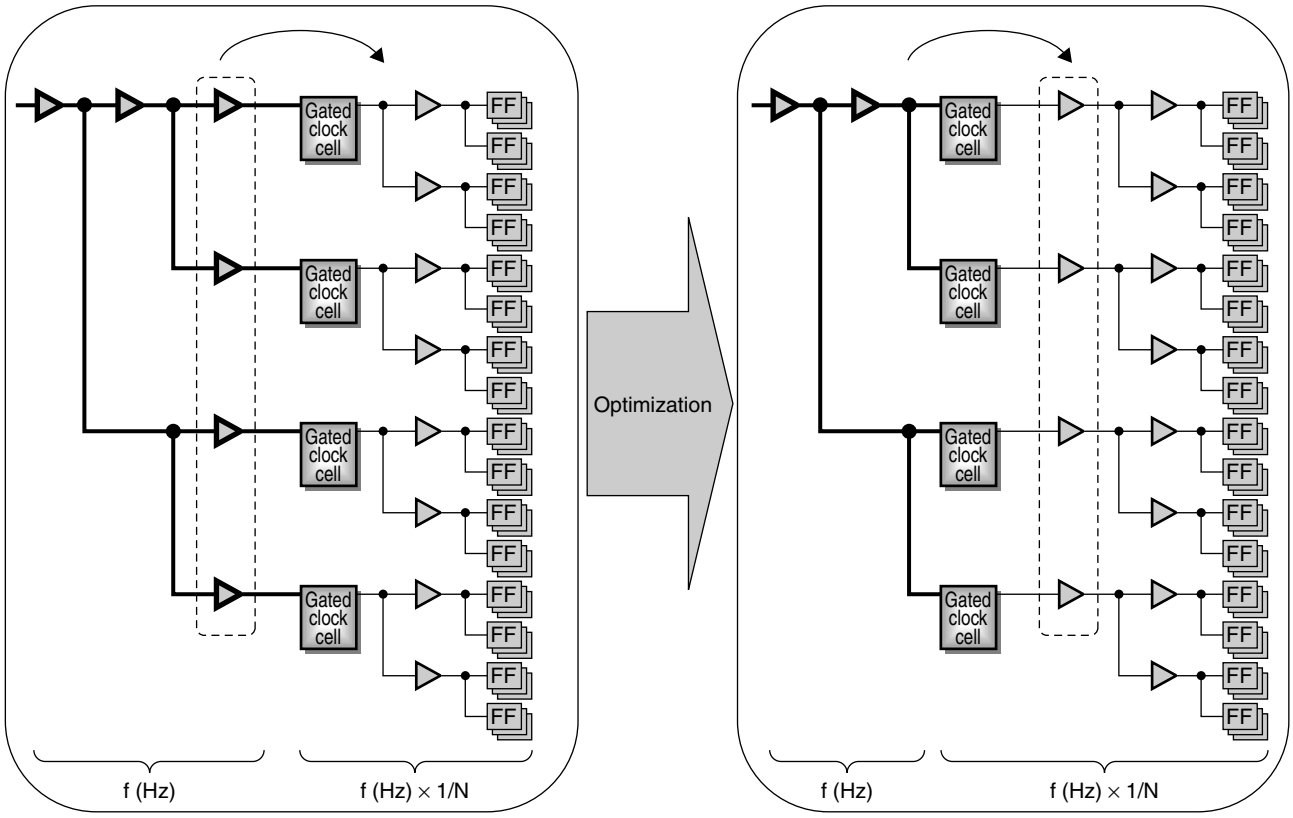

Figure 21
Clock tree optimization.

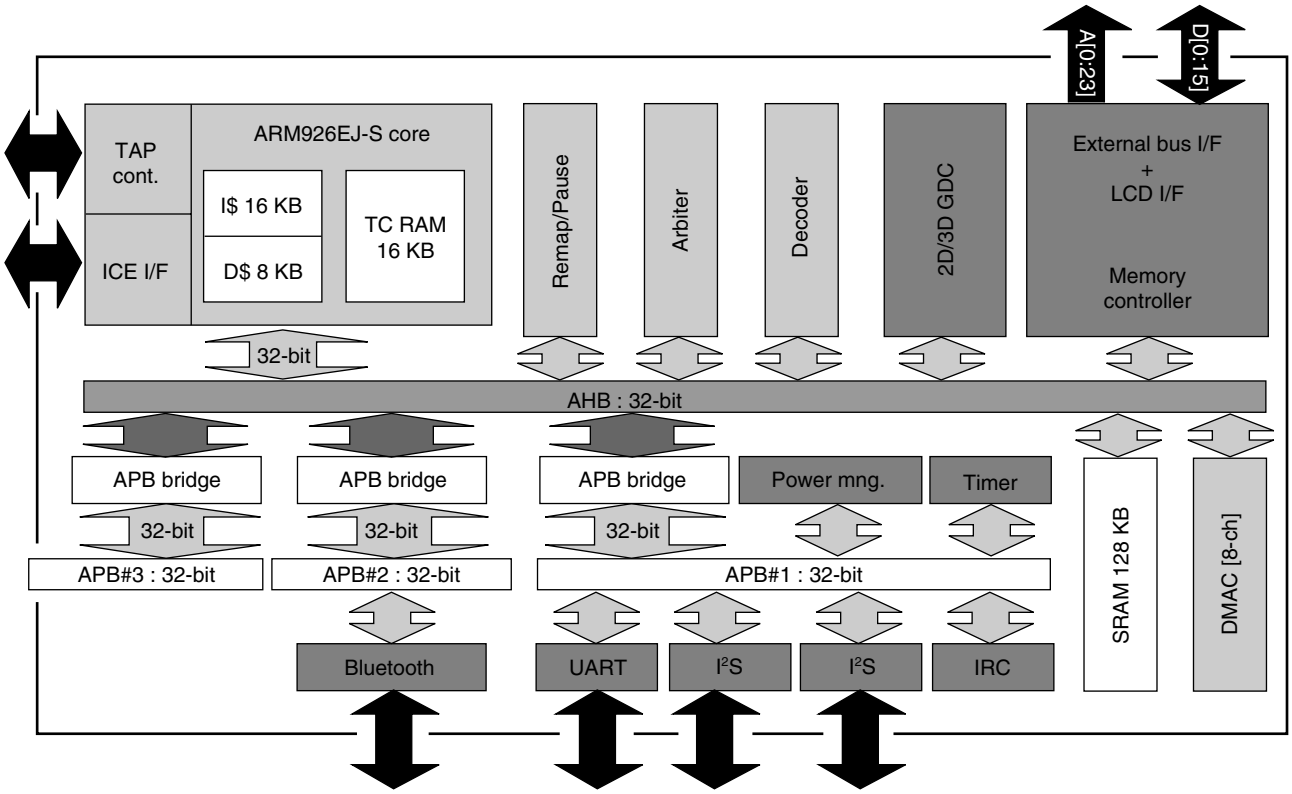

Figure 22
ARMEGA block diagram.

Table 3
Overview of MPEG4 video codec LSI.

	MPEG4 video codec LSI
Technology	0.18 µm CMOS
Package	HQFP208

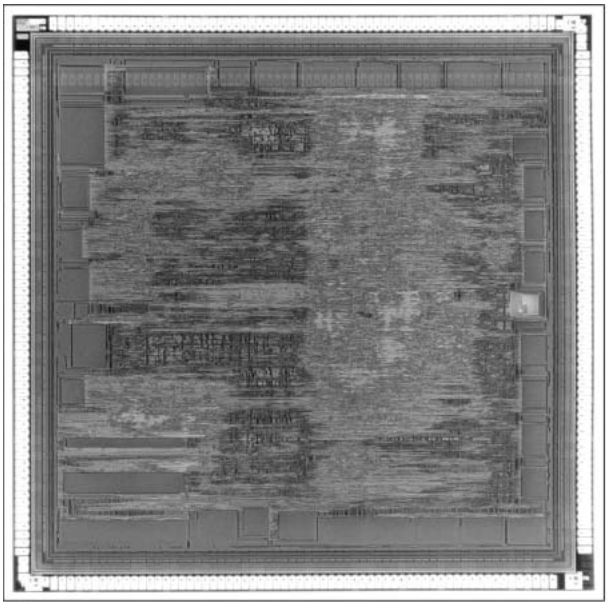

Figure 23
Die photo of MPEG4 video codec LSI.

5.3 Software

Bluetooth protocol stacks and 2D/3D graphics device driver software are already supported for ARMEGA. We also plan to deliver the following software modules:

- An Internet browser,
- streaming protocol,
- network communication protocol,
- SSL/TSL,
- video/audio CODEC,
- speech recognition/voice synthesis,
- TV conferencing,
- mail,
- still pictures, and
- RTOS.

By delivering these software modules, we will be able to flexibly support a wide range of customer requirements.

Table 4
Overview of 2D/3D graphics accelerator core.

Performance	85 M pixels/s
Resolution	352 × 288 (CIF)
Layers	2
Power	15 mW @1.5 V, 33 MHz
Host I/F	AHB (rev 2.0)
Display Color opt.	8 to 24 bits/pixel
2D rendering	Dot, line, bold line, etc.
3D rendering	Shading, texture
Special effects	Pixel alpha blending
HW cursor	16 × 16

6. Conclusion

We have developed new, high-power GaAs FETs, small-volume SAW filters, and low-power baseband devices. We have also developed a mobile multimedia platform using these advanced devices. These devices will enable customers to develop extremely small, long standby-time and long talk-time handsets with various multimedia functions for the IMT-2000 system.

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