Quantitative Ultra Shallow Dopant Profile Measurement by Scanning Capacitance Microscope

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This paper compares scanning capacitance microscope (SCM) signals of an n-MOS transistor implanted with arsenic ions at an energy as low as 5 keV with a vertical secondary ion mass spectroscopy (SIMS) profile of the same device. Then, it describes SCM measurement by the application of a DC voltage sufficient to compensate for the flat band shift caused by the interaction between the probe of a conductive scanning probe microscope (SPM) and a silicon surface. To acquire the exact impurity distribution beneath a silicon surface, the SIMS measurement was carried out at a primary ion energy of less than 1 keV. As a result, the calibration of SCM signals using SIMS data was accomplished in the ultra shallow region near the silicon surface. It was also confirmed that the formalism based on the depletion approximation applies in this region. Using this formalism, we show that, at concentrations around 10^{18} cm^{-3}, SCM enables quantitative two-dimensional dopant profiling near the source/drain extension at a resolution of better than 10 nm. Moreover, by optimizing the sample preparation and measurement conditions, it is also possible to analyze a sub-µm gate transistor with a 60 nm channel length and investigate the complex dopant distribution in the source/drain region, including the edge of the shallow trench isolation.

1. Introduction

As the dimensions of devices have shrunk, two-dimensional dopant profiling of advanced silicon transistors has become an important technique for obtaining the required electrical characteristic in devices. As a result, various analytical techniques have been developed to obtain two-dimensional information. The differential etching technique facilitates qualitative evaluation of dopant profiles by a transmission electron microscope (TEM)[1)-3)] and scanning electron microscope (SEM).[4)] However, since it is difficult to control the etching rate, these techniques do not provide quantitative information of two-dimensional profiles. On the other hand, the scanning capacitance microscope (SCM) has been shown to be useful for quantitative two-dimensional dopant profiling, but it is difficult to extract a meaningful two-dimensional dopant profile with a high accuracy from SCM images in the vicinity of p-n junctions. Recently, to resolve this problem, it has been suggested that resolution can be improved by using a silicon semiconductor tip.[5)] Also, the qualitative and quantitative relationship between the applied V_{bias} and the p-n junction location has been investigated.[6)] In advanced complementary metal oxide semiconductor (CMOS) transistors, the fabrication of a shallow source/drain (S/D) extension has been an important technology. For a sub-0.1 µm CMOS device, for example, an S/D extension with a junction of less than 40 nm will be required. In order to perform quantitative analysis by SCM in the vicinity of an S/D extension, calibration by means of an advanced evaluation method with a high accuracy beneath the silicon surface is indispensable.

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We set ourselves the goal of accomplishing quantitative two-dimensional dopant profiling of an advanced CMOS device. At present, advanced SIMS allows us to measure the impurity distribution to a resolution of within a few nm beneath the silicon surface. We therefore calibrated the equipment we used in this work using SIMS data. Based on the work reported in one of our previous papers,[7] we optimized the sample preparation procedure and the measurement conditions of an advanced SCM system. As a result, we can now perform a quantitative evaluation of a two-dimensional dopant profile by means of SCM measurement. In this paper, we describe how we met the goal we set and present some quantitative results for an advanced CMOS transistor.

2. Experimental procedure
2.1 Sample preparation

In order to acquire a two-dimensional dopant profile of a device, the device must be cut cross-wise to expose the region of interest. In general, a cross-sectional sample is prepared by cleaving followed by polishing. The cross-sectional surface of an SCM sample must have a low roughness, no surface damage, and a high cleanliness. Although this procedure resembles the standard technique

(a) Schematic model of SCM measurement

(b) Block diagram of SCM measurement

Figure 1
System for acquiring SCM signals from a cross-sectional sample. The scanning probe tip detects a 100 kHz reference signal. The output (dC/dV) for SCM measurement depends on the variation of silicon capacitance (C_{Si}) due to dopant distribution.

for the cross-sectional preparation of a TEM sample, an additional polishing in colloidal silica solution is required to obtain the required quality for SCM imaging. Additionally, to improve the reproducibility of SCM results to be used for quantitative analysis, the surface should be coated with native oxide to eliminate the non-uniform charge distribution that remains after polishing. In the present work, the finishing process for cross-sectional samples consisted of heat treatment under UV irradiation on a hot plate as described by Zavyalov et al.[8]

2.2 Measurement

An atomic force microscope is used to position a nanometer scale tip on the silicon surface, and the local capacitance change is measured as a function of the applied voltage V. We used a commercial SCM instrument (Digital Instruments Dimension 3100 atomic force microscope) to obtain the images presented in this paper. **Figures 1 (a)** and **(b)** show a schematic model and the block diagram of the system for acquiring SCM signals from a cross-sectional sample.

SCM measurement is done in constant voltage-change (constant dV) mode by applying a 100 kHz AC voltage of about 1 V to the sample. The SCM consists of a contact-mode atomic force microscope with a circuit tuned to about 915 MHz coupled to the tip-sample capacitance. The system is configured to measure dC/dV, which depends on the variation of silicon capacitance (C_{Si}) due to dopant distribution. In general, when the probe of a conductive scanning probe microscope (SPM) contacts a silicon surface through an insulating layer, a flat-band offset occurs because of the movement of carriers from the insulating layer to the conductive SPM probe. Because of this flat-band offset, the magnitude of the SCM signal in the vicinity of the p-n junction does not reflect the carrier density.[9] The flat-band offset can be compensated for by applying a DC offset voltage to the sample. In principle, by applying a DC offset voltage, the change in capacitance due to the accumulation and depletion
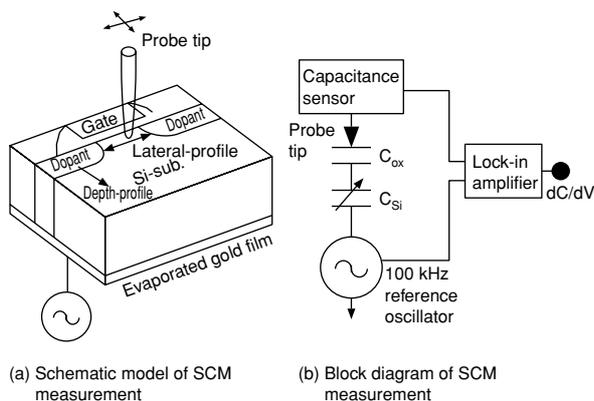
caused by the applied AC voltage can be maximized. However, the magnitude of the SCM signal varies in proportion to this change. Therefore, in the present work, the level of the applied DC voltage is set according to the magnitude of the SCM signal.

This SCM instrument can acquire SCM images in the amplitude mode and the phase mode, which reveals whether the carriers are n type or p type. The Lock-in amplifier used to measure the SCM output operates at the same frequency as the frequency of the applied AC voltage. In the phase mode, the phase of lock-in has to be designated. When the correct phase is selected, whenever there is a change of carrier type, the Lock-in amplifier output changes polarity. In the experiment, the phase is adjusted to around ±90° to obtain the best contrast in the SCM images.

SIMS measures the impurity distribution to a resolution of a few nm beneath the silicon surface. Our calibration of two-dimensional SCM data is based on one-dimensional SIMS data. Therefore, to acquire the exact dopant profile in the ultra shallow region, SIMS measurement is carried out at an energy below 1 keV.

3. Results and discussion

3.1 Two-dimensional SCM images

Figure 2 shows SCM images of a cross-sectional sample of a gate-like structure at different applied DC voltages. The silicon wafer was implanted with As ions at a dose of 1.0×10^{15} cm^{-2} at an energy as low as 5 keV and subsequently annealed at a temperature above 1000°C. Figure 2 (a) shows the schematic model of a gate-like structure, and Figures 2 (b) to (f) show SCM images of this sample at five different DC voltages.

The highest contrast of n-type carriers in the implanted region is acquired at an applied DC voltage of –0.5 V (Figure 2 (c)). Therefore, we used the SCM image at this DC voltage to determine the amount of two-dimensional concentration beneath the silicon surface. To determine the location of the p-n junction, the DC voltage must be carefully adjusted, because the carrier density in the measured region is not uniform and therefore the measured position of the p-n junction changes.

(a) Schematic model   (b) DC = –1.0 V   (c) DC = –0.5 V

(d) DC = 0 V   (e) DC = 0.5 V   (f) DC = 1.0 V

0.1 µm
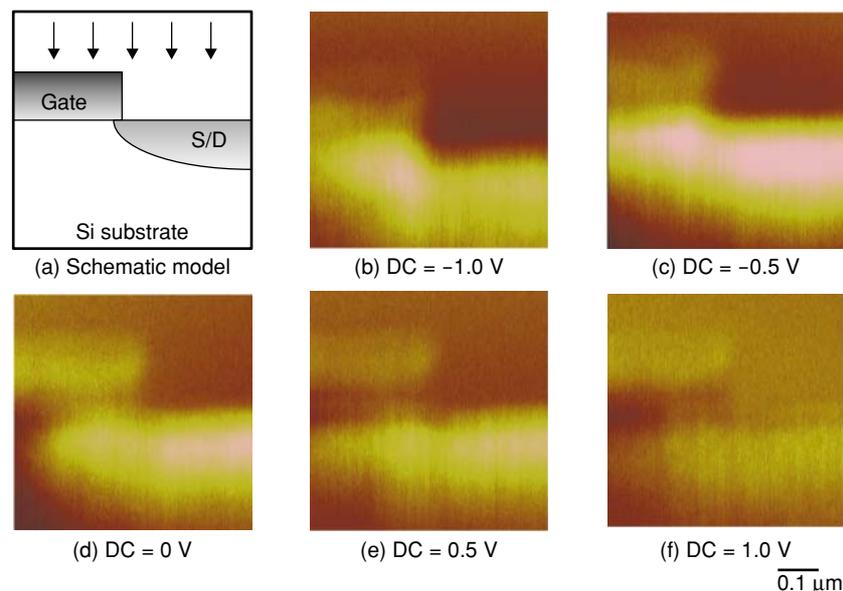
Figure 2
SCM images of a gate-like structure at different DC voltages. Figure 2 (a) shows a schematic model of the structure. Figures 2 (b) to (f) show the SCM images. These images were acquired at an applied AC voltage of 0.5 V in the phase mode. The lock-in phase was 85°. The brighter areas are mainly due to n-type carriers, and the darker areas are mainly due to p-type carriers.

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3.2 Calibration

The doping concentration (N_a) using the depletion approximation[10] is as follows:

$$N_a = N_0\left(\frac{C_{OX}}{\Delta C} - 1\right)^2, \tag{1}$$

where N_0, C_{OX}, and ΔC are, respectively, the proportional constant, oxide capacitance, and total capacitance change, which can be determined from the SCM data. Therefore, if we use SIMS data to determine N_a and SCM data to determine ΔC, we can determine N_0 and C_{OX}. **Figure 3** shows a comparison between one-dimensional SIMS and SCM depth profiles. The relationship in Equation (1) seems to be correct in the region below 50 nm, and the depth resolution is better than 10 nm. Diebolt et al.[11] showed that the maximum depletion width (Wmax) is approximately 2 nm at a concentration of 10^{20} cm^{-3}. Additionally, the doping concentration rapidly decreases in the deep region beyond 40 nm, as shown by the SIMS profile in Figure 3. For these reasons, we believe that we have achieved a spatial resolution of better than 10 nm without an edge effect at the silicon substrate edge.

Figure 4 shows the SIMS profile and the dopant depth profile calculated from Equation (1) using the depth profile determined from SCM data. The measured and calculated doping concentrations (N_a) show excellent agreement at around 10^{18} cm^{-3}, but do not agree above a concentration of 10^{20} cm^{-3}. However, this disagreement is appropriate in principle because ions in silicon at concentrations above 10^{20} cm^{-3} are mostly electrically inactive.[12] It is considered that the contact area of an SPM probe with a diameter larger than 10 nm extends beyond the silicon surface. This reduces the SCM signal amplitude, which causes the carrier density to be overestimated. In order to avoid this problem, it is desirable to acquire SCM signals using a conductive SPM probe with a smaller diameter.

Therefore, we concluded that quantitative two-dimensional dopant profiling is possible at concentrations around 10^{18} cm^{-3} in this ultra shallow region.

3.3 Quantitative evaluation of two-dimensional dopant profile

Figure 5 (a) shows a cross-sectional SCM image of an n-MOS transistor. The gate electrode is assigned as a mask. To fabricate a high-performance
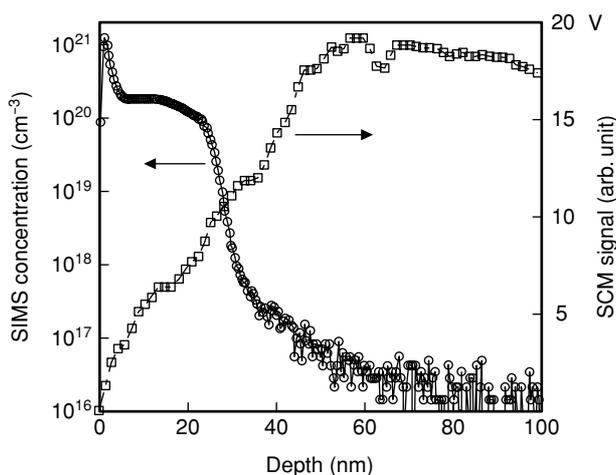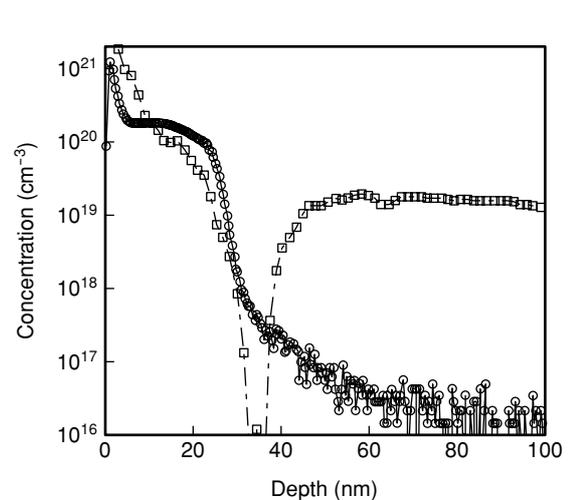

Figure 3
Comparison between SIMS data (○) and SCM (□) signals. The origin of the SCM profile is at the silicon surface. The surface position was determined using an atomic force microscope (AFM).

Figure 4
Comparison between SIMS data (○) and converted SCM signals (□). These SCM signals are derived from SIMS data of the same depth.
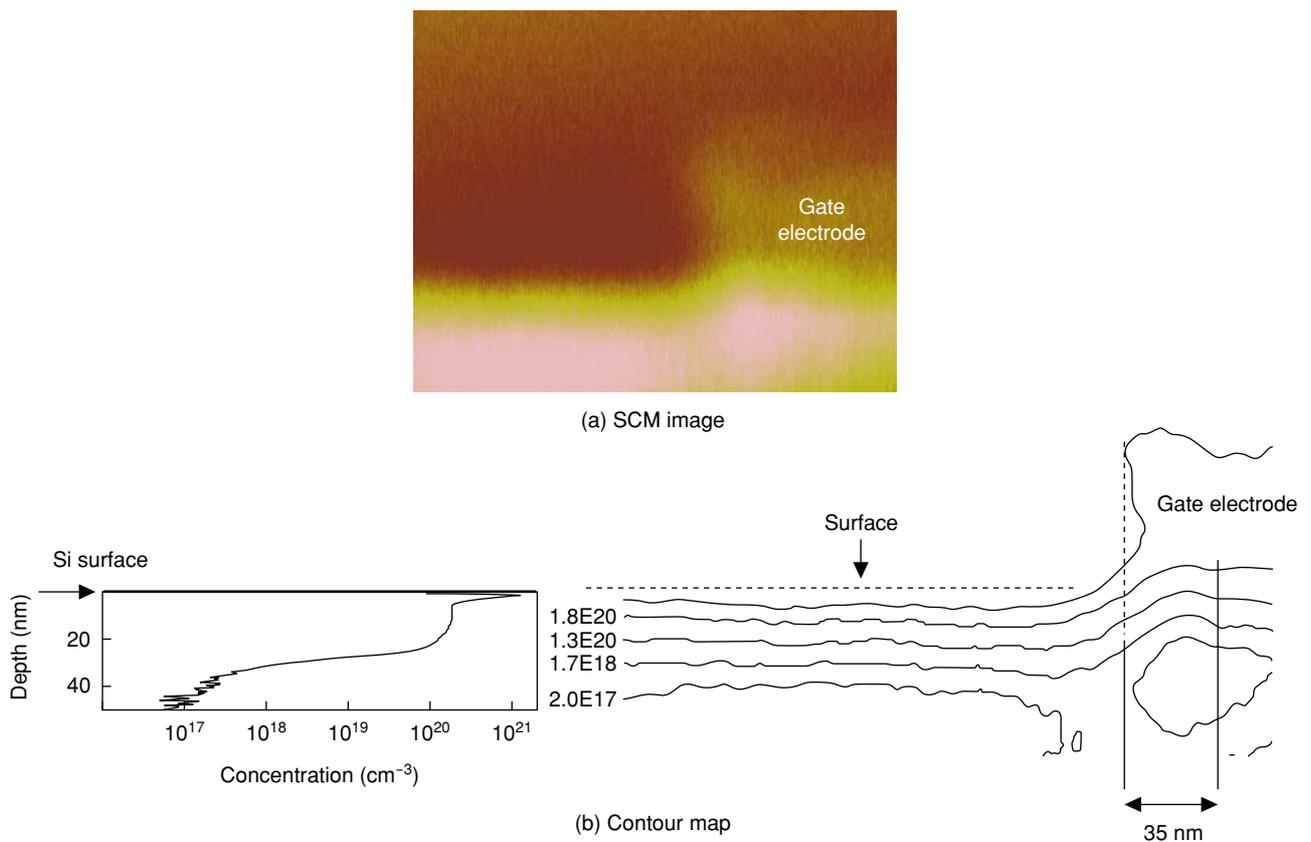
(a) SCM image

(b) Contour map

Figure 5
Quantitative two-dimensional dopant profile. (a) cross-sectional SCM image of an n-MOS transistor. Brighter areas correspond to the n-type regions, while the darker areas correspond to insulating materials. (b) The contours show the concentrations in the vicinity of the gate electrode. The positions of the gate edge and silicon surface were determined using an AFM.

CMOS transistor, the two-dimensional dopant profile beneath this gate electrode, which is called an S/D extension, must be strictly optimized. We obtained approximations for the two-dimensional distribution from the one-dimensional SIMS results, and then we investigated the dopant profile in the vicinity of this gate electrode edge in detail. **Figure 5 (b)** shows contour plots that are based on the SCM data in Figure 5 (a). The dopant concentration in this figure is converted from one-dimensional SIMS data. From these results, even in the two-dimensional case, it is clear that quantitative two-dimensional dopant profiling can be achieved by SCM at a resolution better than 10 nm for concentrations around 10^{18} cm^{-3}. Furthermore, we found that the carrier moves underneath the gate electrode up to a distance of about 35 nm.
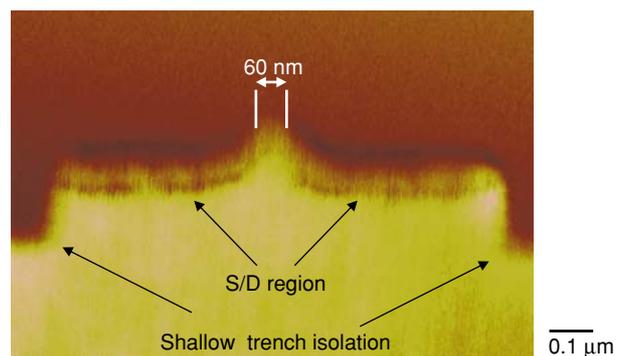

Figure 6
SCM image of advanced CMOS transistor with 60 nm channel length.

3.4 Application to an advanced CMOS transistor

Figure 6 shows the results of applying this

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technology to an advanced CMOS transistor. The figure shows that SCM measurement is sufficient for analyzing the transistors of 0.1 μm-generation devices with a 30 nm channel length. Moreover, the complex structure of the S/D region and the location of the shallow trench isolation are also visible. Therefore, SCM analysis is not only useful for obtaining the quantitative two-dimensional profile of a cross-sectional sample but also for investigating the phenomena of leakage at the interface and at the edge of the shallow trench isolation.

4. Conclusion

In this paper, we have investigated the quantitative analysis of two-dimensional dopant profiles by means of SCM measurement and its application.

The results can be summarized as follows:
1) Direct calibration of SCM signals using SIMS data was accomplished in the ultra shallow region near the silicon surface of a sample with a junction depth of less than 30 nm.
2) The formalism based on the depletion approximation can be used to calibrate SCM signals of this region using SIMS data.
3) At the vicinity of the source/drain extension, quantitative two-dimensional dopant profiling can be achieved by SCM at resolutions better than 10 nm at concentrations around 10^{18} cm^{-3}.
4) By optimizing the sample preparation and the measurement conditions, it is also possible to analyze the transistors of 0.1 μm-generation devices with a 30 nm channel length and investigate the phenomena of leakage at the interface and at the edge of the shallow trench isolation.

We showed that SCM is a powerful tool for quantitative two-dimensional dopant profiling in the ultra shallow region when the experimental conditions are appropriate for SCM measurement.

In the present work, the native oxide is used as an insulating layer between the conductive

SPM tip and the silicon surface. Therefore, in the next step, we should improve the quality of the insulator by depositing an additional oxide after removing the native oxide. We expect that this will make it possible to perform two-dimensional dopant profiling from an SCM signal even below the p-n junction.

References

1) H. Cerva: Two-dimensional delineation of shallow junctions in silicon by selective etching transmission electron microscopy cross-sections. *J. Vac. Sci. Technol.*, **B10**, p.491-495 (1992).
2) C. Spinella, V. Raineri, and S. U. Campisano: Selective Etching of B-Doped Silicon: Mechanisms and Two-Dimensional Delineation of concentration Profiles. *J. Electrochem. Soc.*, **142**, p.1601-1607 (1995).
3) C. Spinella, V. Raineri, M. Saggio, V. Privitera, and S. U. Campisano: Two-Dimensional Profiling by selective etching: the role of implant induced secondary defects. *Nucl. Instrum. Methods*, **B69**, p.139-143 (1995).
4) L. Gong, S. Peterson, L. Frey, and H. Ryssel: Improved delineation technique for two dimensional dopant profiling. *Nucl. Instrum. Methods*, **B69**, p.133-138 (1995).
5) M. L. O'Malley, G. L. Timp, W. Timp, S. V. Moccio, and J. P. Garno: Electrical simulation of scanning capacitance microscopy imaging of the *pn* junction with semiconductor probe tips. *Appl. Phys. Lett.*, **74**, p.3672-3674 (1999).
6) J. J. Kopanski, J. F. Marchiando, and B. G. Rennex: Carrier concentration dependence of the scanning capacitance microscopy signal in the vicinity of p-n junctions. *J. Vac. Sci. Technol.*, **B18**, p.409-413 (2000).
7) Y. Kikuchi, T. Kubo, and M. Kase: Quantitative ultra shallow dopant profile measurement by scanning capacitance microscope. in Proceedings of Microscopy of Semiconducting Materials XII, edited by A. G. Cullis and J. L. Hutchison, 2001, p.519-522.

8) V. V. Zavyalov, J. S. McMurray, and C. C. Williams: Advances in experimental technique for quantitative two-dimensional dopant profiling by scanning capacitance microscopy. *Rev. Sci. Instrum.*, **70**, p.158-164 (1999).

9) H. Edwards, R. McGlothlin, R. S. Martin, Elisa U, M. Gribelyuk, R. Mahaffy, C. K. Shih, R. S. List, and V. A. Ukraintsev: Scanning capacitance spectroscopy: An analytical technique for pn-junction delineation in Si devices. *Appl. Phys. Lett.*, **72**, p.698-700 (1998).

10) A. Erickson, L. Sadwick, G. Neubauer, J. Kopanski, D. Adderton, and M. Rogers: Quantitative Scanning Capacitance Microscope Analysis of Two-Dimensional Dopant Concentrations at Nanoscale Dimensions. *J. Electro. Material*, **25**, p.301-304 (1996).

11) A. C. Diebold, M. R. Kump, J. J. Kopanski, and D. G. Seiler: Characterization of two-dimensional dopant profiles: Status and review. *J. Vac. Sci. Technol.*, **B14**, p.196-201 (1996).

12) M. Ramamoorthy and S. T. Pantelides: Complex Dynamical Phenomena in Heavily Arsenic Doped Silicon. *Phys. Rev. Lett.*, **76**, p.4753-4756 (1996).

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