

Decoupling Capacitor with Low Inductance for High-Frequency Digital Applications

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Because of the rapid progress of LSI technology, the operating frequency of LSIs is increasing and the power supply voltage is decreasing. To use high-performance LSIs effectively, new decoupling capacitors that can suppress the switching noise generated by LSIs and stabilize the supply voltage are required. We have developed a capacitor which can satisfy these requirements around the 300 MHz frequency range by using a (Ba,Sr)TiO₃ (BST) Chemical Solution Deposition (CSD) film and fine-pitch electrode structure. Two 200 nm-thick BST dielectric layers are deposited on an Si wafer with an Au-base electrode. The solder bump terminal for mounting to the circuit board is formed on the top Cr/Pt/Au electrode. The developed capacitor has a capacitance density of 2 μF/cm², an inductance of 30 pH, a resonant frequency around 230 MHz, and a breakdown voltage of 10 V. This paper describes the material technology of the dielectric BST film and thin-film electrode of the new capacitor.

1. Introduction

In the past few decades, the number of transistors being integrated into LSIs has increased exponentially according to the scaling rule. Scaling the transistors, for example, by one half increases the transistor density four times, decreases the transistor speed delay by one-half, and halves the operating voltage. However, increasing the number of transistors in an LSI decreases the overall impedance between the power supply and ground plane (VG impedance), which increases the LSI's current consumption and therefore increases its power consumption.¹⁾ Also, when the supply voltage in the LSI circuit drops, a large amount of current is required to return to the correct operating voltage. Thus, the VG impedance must be lowered to suppress voltage fluctuations. Placing a decoupling capacitor with a low impedance and, in particular, a low inductance near an LSI is one of the best ways to supply additional current to prevent momentary drops in supply

voltage.²⁾

Figure 1 shows the basic idea for obtaining a low power-distribution impedance using various types of capacitors. Different capacitors with various impedance characteristics are required to avoid anti-resonance. Utilizing a large number

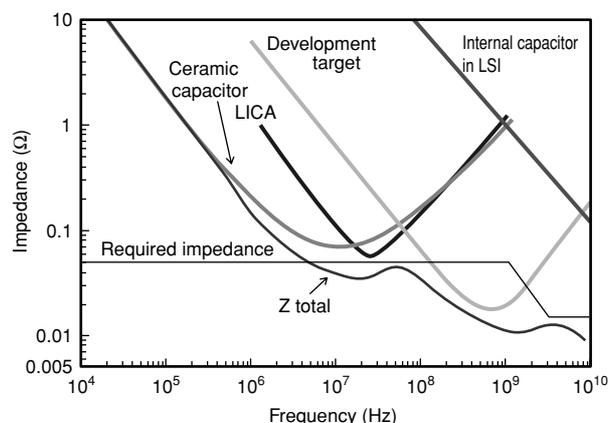


Figure 1 Impedance characteristics of various capacitors and required impedance.

of capacitors in parallel is also necessary to lower the total impedance below the target impedance across a wide frequency range.

Currently, three types of capacitors are used for high-speed digital circuit applications: multilayer ceramic capacitors, Low Inductance Chip Arrays (LICA) produced by AVX,³⁾ and internal capacitors in LSIs. Internal capacitors operate at frequencies above 1 GHz, which is close to the operating frequency of high-speed LSIs. In contrast, ceramic capacitors and LICA can only be used up to approximately 50 MHz. When only these three types of capacitors are used, it is difficult to cover frequencies around 300 MHz.

As described above, placing many capacitors in parallel is effective for lowering the impedance. However, since the area for mounting devices on the circuit board is limited, a large number of capacitors cannot be placed in this current system. Therefore, to obtain a lower impedance over a wide frequency range, it becomes necessary to develop a decoupling capacitor that can cover the frequency range around 300 MHz. To meet this requirement, we developed a new decoupling capacitor. The new capacitor features BST CSD films, thin-film Au electrodes, and a fine-pitch terminal structure. This paper describes the material characteristics of the BST dielectric, the interfacial reactions between the electrodes and dielectric, and the capacitor's electrical characteristics.

2. Overview of decoupling capacitors

A decoupling capacitor for high-frequency applications is most effective when it is close to the LSI, because this minimizes the inductance of the circuit board wiring and interconnects. There are three methods of placing a decoupling capacitor: (a) incorporating a dielectric layer in the wiring layer in the circuit board underneath the LSI, (b) placing a capacitor between the LSI and circuit board as an interposer, and (c) placing a capacitor near the LSI as a discrete component, as shown in **Figure 2**. These methods have the

following advantages and disadvantages.

In the first method, the capacitor is placed close to the LSI and the dielectric layers can be easily designed in the circuit board (e.g., it is easy to control the number of layers and the thickness and place the layers between the ground plane and power supply plane). Therefore, this method provides capacitors with a high capacitance and low inductance. However, if such a capacitor fails during the manufacturing process or during operation, it cannot easily be replaced, so the whole circuit board would need to be changed. This makes it necessary to obtain a high yield, because a low yield results in a high manufacturing cost.

The second method also places a capacitor close to the LSI. Therefore, the sheet inductance of wiring can be minimized. This method requires a substrate with three types of via holes that connect to the signal, ground, and power supply layer.

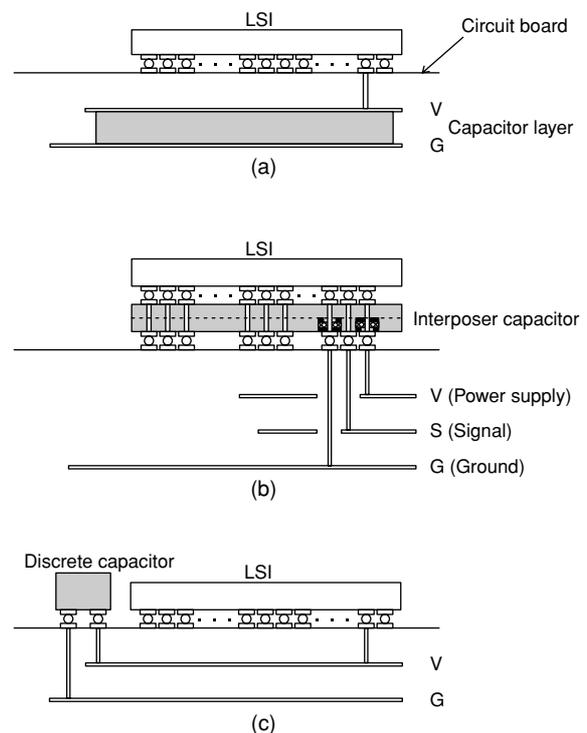


Figure 2
 Three types of decoupling capacitor: (a) capacitor layers incorporated in wiring circuit layer in circuit board, (b) interposer type capacitor placed between LSI and circuit board, and (c) discrete type capacitor mounted on circuit board.

Although a multilayer capacitor structure can be fabricated in the substrate as in the first method, the area of each dielectric layer is limited to the size of the interposer substrate. Also, the capacitors of this second method are not universal components but must be custom made because the via configuration of the interposer must be the same as that of the LSI. Therefore, this type of capacitor is relatively expensive and is therefore unsuitable for mass-production. Moreover, this type of capacitor is also not easy to replace, because it has two kinds of solder bump faces. Therefore, to obtain high-reliability interconnections with this type, solder materials with different optimum reflow-temperatures must be used.

The third method is widely applied to general discrete components. However, with this method, the distance between the LSI and capacitor is greater than with the other two methods, so the sheet inductance is higher. Also, since the capacitor occupies space on the surface of the circuit board, high-density mounting of LSIs is sometimes not possible, because of the large number of discrete passive components that are required on the circuit board. However, since the capacitors of this third method are universal components, they are inexpensive to produce. Also, these capacitors are easy to replace.

The capacitor we developed in this study is of the third type. Therefore, to cover the frequency range around 300 MHz, we needed to reduce the inductance in the capacitor itself.

Figure 1 shows typical impedance curves of the three types of currently used capacitors mentioned in Section 1 as a function of frequency. The slope of the impedance below the resonant frequency depends on the capacitance, the impedance at the resonant frequency is the capacitor's equivalent series resistance (ESR), and the slope in the higher frequency range depends on the equivalent series inductance (ESL). A capacitor with a high capacitance, low ESR, and low ESL is required to suppress the impedance. Our ob-

jective was to obtain a high-capacitance capacitor with an impedance below the target impedance by lowering the ESR and ESL below the values found in present ceramic chip capacitors and LICA.

A capacitor's characteristics are strongly related to the properties of the dielectric material. The value of the ESR is affected by the capacitor's electrodes, and the ESL can be controlled mainly by the design of the capacitor's structure. In the following sections, we describe our research and development in these areas in detail.

3. Research and development

3.1 Dielectric material

To make a high-capacitance and high-resistance capacitor, we need a dielectric material that has a high dielectric constant and a high dielectric strength. Also, a material without piezoelectricity is preferred, because piezoelectricity may cause damage between the dielectric layer and electrode during voltage fluctuation.

Figure 3 shows the dielectric strength versus dielectric constant for various thin-film dielectric materials.⁴⁾ The figure suggests there is an inverse relationship between the dielectric constant and dielectric strength. Other factors that have been shown to influence dielectric

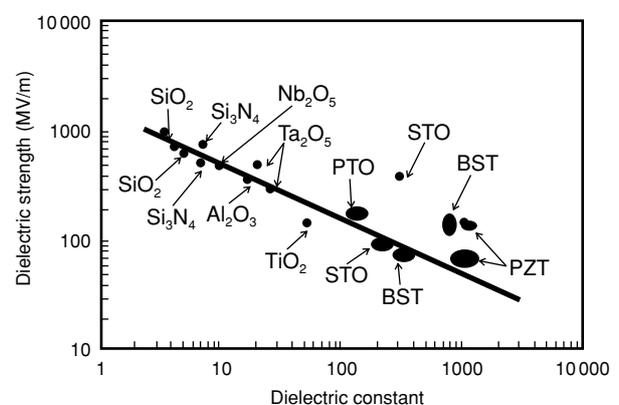


Figure 3
Correlations between dielectric strengths and dielectric constants of thin-film dielectric materials.

Table 1
Dielectric constants and dielectric strengths of BSTs annealed in atmospheres with different oxygen contents.

Ambient atmosphere (oxygen content)	Dielectric constant	Dielectric strength (MV/m)
Ar (2 ppm)	230	18
N ₂ (100 ppm)	225	21
Air (20%)	265	52
O ₂ (100%)	240	54

strength in BST thin-film capacitors include the film microstructure, electrode material, film stoichiometry, and the incorporation of dopants.⁵⁾

The required thickness of the dielectric layer depends on the dielectric strength of the dielectric material and is around 200 nm. The required capacitance is more than 1 $\mu\text{F}/\text{cm}^2$, and a voltage of at least 10 V must be applied to test for a high-reliability product. Thus, the dielectric material must have a dielectric constant exceeding 200 and a dielectric strength exceeding 50 MV/m. As shown in Figure 3, BST can meet both of these requirements.

Since the ferroelectricity/paraelectricity transition temperature of BST can be shifted to below room temperature by adjusting the ratio of BaTiO₃ to SrTiO₃, a material with non-piezoelectricity can be obtained at room temperature. Therefore, BST can satisfy all of the above requirements for a dielectric material. Thus, we decided to use BST in our decoupling capacitor.

Our BST (Ba_{0.5}Sr_{0.5}TiO₃) film is deposited by the CSD method and has a granular microstructure. By optimizing the annealing conditions of the BST gel, for example, the temperature, time, and atmosphere, we obtained a 150 nm BST film with a dielectric constant of about 250 and a dielectric strength of more than 50 MV/m. **Table 1** shows the dielectric constants and dielectric

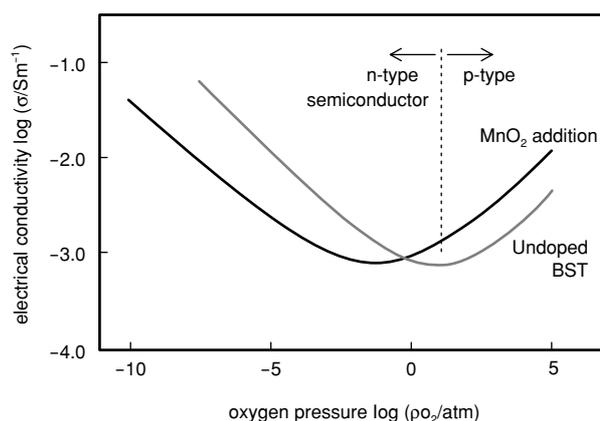


Figure 4
Effect of Mn-doping in BST on the electrical conductivity as a function of oxygen pressure in the ambient atmosphere.

strengths of BST films annealed in different atmospheres at the optimized temperature and time (750°C and 15 minutes).

These four films have almost the same dielectric constants, but the dielectric strength of the air and O₂ films are more than double those of the other two films. The Ar and N₂ we used are contaminated by 2 ppm and 100 ppm of oxygen, respectively, which increases the dielectric strength. When we apply the dielectric strength data in Table 1 to the equilibrium electrical conductivity diagram as a function of the partial pressure of oxygen in the ambient atmosphere, it seems that these data are located in the n-type semiconductor region, as shown **Figure 4**.

We assume that when the film is annealed, oxygen is lost from the lattice of the BST due to the formation of ionized oxygen vacancies and electrons in the conduction band. On cooling to room temperature, a large fraction of the electrons remain in the conduction band, because the ionization energy of the oxygen vacancies is low. To obtain a higher breakdown voltage, we assume that increasing the hole concentration, decreasing the electron concentration, and shifting the minimum in the conductivity-oxygen pressure relation to lower oxygen pressure are effective approaches. Therefore, we decided to anneal the BST film in air because of its high oxygen content.

Small amounts of Mn have been shown to lower leakage current, reduce resistance degradation by slowing the reduction of insulation resistance under a prolonged voltage stress, and increase dielectric strength.^{6,7)} X-ray photoelectron spectroscopy (XPS) measurements indicate that Mn compensates for the excess donor charge that is present in nominally undoped CSD BST films.⁸⁾ The reduction in leakage current in Mn-doped CSD BST films may be due to increased depletion widths, resulting in lower tunneling currents.⁹⁾ Mn may also lower leakage by trapping injected carriers by the reactions $Mn^{4+} + e^- \rightarrow Mn^{3+}$ and $Mn^{3+} + e^- \rightarrow Mn^{2+}$ depending on the valency of the Mn ion. Mn substitutes for Ti^{4+} at the B site of the ABO_3 perovskite lattice and thus acts as an acceptor type dopant.¹⁰⁾ In addition to lowering leakage, Mn has also been shown to increase the time before the onset of resistance degradation. The improvement in resistance degradation is thought to be due to Mn gettering positively charged oxygen vacancies, thereby preventing oxygen vacancy migration under an applied field.⁷⁾ By adding 1 at% Mn to CSD BST, a dielectric strength greater than 50 MV/m was obtained.

3.2 Electrode structure

To obtain a lower ESR in the capacitor, the electrical resistance of the electrodes must be minimized. Therefore, the electrode material should have a low resistivity and a thicker electrode is favorable. Furthermore, since BST is annealed in air as described in the previous section, a conducting material that is not oxidized in air at high temperature is required. The candidate materials which satisfy these requirements are Pt, Au, and oxide-based conducting materials such as RuO_2 , $SrRuO_3$, and IrO_2 .¹¹⁾ Since oxide-based conductors have a higher resistivity ($\sim 50 \mu\Omega \cdot cm$) than Pt ($10.6 \mu\Omega \cdot cm$) and Au ($2.3 \mu\Omega \cdot cm$), Pt and Au were promising materials for the electrode. **Figure 5** shows the impedance curves of three capacitors having the following material combinations

in their bottom electrodes:

- 1) Ti (100 nm)/Pt (400 nm)
- 2) Ti (100 nm)/Au (300 nm)
- 3) Ti (100nm)/Pt (100nm)/Au (150 nm).

These capacitors are fabricated with a 160 nm-thick BST CSD dielectric layer (dielectric constant: 220) on an Si wafer with a SiO_2 layer. Each capacitor has a gold top electrode. A 100 nm layer of Ti, which is commonly used as an adhesion layer, is formed below the bottom electrode. From Figure 5, we can see that the impedance of these capacitors is changed by the material combination of the bottom electrode.

Regarding the capacitance and ESR:

- The Ti/Pt capacitor has a capacitance that agrees with the value calculated for the capacitor configuration and dielectric constant of the material. The ESR of this capacitor is relatively high at 0.4Ω .
- The Ti/Au capacitor has a much lower capacitance than the expected value and, as expected, it has a low ESR.
- The Ti/Pt/Au capacitor has a capacitance between those of the Ti/Pt and Ti/Au capacitors and a higher ESR.

To clarify the impedance characteristics of these capacitors, we examined the elemental depth profile of the capacitor layers using an Auger

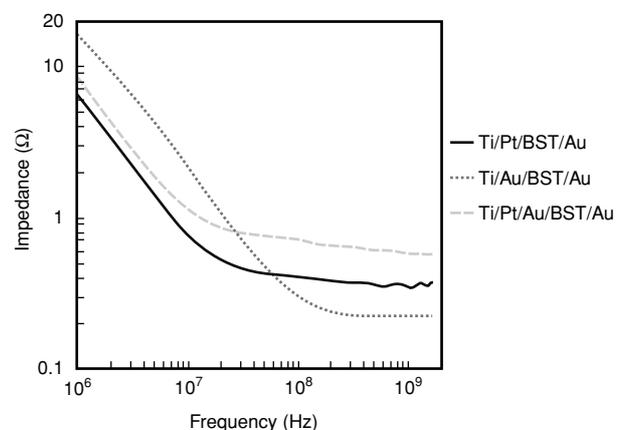


Figure 5 Impedance characteristics of capacitors with various electrode material combinations as a function of frequency.

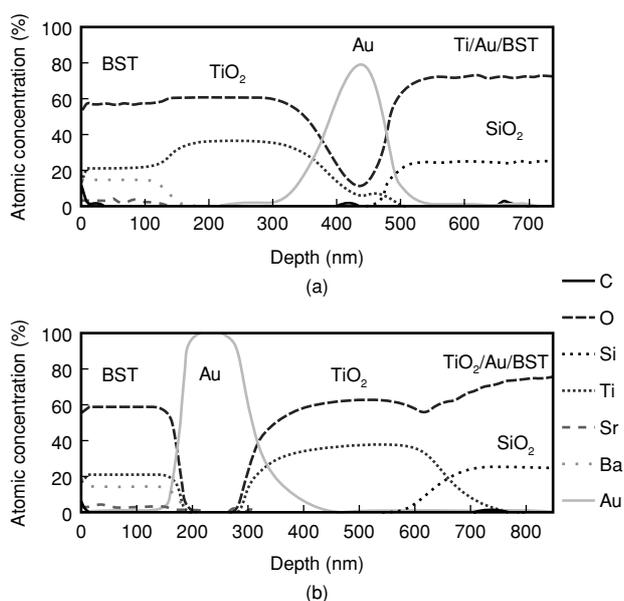


Figure 6
Depth profiles of elements in capacitors with (a) a Ti/Au/BST bottom electrode and (b) a TiO₂/Au/BST bottom electrode. Annealing was done at 750°C for 15 minutes.

Electron Spectroscopy (AES).

In the case of the Ti/Pt capacitor, a Pt-Ti-O compound is formed between the SiO₂ on Si and the remaining Pt layer. It appears that, in this structure, the Ti reacts with the SiO₂ on Si and the Pt during annealing. We suppose that this reaction causes the relatively high ESR of this capacitor. Since the remaining Pt layer acts as a barrier to Ti diffusion, the BST is not damaged by Ti diffusion. This probably explains why the measured capacitance is close to the calculated value.

Figure 6 (a) shows the depth profiles of the elements in Si/SiO₂/Ti/Au/BST annealed at 750°C for 15 minutes. The layer structure after annealing is Si/SiO₂/Au/TiO₂/BST. We suppose that interdiffusion between Ti and Au occurs and the Ti in the Ti-Au interdiffusion zone reacts with O in the BST. After the interdiffusion, all of the Ti in the Au-Ti is consumed to form TiO₂ adjacent to the BST, and as a result, a pure Au layer seems to be formed, which could explain the low ESR characteristics in the Ti/Au case. The low capacitance is caused by the TiO₂ (low dielectric constant)

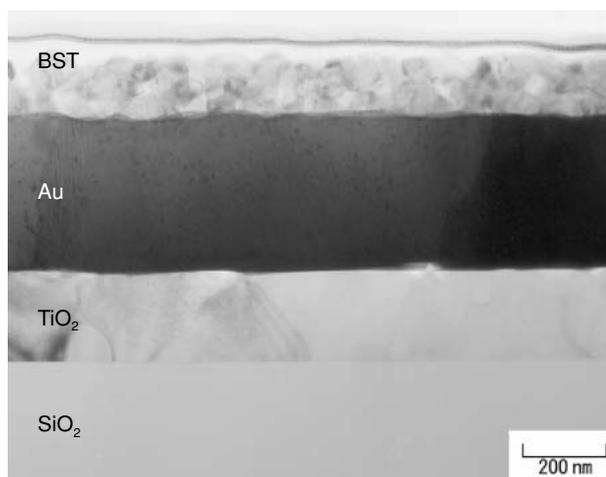


Figure 7
Cross section of TiO₂/Au/BST layers annealed at 750°C for 15 minutes.

layer, which is formed in series with the BST layer, as shown in Figure 6 (a).

In the Ti/Pt/Au case, it seems that Ti diffusion through the Pt/Au to the BST does not proceed sufficiently. We believe that this results in incomplete formations of the TiO₂ layer and pure Au layer, leading to the observed high capacitance and high ESR compared to the Ti/Au case. These results suggest that the movement of Ti during annealing affects the value of capacitance and ESR. Therefore, we applied TiO₂ as an adhesion layer instead of Ti. **Figure 6 (b)** and **Figure 7** indicate the post-annealing depth profiles of Si, SiO₂, TiO₂, Au, and BST and a post-annealing cross-sectional view observed by Transmission Electron Microscope (TEM), respectively. The layer structure does not differ from that before annealing, and therefore a high capacitance and low ESR are confirmed in this layer structure.

In order to lower the ESL, it is necessary to decrease the parasitic inductance of the electrodes. Reducing the electrode length is an effective way to achieve this and also reduces the electrode inductance. The discrete decoupling capacitor has two types of electrodes: a ground terminal (G) and a power supply terminal (V). The current flows in opposite directions in the two types of

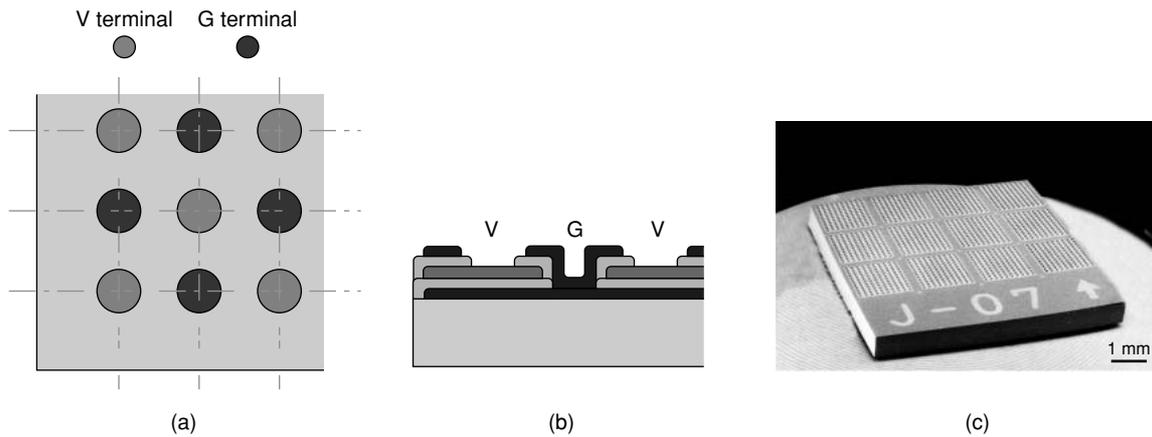


Figure 8 (a) Configuration, (b) cross-section, and (c) photograph of the G-V terminals of the developed capacitor.

terminals. A reduction in inductance can be achieved by designing an alternative current path, that is an alternate arrangement of G and V terminals, to minimize the inter-electrode mutual inductance as shown in **Figure 8 (a)**.

When the capacitors are connected in parallel, the inductance is added reciprocally according to the equation $1/L = \sum 1/L_i$. Therefore, as the number of terminals increases, the total inductance of the capacitors decreases. To increase the number of terminals in the given area, the inter-terminal spacing must be reduced. We applied the above three approaches in our capacitor.

The distance between the terminals is 150 μm , and 120 terminals are formed in a $1.6 \times 1.8 \text{ mm}$ area. **Figure 8 (b)** shows a cross-sectional schematic of the capacitors. To shorten the electrodes and thereby reduce the parasitic inductance, the columnar via structure is not applied.

3.3 Characteristics of the capacitor

We applied the results of our investigation into dielectric materials and electrode structure and developed a new discrete decoupling capacitor with a low inductance.

The capacitor contains two BST dielectric layers and a polyimide protection layer formed on the surface. Cr/Pt/Au metallization is formed on

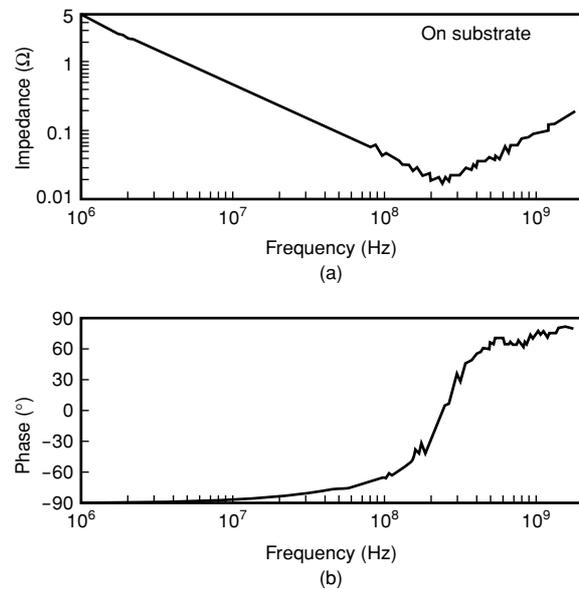


Figure 9 Impedance and phase of the mounted capacitor as a function of frequency.

the top electrode of the capacitor for a solder bump using an Sn-Ag lead-free solder system. The impedance characteristics are shown in **Figure 9**. The capacitance density is 2 $\mu\text{F}/\text{cm}^2$, and the capacitor can withstand a voltage of 10 V. When this capacitor is mounted on a circuit board, its ESR, ESL, and self-resonant frequency are 0.04 Ω , 30 pH, and 230 MHz, respectively.

4. Conclusion

We studied low-impedance decoupling capacitors for suppressing switching noise and stabilizing the voltage supply for LSIs operating around 1 GHz. A higher capacitance, lower ESR, and lower ESL capacitor are necessary to achieve a low impedance. This paper described our development of a new capacitor, focusing on the material technology.

We developed a dielectric material with a dielectric constant of about 250 and a dielectric strength of more than 50 MV/m in BST doped with Mn using the CSD method. To do this, we optimized the annealing temperature, time, and atmosphere. By using TiO_2/Au in the bottom electrode, diffusion of the adhesion layer can be prevented. As a result, the electrode layer structure provides a low ESR while maintaining a high capacitance. Because of the alternating configuration of ground and power supply electrodes and the large number of terminals, the capacitors have a low inductance. The prototype capacitor we developed has a capacitance density of $2 \mu\text{F}/\text{cm}^2$, an inductance of 30 pH, a resonant frequency of 230 MHz, and a breakdown voltage of 10 V.

To increase the capacitance and decrease the impedance of the capacitor, future work should focus on improving the capacitor layer, for example, by decreasing the dielectric film's unevenness and stress to increase the number of layers and developing a material with a higher dielectric constant and a higher dielectric strength.

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