A Study of Current Multilevel Interconnect Technologies for 90 nm Nodes and Beyond

●Takayuki Ohba

(Manuscript received February 7, 2002)

Technology trends of interconnects differ from those of transistors in that the performance of interconnects decreases as they are scaled down to satisfy stricter limits on line width and inter-line horizontal space. As interconnects follow this reverse scaling, the number of interconnects has been increased to realize a lower sheet resistance and higher reliability. A maximum of 10 levels of Cu interconnects is anticipated for 90 nm-generation logic devices that enter the gigahertz band. Cu/Low-k multilevel interconnect technology is an established technology that reduces wiring capacitance and therefore delay times. The incompatibilities between Cu interconnect processes and the material characteristics of Low-k have been investigated. This paper describes the current status and issues of Cu interconnects in system LSI and Cu/Low-k multilevel interconnects for 90 nm.

1. Introduction

The multimedia market represented by mobile devices has expanded very rapidly, and huge levels of system LSI consumption are expected. By 2010, system LSIs are expected to take the position currently held by memory and logic devices. One of the main technologies for system LSIs is the System-on-a-Chip (SoC). Recently, the Jisso Consortium, which is a consortium for advanced packaging technology, has proposed the System-in-a-Package (SiP), which has similar functions to the SoC.[1),2)]

With SoC and SiP, process development is carried out from the nano scale to the micron scale to meet the need for downsizing, high-speed processing, and lower power consumption in multimedia devices. High-speed processing in MPUs has been achieved through a combination of Cu interconnects and low-permittivity (Low-k) dielectrics. The Cu/Low-k combination has also been investigated for high-speed data transfer between chips in SiP.

This paper describes the current status of Cu/Low-k technology and investigates various Low-k materials and the feasibility of using Cu/Low-k technology in wafer processing. This paper also presents some predictions for the latest Cu/Low-k Damascene technologies.

2. System LSIs in multimedia

The advantages of system LSIs are their abilities in real-time data processing, multifunctional processing, and high-speed data transfer, which are indispensable functions in the multimedia world (**Figure 1**).[3)] LSI performance has been the decisive factor in the high-speed Internet infrastructure, and now that faster MPUs have been developed, more and more of the infrastructure will be made up of high-speed peripherals containing system LSIs.

Unlike transistor speed, which is limited only by gate architecture, the operation speed of a system is determined by the delay time of interconnects between devices, global wires, and

systems. The total delay time is given by the expression $\tau_{total} = \tau_{gate} + RC_s$, the derivation of which is given in the Appendix. The delay time due to interconnects in the current chip scale is determined by the interconnect resistance and wiring capacitance (RC delay). However, if there is a long distance between transistor blocks in a large chip operating at a high clock frequency, the LC delay becomes the dominant factor in the delay time because the inductance L increases with distance.[4] Therefore, for general transmission lines of SoC/SiP systems and high-speed system LSIs, it is essential to minimize the transfer loss due to the skin effect. This can be achieved, for example, by using twisted pairs for long connections and RC lines using Cu/Low-k for short connections.

3. Requirements for advanced Cu interconnect technologies

The major interconnect challenges are how to reduce the wiring resistance, capacitance, and number of migration failures. Copper (Cu) is used instead of aluminum (Al) because its resistivity is 1.67 μΩ-cm while that of Al is 2.62 μΩ-cm. Also, the higher melting point of Cu (1083.4°C vs. 660°C) makes it more resistant to migration failures than Al. **Figure 2** shows a comparison of the electromigration (EM) resistance of Cu and Al wire. As can be seen, the EM resistance of Cu is about two orders of magnitude higher than that of Al.[5] **Figure 3** shows the wiring capacitance of parallel wires 800 nm and 400 nm thick as a function of wiring pitch (width of wires and spaces). The wiring capacitance increases as the wiring pitch is reduced because the capacitance increases as the wires come closer together. The wiring capacitance can be lowered without increasing the sheet resistance by changing the metal from Al to Cu and changing the thickness from 800 nm to 400 nm as seen in Figure 3 I to II. This is because the resistivity and aspect ratio of Cu wire are lower than those of Al. The use of Cu interconnects therefore makes it easier to design high-density interconnects and reduces the number of interconnect levels compared to when Al is used. The reduction of interconnect levels reduces the manufacturing cost and increases the reliability because the interconnect process accounts for more than two-thirds of all wafer processes for 90 nm-generation devices.

To further lower capacitance, as seen in

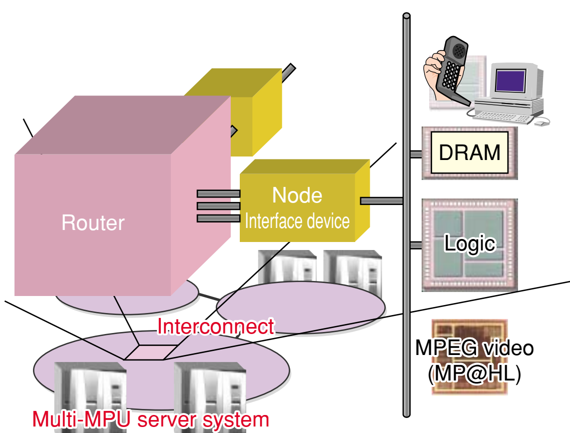


Figure 1
Schematic of global system and system LSIs.

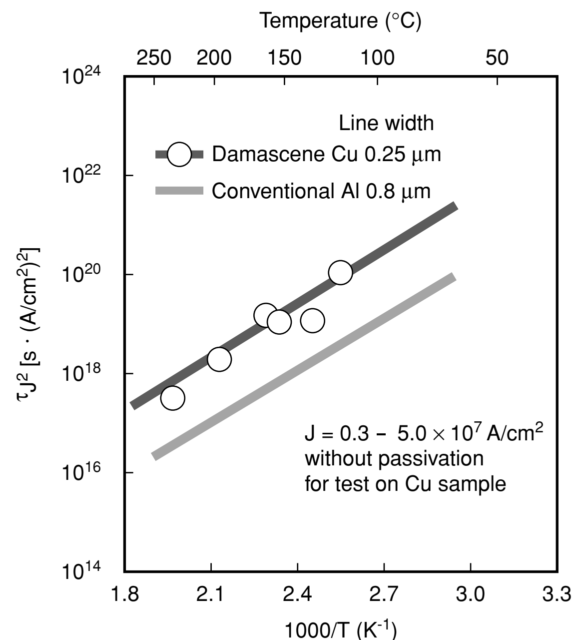


Figure 2
Arrhenius plot of electromigration resistance of Cu and Al wire, where τ and J are the failure time and current density, respectively.[5]

Figure 3 III, the permittivity (dielectric constant: k) of the inter-level dielectric (ILD) film should be lowered. This is the reason why Low-k (low permittivity) materials have been the focus of investigation in efforts to fabricate Cu interconnects with a low wiring capacity.

4. Current status of Low-k materials

Silicon dioxide (SiO_2, k = 4.2) has been used for inter-level dielectric films, because in addition to its superior thermal stability, moisture resistance, and resistance to chemicals, a lot of expertise has been accumulated about SiO_2 wafer processing. To maintain the integration capability in manufacturing, fluorine-doped SiO_2 (FSG, k ~ 3.6) has been developed as a post SiO_2 alternative. The permittivity of FSG film goes down as the fluorine concentration increases. However, increasing the fluorine concentration excessively increases the likelihood of film peeling and corrosion. This is because the reactivity of a fluorine-terminated SiO_2 surface is low and fluorine reacts easily with moisture to form hydrogen fluoride (HF). Therefore, various organic and inorganic materials have been proposed, including porous films (**Table 1**).[6] These low-permittivity materials are called Low-k materials, and materials with an even lower permittivity are called Very Low-k (VLK) materials.

In the case of Cu/VLK materials, the most serious problem is thermal stress. This is because there is a trade-off between a VLK's permittivity and its thermal expansion coefficient (**Figure 4**). When materials having different thermal expansion coefficients are added to either side of an interconnect, the interconnect is subjected to compressive and tensile stresses. **Figure 5** shows simulations of these stresses in eight levels of Cu interconnects in SiO_2 and a typical organic material at 400°C. Wire failures due to stress-migration (SM) occur when the stress exceeds the critical strength of Cu.

Figure 6 shows an estimation of inter-trench wiring capacitance as a function of the ILD permittivity when SiN and SiO_2 are used as cap and stopping layers either side of the ILD. The figure shows that although the capacitance decreases with the ILD permittivity, even at k = 1 (air bridge) it is still as high as 150 fF/mm. This high value is

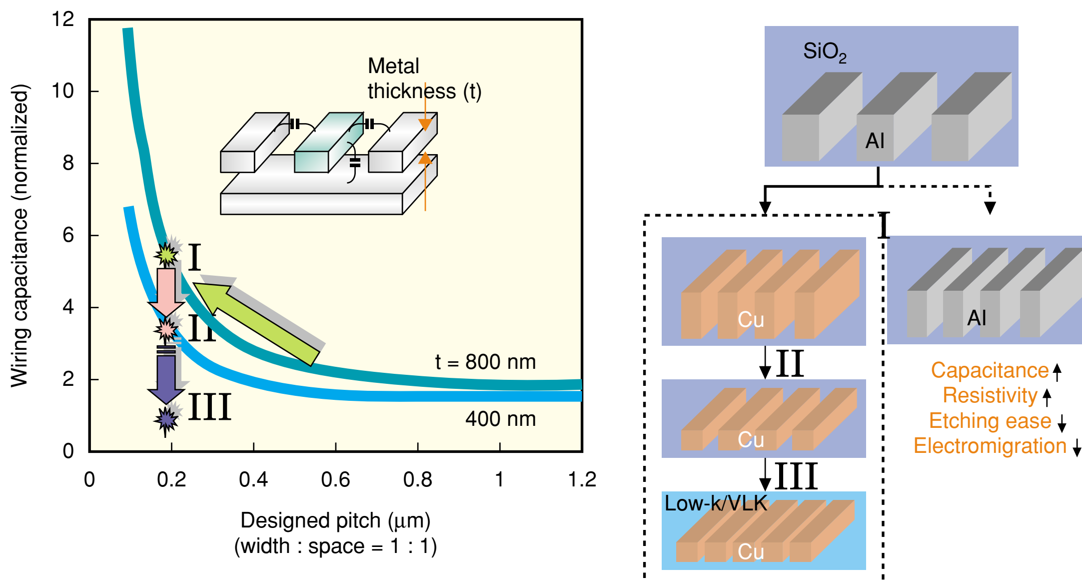


Figure 3
Wiring capacitance as a function of wiring pitch for 800 nm and 400 nm metal thicknesses.

Table 1
Comparison of Low-k materials.

Deposition method	Type of materials	Dielectric constant				
		4.0 to 3.6	3.5 to 3.1	3.0 to 2.6	2.5 to 2.1	< 2.0
CVD	Inorganic	SiOF	SiOF	BN		
			SiOB			Air gap
	Organic			Palylene-N	Palylene-F	
				Black Diamond[1)]	a-CF	
				Flow Fill[2)]		
				Coral[3)]		
Spin On	Inorganic SOG			T-22[4)]		Nanoglass[4)]
				FOX[5)]	NCS[7)]	HPS[7)]
				Type-12[6)]		
	Organic SOG			HSG-R7[8)]	ST-F2000[8)]	
				Type-9[6)]		
				T-18[4)]		
				HOSP[4)]		
	Organic polymer			SiLK[9)]	Cytop[12)]	Speed Film[13)]
				FLARE[4)]	Nautilus[9)]	
				Cyclotene[9)]	ELK-FLARE[4)]	
				Velox[10)]		
				Alcap[11)]		
				PQ-600[8)]		
				PQ-100[8)]		

note 1) Applied Materials, 2) Trikon, 3) Novellus Systems, 4) AlliedSignal, 5) Dow Corning, 6) TOK, 7) CCIC, 8) Hitachi Chemical, 9) Dow Chemical, 10) Schumacher, 11) Asahi Chemical, 12) Asahi Glass, 13) Gore

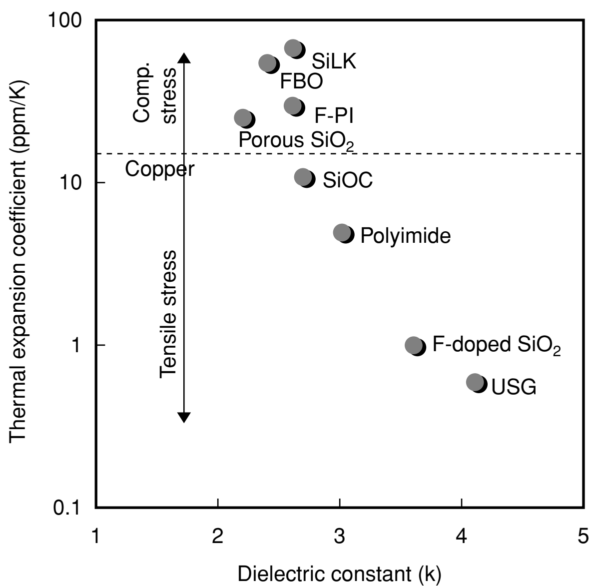


Figure 4
Thermal expansion coefficient as a function of dielectric constant.

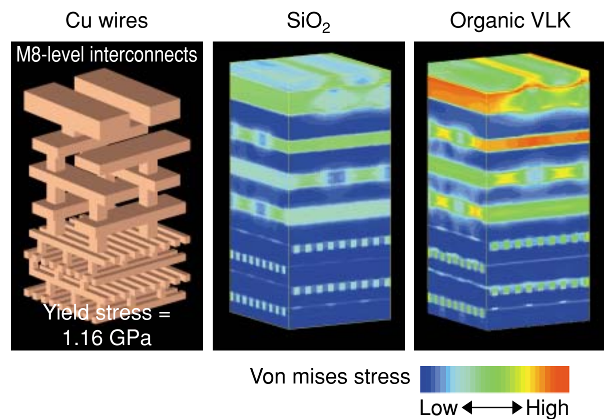


Figure 5
Simulated thermal stresses in 8 levels of Cu interconnects with SiO_2 and organic Low-k interlevel dielectrics (ILD) at 400°C.

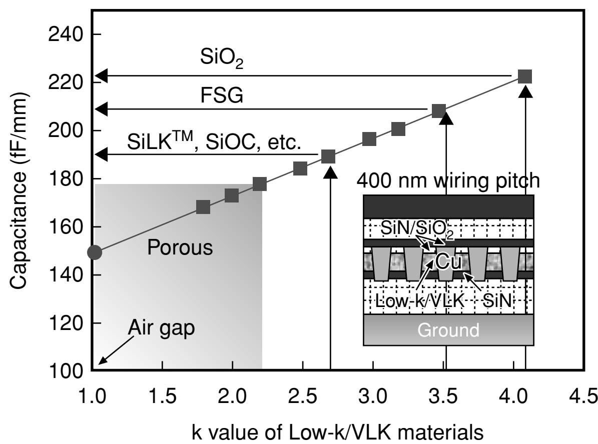


Figure 6
Estimation of inter-trench wiring capacitance as a function of dielectric constant of SiN/SiO_2 (70 nm/70 nm), Low-k/VLK (190 nm), and SiN (30 nm) ILDs.

Table 2
ILD structures for nodes down to 70 nm.

Node (nm)	180	130	90	70
k	3.5	2.7	2.7	< 2.5
Dielectric	FSG	SiLK™/USG	SiLK™	Porous
SiN, SiO^2, ILD structures	Cu, FSG	Cu, USG	Cu, VLK	Cu, VLK

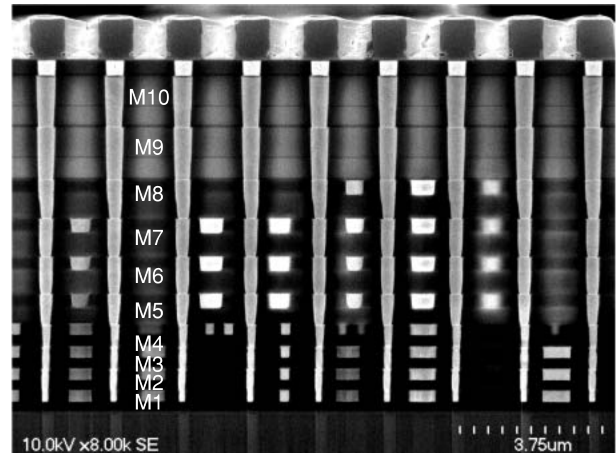


Figure 7
Cross-sectional SEM picture of 10-level Cu dual-Damascene structure fabricated using SiLK™ at the lower level (minimum feature size from M1 to M4) of multilevel interconnects.

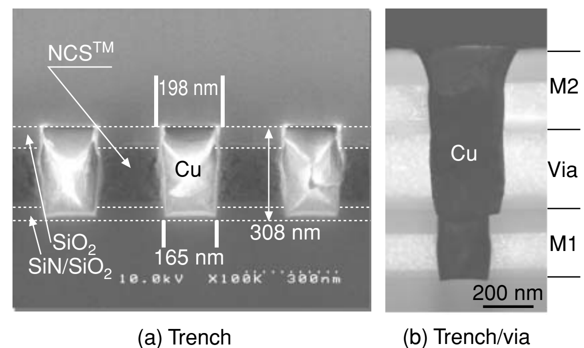


Figure 8
Cross-sectional SEM pictures of dual-Damascene Cu structure fabricated using porous SiO_2 (NCS™, k = 2.2).

due to the presence of the cap and stopping layers. **Table 2** shows various ILD structures that can be used to achieve appropriate wiring capacitances for nodes down to 70 nm. Using a combination of an organic Low-k (SiLK™ k = 2.7) and an SiO_2 hybrid structure, a wiring capacitance of 197 fF/mm with 0.4 µm lines and 130 nm spaces has been achieved.[7] To lower wiring capacitances below 190 fF/mm, SiO_2 hybrid structures are not suitable and must be replaced with a Low-k material. **Figure 7** shows a cross-sectional SEM picture of 10-level interconnects for a 90 nm-generation device that were fabricated using a production-worthy single-Damascene process. The dielectric layers between the interconnects are made of SiLK™ (M1-M4), SiOC (M5-M8), and SiO_2 (M9-M10). For the next generation down to 70 nm, porous materials having a k below 2.5 must be used in order to achieve wiring capacitances below 180 fF/mm. **Figure 8** shows a Cu plug we fabricated using a silicate porous VLK (Nano Cavity Silica = NCS™) and a single-Damascene structure. The wiring capacitance is 170 fF/mm, and the porosity is 38% (k = 2.2).

5. Cu dual-Damascene technologies

Cu interconnects having a Damascene structure are now widely used. In a Damascene

interconnect, Cu is embedded into a wiring pattern formed on dielectrics and then the excess Cu is polished-off with chemical-mechanical polishing (CMP). In the early stage of development, Cu dry etching was performed as well as Al patterning. However, it was very difficult to form fine Cu pattern without degrading resistivity, because the process produced Cu byproducts having a low vapor pressure and the Cu was easily oxidized. **Figure 9** shows the dual-Damascene (DD) process,[8] in which sequential patterning is performed from a horizontal trench pattern to via holes. Compared with the single-Damascene process, the metal interface between the via and trench is eliminated and thus the number of process steps are reduced. As a result, DD can provide a low wiring resistivity and shorter turn-around-time (TAT).

The process and process steps of the dual-Damascene method vary according to whether an organic or inorganic material is used for the dielectrics. Especially, the dry etching processes, photolithography resist masks, and etching-stopping layers for organic and inorganic materials are very different from each other. Because the etchant gases used in the DD dry etching process are different, for example, N_2/H_2 is used as an organic Low-k etchant and CxFy is used as an inorganic etchant, the etching selectivity of the resist mask for the stopping layer is different. The tradeoffs between critical dimension (CD) control of trench patterning, sputtering damage, and etching residues are common concerns in the etching process. Since there is both a physical and a chemical tradeoff, it takes time to optimize the etching profile and material combinations. **Figures 10 (a)** and **(b)** show, respectively, etching profiles of SiOC VLK dielectrics formed with the conventional etching process and an optimized etching process.

Because the etching profile of a trench is a cross-section of a Cu interconnect, the wiring resistance is changed for different etching profiles. When the tops of trenches are tapered due to excess sputtering during dry etching, the wiring resistance and wiring capacitance are changed and also electrical leakage tends to occur between interconnects (**Figure 11**). Meanwhile, the historical problem of etching residues that form at the via-holes is difficult to resolve rationally. One of the reasons for the difficulty is that etching residues such as hydrocarbons that are generated during etching and deposition are needed to form a fine trench and via structure. This means that the etching profile must be tuned from the etching reaction rate, the concentrations of byproducts, and residues.

Cu deposition by electrochemical deposition

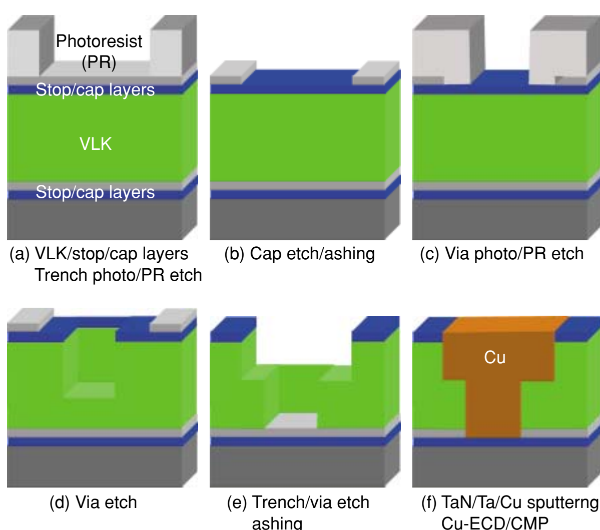


Figure 9
Process sequence for dual-Damascene interconnects.

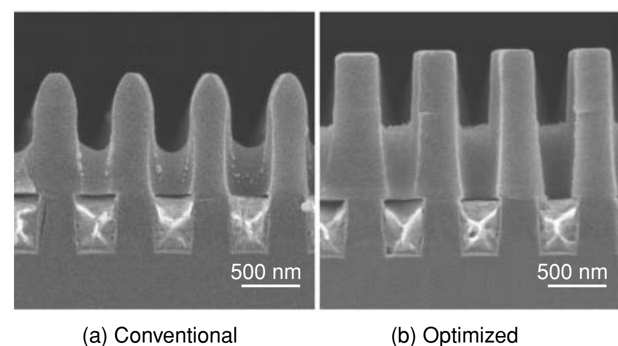


Figure 10
Cross-sectional SEM pictures of dual-Damascene structures after etching.

(ECD) methods, for example, electroplating, are used for Cu interconnects.[9] Electrochemically deposited Cu is a metallurgically metastable film, as demonstrated by its recrystalization even at room temperature.[10] In fact, the sheet resistivity of as-deposited ECD-Cu drops about 30% after 180 hours at room temperature and the grain size changes from 0.1 µm to 1 µm.[11] Many micro-voids below 5 nm are observed in as-deposited ECD film (**Figure 12**). On the other hand, the sheet resistivity and grain size of sputtered Cu film do not change at room temperature. The room-temperature recrystalization of as-deposited ECD-Cu may occur because of the presence of micro-voids due to plating chemistry. Therefore, to achieve metallurgically stable Cu metallization and fabricate Cu plugs in a DD structure for small-size features, further improvements and developments have been made in terms of additives in the plating and thermal treatment after ECD.

Usually, ECD-Cu is performed on a sputtered Cu/Ta (or Cu/TaN) bilayer, with Cu and Ta (or TaN) used as a seed layer and Cu diffusion barrier, respectively. Because the stepcoverage of sputtered film is poor due to the physical limitations of sputtering and degrades with higher aspect ratios in the trench and via structure, a very thin barrier metal (< 8 nm) is formed at the sidewalls of via-holes. If the thickness of the barrier layer goes down to the microcrystalline size of the barrier metal, films change from a continuous layer to an island-like growth (**Figure 13**). Island-like growth depends on the chemical properties of the Low-k surface and the presence of moisture. Obviously, an island-like barrier layer does not prevent Cu diffusion, and peeling of the Cu seed layer due to poor adherence can be seen when there is an island-like barrier layer. After a lot of effort to optimize surface treatment for the above process issues, adaptable electrical properties have been achieved for the minimum feature size

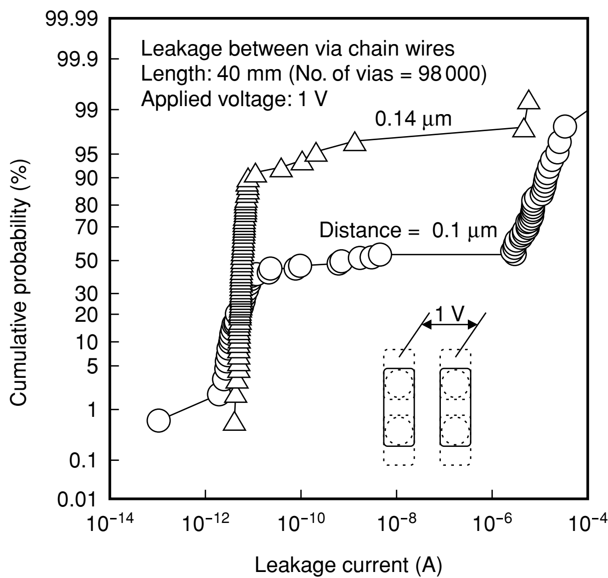
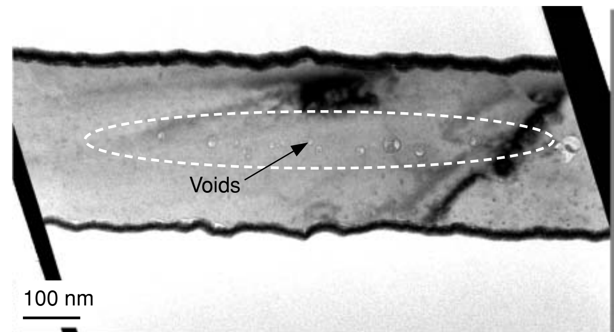
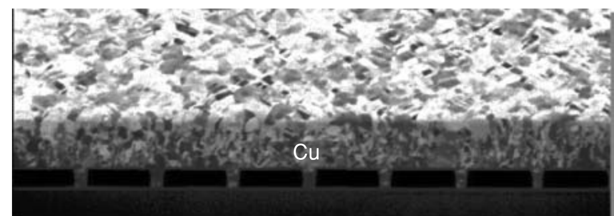


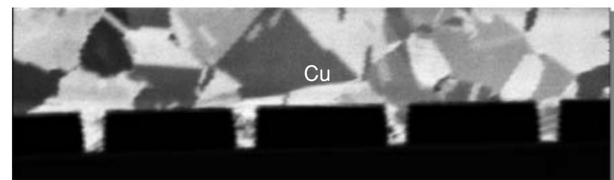
Figure 11
Leakage current of Cu/SiLK™ dual-Damascene interconnects.



(a) Micro-voids < 5 nm observed in as-plated Cu at trench



(b) One day after ECD-Cu (grain size < 0.1 µm)



(c) 11 days after ECD-Cu (grain size > 1 µm)

Figure 12
SEM and TEM pictures of ECD-Cu at room temperature.

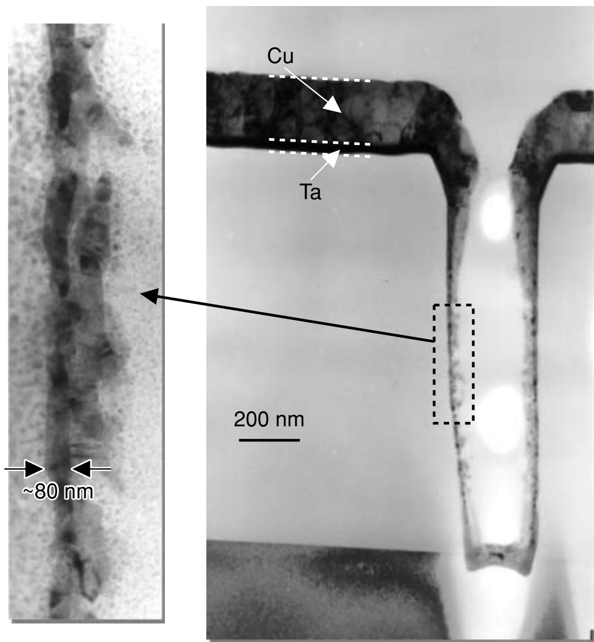


Figure 13
TEM cross-sectional views of Cu seed layer formed on Ta barrier metal. Island-like Cu was formed due to discontinuous barrier layer.

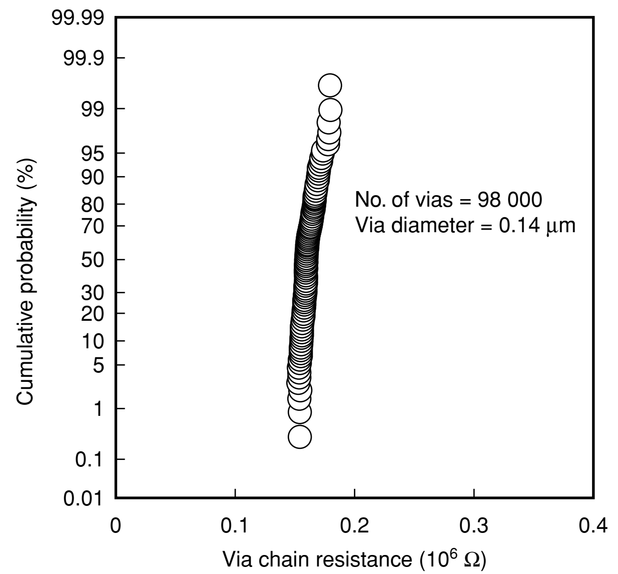


Figure 14
Via-chain contact resistance of Cu/SiLK™ dual-Damascene interconnects.

of Cu/SiLK™ interconnects in 90 nm-generation devices (**Figure 14**).

6. Conclusions

This paper described Cu/VLK multi-level interconnects for system LSIs and 90 nm interconnect technology. Cu/VLK is an essential technology for higher speeds and performance. For Cu/VLK fabrication, it is significant that the choice of Low-k material affects every aspect of ECD-Cu reliability and every process. The key technologies and production-worthy processes for sub-180 fF/mm 90 nm interconnects and beyond have been developed using dual-Damascene Cu structures and the Low-k dielectrics of SiLK™ and porous SiO_2. The contact resistivity and junction leakage current using these Low-k materials at a 0.28 μm pitch are low enough for 90 nm node interconnects.

This work was done in cooperation with the staff members of the 90 nm program at Fujitsu and Fujitsu Laboratories who are working on BEOL and packaging technologies.

Appendix

Total delay time τ_{total} is obtained as follows:

$$\tau_{total} = (R_{on} + R)(C_s + C_L)$$
$$\cong R_{on}C_L + RC_s$$
$$= \tau_{gate} + RC_s ,$$

where

R_{on} : On resistance of MOSFET
R : Wiring resistance
C_s : Wiring capacitance
C_L : Gate input capacitance

References

1) T. Sakurai: Interconnection from Design Prospective. Proc. of Advanced Metallization Conference 2000, ed. by D. Edelstein, G. Dixit, Y. Yasuda, and T. Ohba (Mat. Res. Soc., PA, 2001), p.53.
2) T. Suga and K. Otsuka: A New Era of System Integration and Packaging (in Japanese). *J. Electronics Packaging*. Japan Institute of

Electronics Packaging, **13**, 7, p.621 (2000).
3) T. Ohba: Multilevel Interconnect Technologies in SoC and SiP for 100-nm Node and Beyond. Proc. of IEEE 6th International Conf. on Solid-State Integrated Circuit Technol. (ICSICT), ed. Bing-Zong Li, Guo-Ping Ru, Xin-Ping Qu, Paul Yu, and H. Iwai, p.46 (2001).
4) K. Masu: GHz Interconnect in ULSI (in Japanese). *Technical Report of IEICE.* The Inst. of Electronics, Information and Communication Eng., **101**, 1, p.87 (2001).
5) N. Misawa, T. Ohba, and H. Yagi: Planarized Copper Multilevel Interconnections for ULSI Applications. *MRS Bulletin*, **XIX**, 8, p.63 (1994).
6) T. Ohba: Material and Process Challenges in 100-nm Interconnects Module Technology and Beyond. *J. Electronic Materials,* **29**, 10, p.314 (2000).
7) H. Kudo, K. Yoshie, S. Yamaguchi, K. Watanabe, M. Ikeda, K. Kakamu, T. Hosoda, K. Ohhira, N. Santoh, N. Misawa, K. Matsuno, Y. Wakasugi, A. Hasegawa, K. Nagase, and T. Suzuki: Copper Dual Damascene Interconnects with Very Low-k Dielectrics Targeting for 130 nm Node. Proc. of IEEE Int. Interconnects Conf. (IITC), p.270 (2000).
8) C. W. Kaanta, S. G. Bombardier, W. J Cote, W. R. Hill, G. Kerszykowski, H. S. Landis, D. J. Poindexter, C. W. Pollard, G. H. Ross, J. G. Ryan, S. Wolff, and J. E. Cronin: Dual Damascene: A ULSI Wiring Technology. Proc. of 8th Int. IEEE VLSI Multilevel Interconnection Conf., p.144 (1991).
9) V. M. Dubin, Y. Shacham-Diamand, B. Zhao, P. K. Vasudev, and C. H. Ting: Selective and Blanket Electroless Copper Deposition for Ultralarge Scale Integration. *J. Electrochem. Soc.*, **144**, p.898 (1997).
10) C. Cabral, Jr., P. C. Andricacos, L. Gignac, I. C. Noyan, K. P. Rodbell, T. M. Shaw, R. Rosenberg, J. M. E. Japer, P. W. DeHaven, P. S. Locke, S. Malhotra, C. Uzoh, and S. J. Klepeis: Room Temperature Evolution of Microstructure and Resistivity in Electroplated Copper Films. Proc. of Advanced Metallization Conference 1998, ed. by G. S. Sandhu, H. Koerner, M. Murakami, Y. Yasuda, and N. Kobayashi (Mat. Res. Soc., PA, 1999), p.81.
11) T. Ohba and T. Nakamura: Current Status and Issues for Cu Interconnect Technology (in Japanese). Proc. of Scientific and Tech. Div. (VI) Symp., Japan Inst. Metals, Tokyo, Jan. 26, p.5 (2001).

Takayuki Ohba received the Ph.D. in Electrical Communication from Tohoku University. He joined Fujitsu Ltd., Kawasaki, Japan in 1984, where he has been engaged in research and development of multilevel interconnect processes for high-speed devices and contributed more than 100 papers. He is a member of the Japan Society of Applied Physics and an executive committee member of the Advanced Metallization Conferences.