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Advanced LSI Packaging Technologies

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Mobile devices need to be small, and the packages of most chips have been miniaturized as much as possible in order to meet this need. The Chip Size/Scale Package (CSP) was realized in the 1990s, and Fujitsu, as one of the pioneers in this area, has supplied various CSPs. This paper describes the structure, characteristics, and reliability of Fujitsu's CSPs. Then, a package for high-speed devices is described.

1. Introduction

The emergence of mobile devices such as cellular phones and digital video/still cameras has been made possible by the explosive evolution in semiconductor devices and fine-patterned printed circuit boards (PC boards). One of the results of this evolution is a new concept called the "System-on-a-Chip (SOC)." Today's mobile devices have been realized through the combination of this technology and new LSI packaging technologies.

Mobile devices need small components, so packages must be near to the size of a chip. The Chip Size/Scale Package (CSP) was developed in the 1990s to meet this need. Fujitsu was one of the pioneers of CSPs.[1),2)]

The first compact package for Fujitsu's "Mova F" cellular phone was the Printed Circuit board Leadless Package (PCLP).[3)] This package could endure a reflow temperature (nearly 220°C) although it had a PC-board substrate. Some of the materials used on PCLPs are still being used in current CSPs to maintain a high reliability.

An important year for the CSP was 1992, when the CSP concept was proposed to the package engineering industry. Since then, many kinds of CSPs have been proposed by LSI manufacturers.

The most popular CSP is the Fine pitch Ball Grid Array (FBGA), which is widely used for memory and logic chips. Chapter 2 of this paper describes these FBGAs. Then, Chapter 3 describes the BCC, BCC++, FD-FBGA, Super-CSP, and FLGA packages. (The Small Outline No lead [SON], Bump Chip Carrier [BCC], and Super Chip Size Package [Super-CSP] are described in detail in Ref. 2)). Then, Chapter 4 looks at the multichip package. Another major target for electronic devices is higher speeds – for example, the operating frequency of microprocessors is now entering the GHz region – therefore, in Chapter 5, we describe some packaging technologies for high-speed LSIs. **Figure 1** shows some typical CSPs manufactured by Fujitsu.

2. FBGA[4)]

As shown in **Figure 2**, the FBGA structure and assembly technology are very simple. A chip is attached using an epoxy-based adhesive to a polyimide substrate used as an interposer. In the next step, gold wires 25 μm in diameter are bonded between the chip electrode pads and inner leads on the interposer. Then, the chip area is covered with an encapsulant by transfer molding. Finally, solder balls are mounted onto the solder pads of

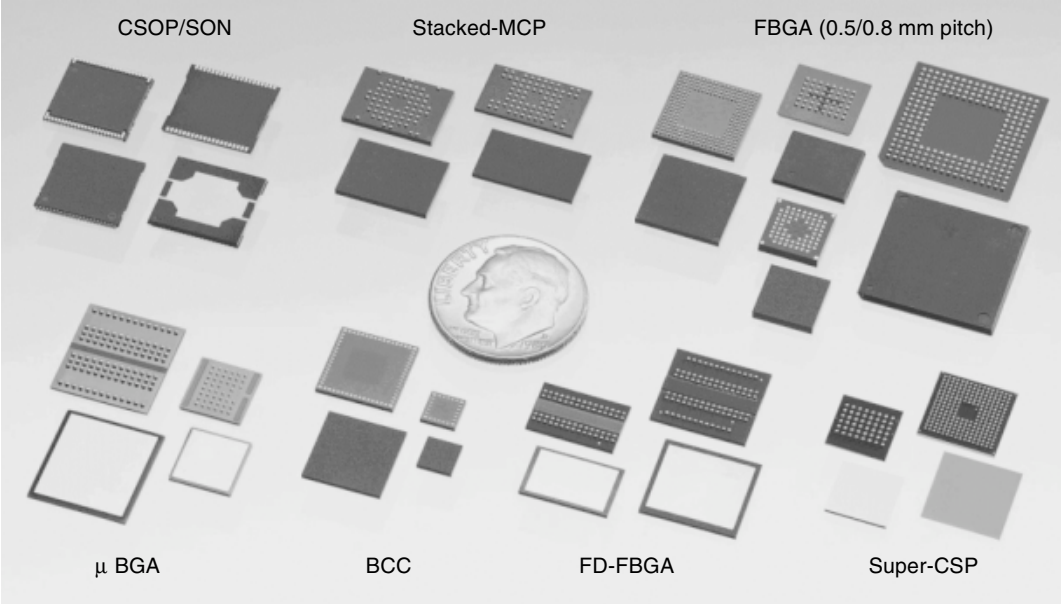


Figure 1
Example Chip Size/Scale Packages (CSPs).

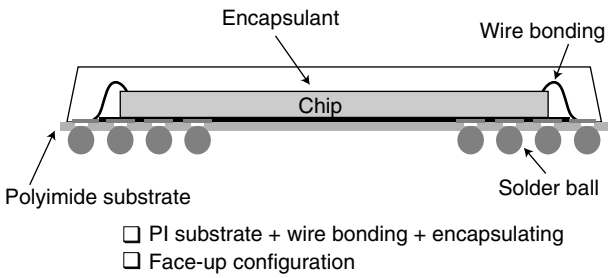


Figure 2
Structure of FBGA.

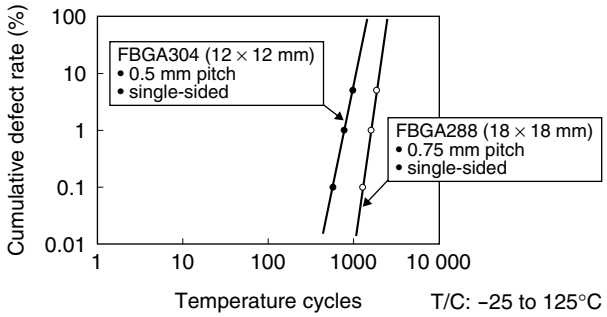


Figure 3
FBGA solder joint reliability after temperature cycling.

the interposer and reflowed in a furnace and the FBGA is cut out from the substrate. This assembly process does not need specially developed equipment because it can be performed using conventional machines without any modifications.

The main concern about CSPs is the reliability of the very fine solder-ball joints, so temperature cycle testing and mechanical testing are key evaluation methods for CSPs. **Figures 3** and **4** show the results of some of these tests for various FBGAs. As can be seen, the tested packages have excellent reliabilities. FBGAs are currently in use in many kinds of mobile devices.

3. New CSPs

The following new CSP packages are available from Fujitsu:

- Bump Chip Carrier (BCC), BCC++
- Face Down – Fine pitch Ball Grid Array (FD-FBGA)
- Super Chip Size Package (Super-CSP)
- Fine pitch Land Grid Array (FLGA)

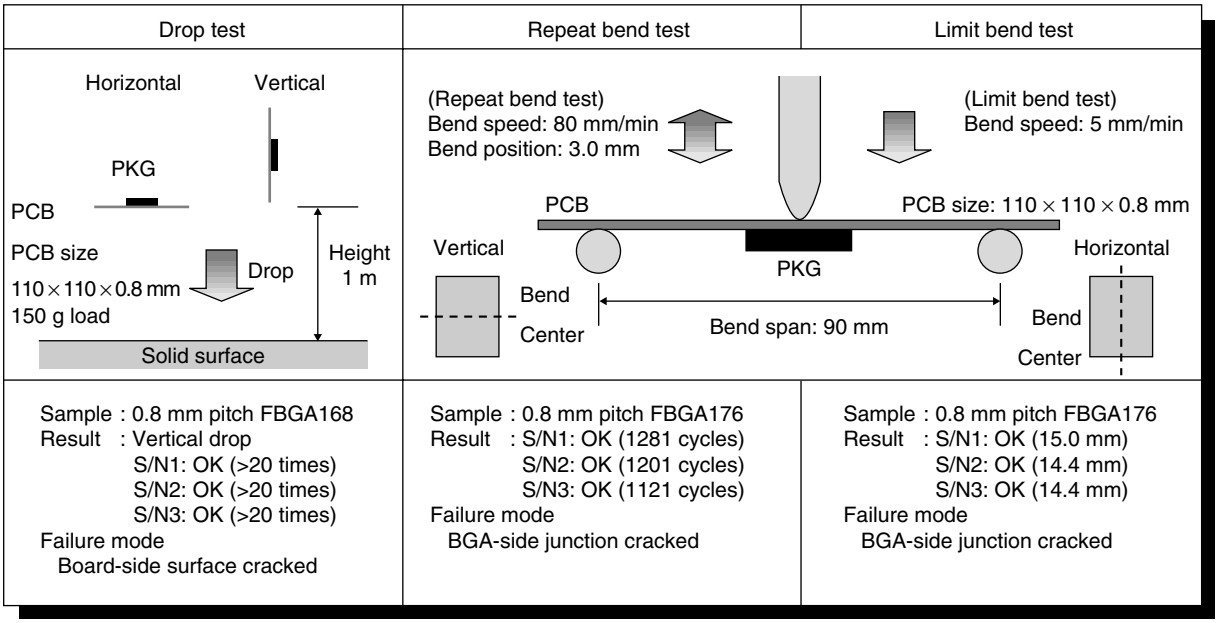


Figure 4
Drop and bend testing.

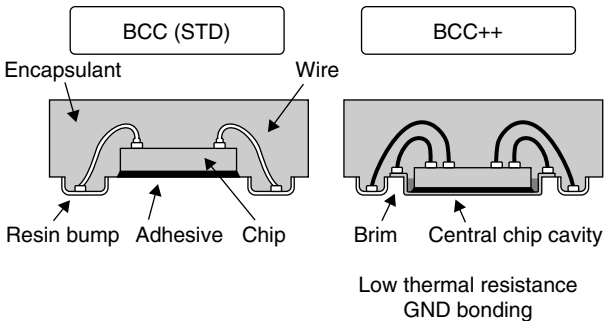


Figure 5
Structure of BCC.

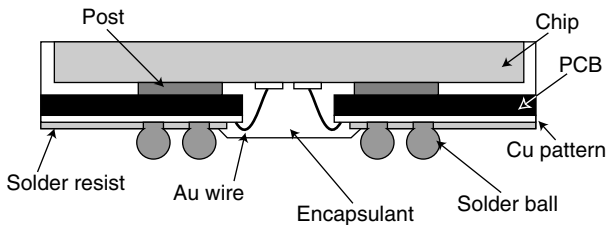


Figure 6
Structure of FD-FBGA.

3.1 BCC, BCC++[5)]

The BCC and BCC++ are unique CSP packages because they have no interposer (**Figure 5**). Instead, these packages use a special leadframe that has plated dimples. First, a chip is bonded with adhesive onto the center of the leadframe and wires are bonded between the dimples and the pads on the chip. After covering the chip with an encapsulant, the uncovered leadframe is etched out except for the dimpled portions, which then become bumps for the outer terminals. The bonded wires are short because there is a direct path between the chip pads and the outer terminals.

The BCC++ has almost the same structure as the BCC except that it has a die stage which is used as a ground plane and heat disperser. These packages are used for RF devices in wireless applications because they have enhanced electrical properties.

3.2 FD-FBGA

Current DRAMs have bonding pads in the center of the chip's upper side, so CSP technology must also be applicable to this configuration. The FD-FBGA is a type of CSP specially designed for DRAMs. The structure is shown in **Figure 6**.

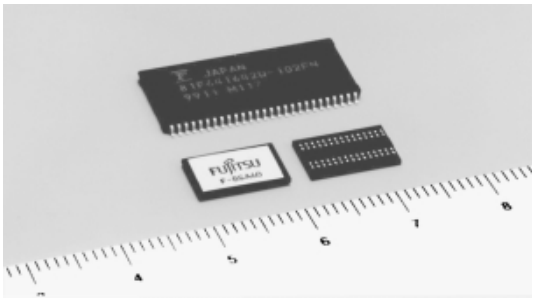
This package uses a PC board of high-temperature FR-4 with adhesive posts for chip attachment and a center opening for wire bonding that has been pressed out. This interposer has a single patterned layer of copper covered by solder resist at the bottom of the package. There is no need to perform through-hole drilling and via plating, so the interposer is cost effective.

Figure 7 shows a FD-FBGA 60-pin version and a conventional Thin Small Outline Package (TSOP) 54-pin version of a 64 Mbit SDRAM. The FD-FBGA package is within 10.10 mm × 6.40 mm × 1.00 mm, weighs 0.11 g, and has a ball pitch of 0.65 mm. The FD-FBGA requires only 25% of the mounting area required by the TSOP. The largest mountable chip size is only 0.5 mm smaller than the package size.

Figure 8 shows the process flow. The work proceeds on a large sheet containing many chips. The chips are attached to the substrate by a chip mounter. The key point is that the height of the epoxy posts provide enough of a gap between the chip and substrate. A gap of over 120 μm enables the encapsulant to flow from the center opening to the side portion of the chip. Because the sides of the chips are covered with encapsulant, when the encapsulant hardens, the FD-FBGA becomes mechanically strong and suitable for fan-out and fan-in ball arrangements.

Because of this feature, this package is suited for the DRAM chip shrinkage. The wire bonding is short, which improves the electrical performance. A ball-mounting machine attaches the solder balls. After the package has been singulated by a sawing machine, it is marked by a laser-marking machine.

Table 1 shows the lumped electrical characteristics of the FD-FBGA 60-pin and TSOP 54-pin that were obtained from a simulation for 100 MHz. The figure shows that the L, C, and R of the FD-FBGA are smaller than in the conventional TSOP. These small values of L, C, and R lead to a small propagation delay and decreased ground bounce. The thermal resistance of the FD-FBGA 60-pin is



FD-FBGA 60-pin, 0.65-mm pitch, 64-Mbit SDRAM (× 16)

Figure 7
FD-FBGA (Face-down fine pitch BGA).

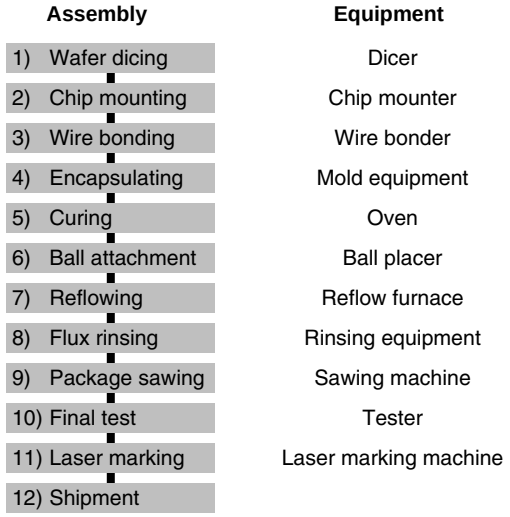


Figure 8
FD-FBGA assembly flow.

Table 1
FD-FBGA electrical characteristics.

	FD-FBGA 60-pin	TSOP 54-pin
Inductance (L)	Max. 1.9 nH Min. 1.0 nH	Max. 6.3 nH Min. 4.6 nH
Capacitance (C)	Max. 0.7 pF Min. 0.4 pF	Max. 0.8 pF Min. 0.6 pF
Resistance (R)	Max. 58 mΩ Min. 32 mΩ	Max.114 mΩ Min. 105 mΩ

note)
Simulator : Parasitic Parameter-3D (R, L), Maxwell-3D (C), IBIS (R, L, C)
Trace length : 0.61 to 1.89 mm (FD-FBGA 60), 4.53 to 7.80 mm (TSOP 54)
Frequency : 100 MHz

around 60°C/W, which is larger than that of the 54-pin TSOP (30°C/W). However, the FD-FBGA has an exposed chip configuration which allows heat to flow freely through a heat sink directly attached to the exposed chip.

Figure 9 shows a Weibull plot of the results of a temperature cycle test for the solder joint reliability of a motherboard with FD-FBGAs mounted on both sides. The figure shows that after 800 cycles, the cumulative defect rate was 0.1%. **Figure 10** shows the results of mechanical tests. These excellent results show that the FD-FBGA has quite a high reliability.

3.3 Super-CSP

The Super-CSP is made by a Wafer Level Packaging (WLP) technology that enables fabrication of extremely small packages (**Figure 11**).

Conventional packaging is performed individually for each chip. (i.e., chip attachment, wire bonding, sealing, solder ball attachment, marking, and singulation). However, Super-CSP is processed

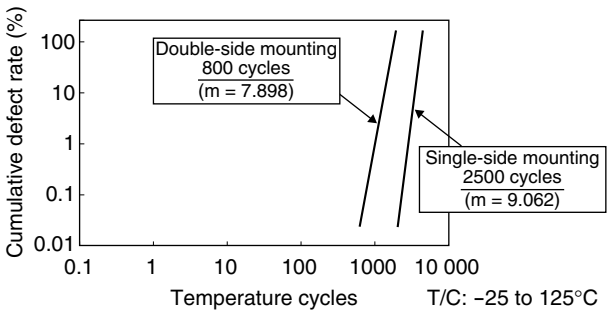


Figure 9
Solder joint reliability of FD-FBGA.

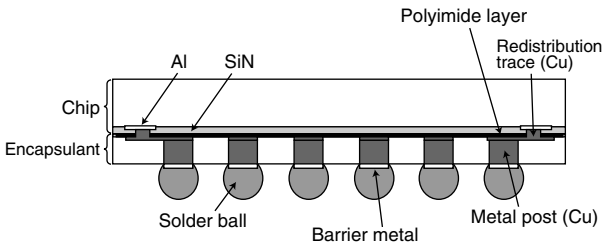
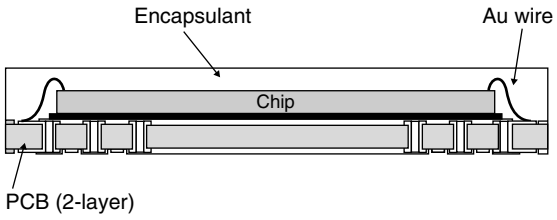


Figure 11
Structure of Super CSP.

	Drop test	Bending cycle test	Bending test
	• Package: FD-FBGA 60-pin • Board: FR-4 (t = 0.8 mm), Land diameter: 0.35 mm, Solder resist opening: 0.45 mm		
Method	Horizontal drop Package Test board Sample (on single side) + dummy weight 150 g Height: 1 m Concrete floor	Condition Bending speed: 80 mm/min Bending displacement: 3.0 mm Bending cycle test Bending test Tool Bending span: 90 mm	
Results	Dropping 55 times: Pass Destruction mode: Cu trace open on the test board (solder joint part: no crack)	Bending cycle 6250 cycles: Pass Destruction mode: Solder ball crack (package side)	Bending displacement 9.00 mm: Pass Destruction mode: Chip crack

Figure 10
Drop test, bending cycle test, and bending test.



❑PCB substrate + wire bonding + encapsulating
❑Terminal pitch is 0.65 mm

Figure 12
Structure of FLGA.

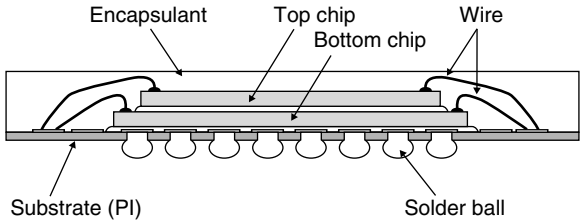


Figure 13
Structure of stacked MCP (FBGA).

by the following steps: re-routing, metal-post formation, compression molding, ball attachment, and dicing and the work done in these steps follows the shape of the wafer not the chips. Also, electrical function testing throughout the wafer may be possible. A Super-CSP is regarded as a Known Good Die (KGD) that is easy to handle and mount onto a motherboard. The Super-CSP is therefore expected to be used in Multi Chip Modules (MCMs) and Direct Chip Attach (DCA) applications.

3.4 FLGA

The structure of this CSP looks almost the same as that of an FBGA, but this package has no solder balls on the outer terminals (**Figure 12**). This package uses a PC-board as the interposer. The encapsulant has almost the same thermal expansion as the PC-board. These two features give the FLGA good mechanical reliability. This package is suitable as a lead free package because of the absence of solder balls.

4. Multi chip package

The basic concept of SOC is to integrate various circuits such as logic and memories on a single chip. However, recently another solution has been proposed by packaging technologist. This idea is the "Multi Chip Package (MCP)," which contains multiple memory and logic chips in a single package and is operated just like SOC. The MCP, therefore, is a system-oriented solution.

Figure 13 shows the structure of an MCP package. The key packaging technologies used here are stacked chip bonding and wire bonding. The chip is bonded with an adhesive tape that does not extend beyond the chip's periphery. Because this tape does not cover the wire-bonding pad, wire can be bonded onto clean pads. Because the top chip is farther away from the substrate than the bottom chip, the wires of the top chip need to be as straight as possible to minimize their length. To achieve this, a special wire looping technique is used on the wire bonder. Flash Memory and SRAM have already been combined using this package technology, and new combinations of logic and memory will be realized in the near future.

5. Enhanced package for high-speed LSIs

Network devices using SOCs require a greater capacity and faster data interchange and transmission rates. **Figure 14** shows projections for data rate regarding transmission devices. To achieve these projections, it will be necessary to increase the signal number and transmission speed per path.

5.1 High-pin-count package

Increasing the I/O pin count of an LSI chip is an effective way to increase the data rate because it enables I/O data to move over wide signal paths. As shown in **Figure 15**, the conventional chip interconnect technologies of wire bonding and TAB lead terminals from the periphery of the chip. Flip-chip bonding, on the other hand can lead terminals from any position on the chip surface.

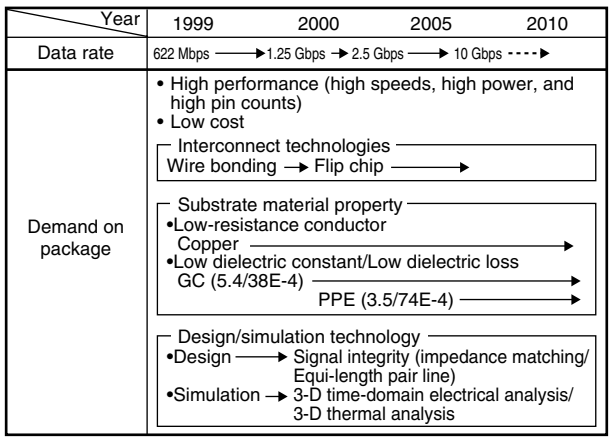


Figure 14
Market trend for transmission devices.

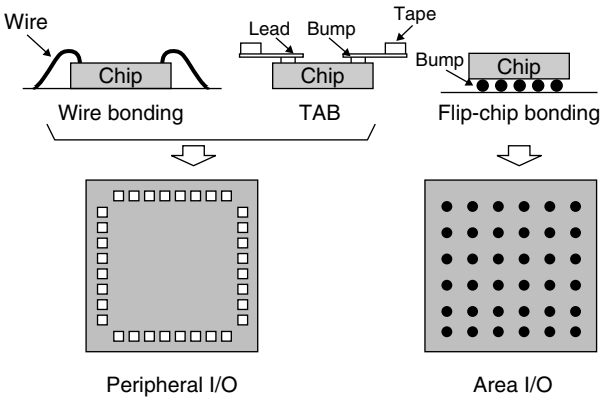


Figure 15
Interconnection technologies.

Flip-chip bonding therefore is better suited for high pin counts.

Figure 16 shows a typical FC-BGA that was fabricated using flip-chip technology. **Figure 17** shows the structure of an FC-BGA having a glass ceramic substrate. The advantages of glass ceramics are their low dielectric constant, low-electrical-resistance Cu traces, and a thermal expansion that is close to that of a motherboard. Also, it is easy to make multi-layered (high-density routing) structure.

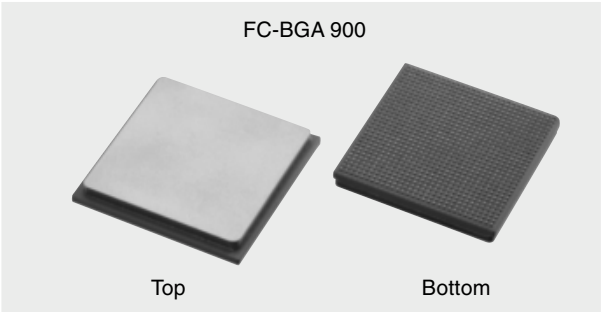


Figure 16
FC-BGA.

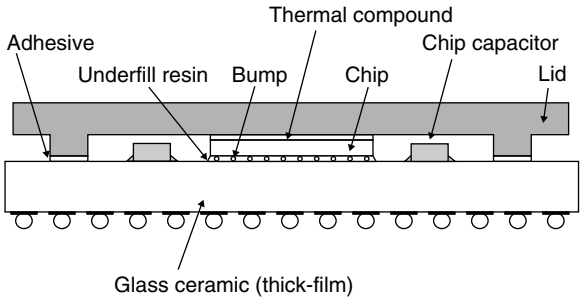


Figure 17
Structure of FC-BGA.

5.2 Packages for high-speed signals

The following problems regarding signal transmission in packages are anticipated:

1) Signal transmission delay
2) Noise
3) Decreased signal energy.

Regarding the first problem, the major causes are long lines and reflections. The lines can be shortened by miniaturizing packages, but this would also necessitate lowering the design rule of the motherboard in addition to reducing the outer lead pitch.

Reflections are caused by characteristic impedance mismatching, so it is important to adjust characteristic impedances to the signal lines of the LSI. **Figure 18** shows the impedance profile of a signal line of the FC-BGA1600. As can be seen, the impedance is within 11 ohms between two pads.

There are two types of noise that present

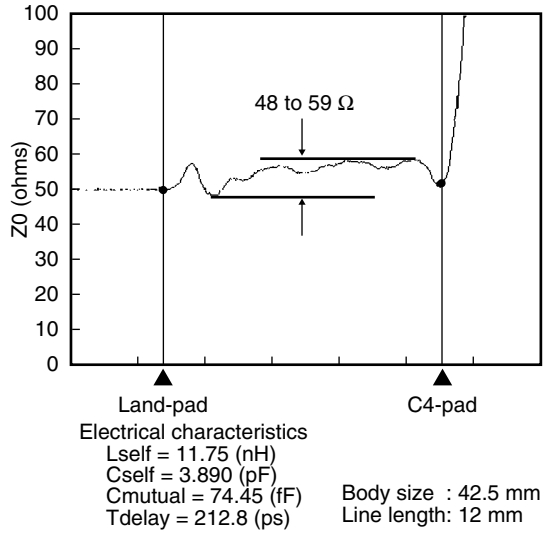


Figure 18
Impedance profile of FC-BGA1600 signal line (longest line).

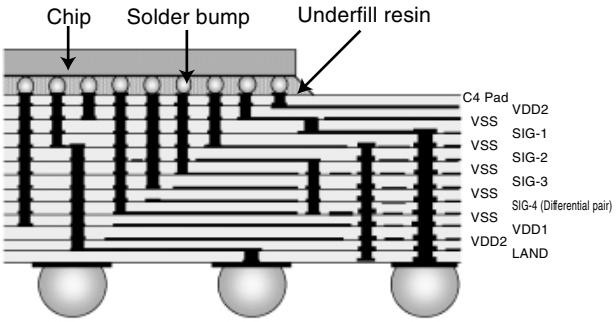


Figure 19
Structure of FC-BGA.

problems: simultaneous switching noise and crosstalk noise. Simultaneous switching noise is caused by changes in the ground voltage level. Generally, it is defined as V = L* di/dt, where L is the inductance of the ground line and di/dt is the rate of change of current in the ground line. Simultaneous switching noise can be reduced by lowering the ground line inductance. Packages with a high pin-count usually have a large internal ground plane, so their grounds have a low inductance. **Figure 19** shows the multi-layer structure of an FC-BGA. Simultaneous switching noise can be further reduced by inserting a bypass capacitor between the power and ground lines.

Crosstalk noise is caused by the influence of inductance and capacitance between adjacent signal lines. Crosstalk can be reduced by shortening signal lines and inserting a ground line between signal lines where necessary.

Another important point that must be considered is that conductor resistances, reflections due to mismatched impedances, and dielectric losses all reduce the energy of a signal.

From the above discussion, a package for high-speed signals has to satisfy following specifications:

- Impedance should be kept constant at 50 ohms throughout the signal transmission paths. Strip structures within a package and flip-chip bonding are suitable regarding this requirement.
- Low dielectric constant materials and low-resistance materials such as glass ceramic and organic materials with Cu wiring should be used.
- The power and ground lines should have a low level of simultaneous switching noise. This requirement necessitates the use of a multi-layer structure.

To summarize this chapter, it can be said that the FC-BGA is the most suitable package for high-speed LSIs.

6. Conclusion

Many CSPs have been developed recently for mobile devices. Design emphasis has shifted away from reducing the size of CSP packages and is now focused on improving electrical performance, reliability, and cost effectiveness.

A new packaging technology called “MCP,” which places multiple chips in a single package, has great potential in electronic devices.

The pursuit of packages with higher and higher performances continues. Especially, network equipment is becoming more important. Also, the importance of electrical simulation and measurement is increasing.

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