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Process Technologies for SOCs

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This paper introduces a family of process technologies for fabriating high-performance SOCs. These technologies can be used to embed digital and analog elements and memory such as SRAMs, ROMs, DRAMs, and flash EPROMs. Currently, any macro cell, except a flash EPROM, can be integrated on a silicon chip using the developed 0.25 μm and 0.18 μm process technologies. Although it is currently very difficult to assure full compatibility between flash EPROMs and other macro cells, these technologies enable a flash EPROM to be embedded in certain 0.35 μm MCUs.

1. Introduction

Because of the miniaturization of transistors and interconnections, it is now possible to integrate more than 10 million transistors on a silicon-chip using 0.2 to 0.18 μm technology. This makes it possible to integrate many kinds of circuits and build very large systems on a single silicon chip called a "System-on-a-Chip (SOC)." To realize an SOC, many sub-systems called "macro cells" are separately developed and then integrated on a chip. Although SOCs have specific, proprietary purposes, the macro cells they contain are pre-designed modular elements that can be used in any SOC. Using macro cells therefore reduces development time and cost. However, when designing an SOC, it is essential that its component macros are inter-compatible. For example, once a macro cell has been verified in a purely digital SOC (i.e., an SOC containing only digital circuits and SRAM), the macro cell should be directly adaptable, with no further verification or tuning, in any other SOC, for example, an LSI containing embedded DRAM or analog macro cells.

Our process technologies are designed to satisfy the above requirement for the production of top-performance SOCs. In this paper, we introduce the features of some already available process technologies and some processing technologies currently being developed.

2. Basic concept of the process technologies

Figure 1 shows the basic process flow. The base-line process technology consists of a dual-gate CMOS with Co-Salicide and up to five metal interconnection layers, which is a sufficient number for purely digital LSIs. Optional process modules are prepared to add analog and DRAM elements for mixed signals and embedded high-density memories. Also, three kinds of gate oxides (GOXs) are available for different supply voltages, for example, for 1.8/3.3/5 V interfaces. All macro cells, except flash EPROMs, are fully compatible with the technologies. Although, as described later, it is very difficult to assure full compatibility of flash EPROMs with other macro cells, they can currently be embedded in a 0.35 μm MCU.

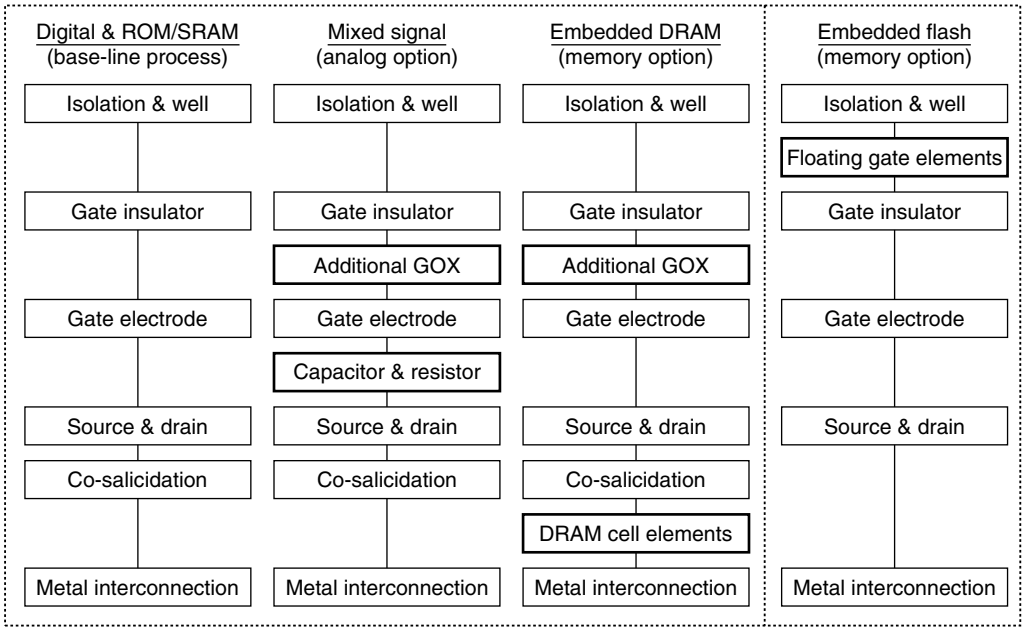


Figure 1
Process flow for SOCs.

Table 1
Main features and development schedule of the technologies.

		0.25 μm	0.18 μm	0.13 μm[note)]
Gate length (μm)		0.24	0.18	0.11
Tr. density (Tr./mm^2)		208k	440k	880k
Supply voltage	Internal	2.5 V	1.8 V	1.5 V
	High voltage	3.3/5 V	3.3/5 V	2.5/3.3/5 V
Power (/MHz BC)		0.05 μW@2.5 V	0.01 μW@1.8 V	0.003 μW@1.5 V
Gate delay: tpd (ps)	Inverter R/O	37	29	20
	2NAND R/O	45	36	26
SRAM cell size (μm^2)		12	4.9	2
DRAM cell size (μm^2)		0.96 to 0.62	0.37 to 0.25	< 0.2
Analog		2.5/3.3 V	1.8/3.3 V	2.5/3.3 V
Mass production	Pure logic Emb. DRAM	Jun. 1998 Sept. 1999	Oct. 1999 Jun. 2000	1st qtr. 2002 1st qtr. 2002

note) 0.13 μm values are targets.

3. Features of the base-line technology[1)-3)]

The target specifications are set according to the SIA road map and the customers' needs. **Table 1** shows the main features and the development schedule of this family of technologies. Every generation, there is approximately a 30% reduction in the physical dimensions. This means that every generation, the density of transistors and memories doubles and the performance (power x delay) is improved by a factor of about 1/6. Two to three different supply voltages (VCCs) are made available in each generation by adopting two to three types of gate insulator. This versitility will be important for integrating digital CMOS and analog/interface circuits with a very low VCC.

Our SRAM cells are not the smallest in the world, but this is because we guarantee a very

Table 2
Electrical and physical design rules of the technology.

		0.25 μm	0.18 μm	0.13 μm[note)]
(Bulk process)				
Gate length	(μm)	0.24	0.18	< 0.13
Effective gate length	(μm)	0.18	0.13	< 0.09
Gate oxide (electrical)	(nm)	6	4	< 3.2
Supply voltage	(V)	2.5	1.8	1.2 to 1.5
Transistor (high Ion/low Ioff)				
NMOS Vth(@Ids = 0.1 μA/μm)	(V)	0.3/0.45	0.2/0.35	0.18/0.34
PMOS Vth(@Ids = 0.1 μA/μm)	(V)	−0.3/−0.45	−0.2/−0.35	−0.18/−0.34
NMOS Ids	(mA/μm)	0.65/0.53	0.66/0.54	0.76/0.59
PMOS Ids	(mA/μm)	−0.28/−0.24	−0.32/−0.24	−0.32/−0.24
Substrate		Epi	Epi	Epi (SOI)
Isolation		LOCOS	STI	STI
Gate oxide		Pure SiO	Pure SiO/ON	ON
Exposure technology		KrF	KrF	ArF
Gate process		Normal	Half-tone + OPC	Half-tone + OPC
Source & drain		CoSi	CoSi	CoSi
(Interconnection process)				
Metal layers		5 Al	5 Al	7 Cu
Interlayer dielectric(k)		USG(4.1)	USG(4.1)/LowK(3.0)	Low-k(2.5 >)
Via filling		Blanket-W	Blanket-W	Cu dual damascene
Planarization technology		HDP + CMP	HDP + CMP	Low-k + CMP

note) 0.13 μm values are targets.
Terms: SOI: silicon on insulator, LOCOS: local oxidation of silicon, STI: shallow trench isolation
OPC: optical proximity correction, USG: un-doped silicate glass

fast operation of up to 770 MHz.[3)] The DRAM cell size has been gradually decreased to provide stable shipment at an early stage of mass production and a very high density and low cost at the peak stage of mass production.

Table 2 shows the electrical and physical design rules. Two types of transistors are available to meet various requirements: a high drain current (Ion) and a low off state leakage (Ioff). **Figure 2** shows Ion-Ioff relations for the 0.25 μm and 0.18 μm technologies. Even though the supply voltage is decreased every generation, the transistor driving current is kept the same. As mentioned above, there is approximately a 30% reduction of physical dimensions every generation, which is almost the same as the reduction rate in the SIA road map for achieving target performance. STI has been introduced in the 0.18 μm technology. Silicon oxi-nitride (ON) will be introduced in the 0.18 μm embedded DRAM and the

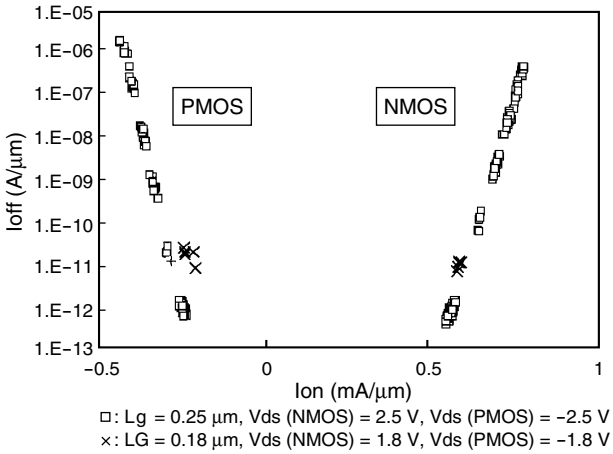


Figure 2
Ion-Ioff relations for various Vt control dosages.

0.13 μm base-line technology to prevent boron penetration from the PMOS gate electrode to the channel. The combination of a high-density plasma (HDP) oxide and chemical mechanical

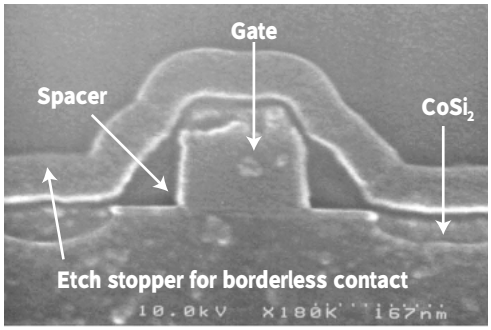


Figure 3
Cross-sectional SEM of 0.18 μm transistor.

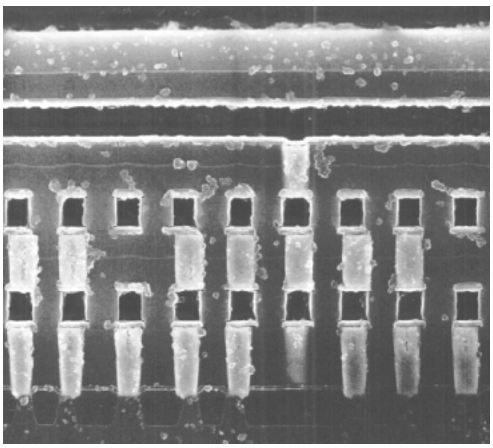
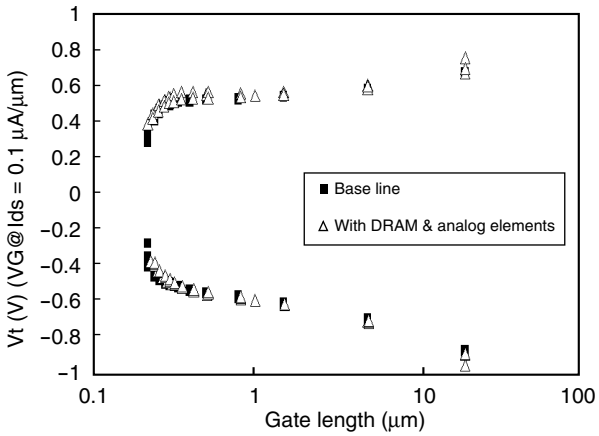


Figure 4
Cross-sectional SEM of 0.18 μm interconnection.



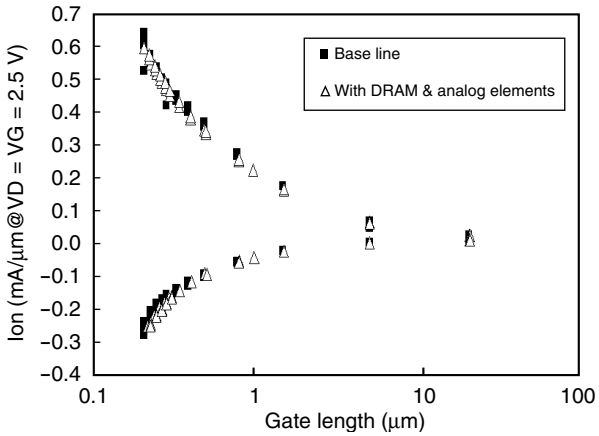


Figure 5
Vt/Ion versus gate length in macro cells with and without analog and DRAM elements: 0.25 μm technology.

polishing (CMP) has been adopted, starting with the 0.35 μm technology for planarized interconnections. Low-k and Cu interconnections will be introduced, starting with the 0.13 μm technology.

Figure 3 shows a cross-sectional SEM of a 0.18 μm transistor. The structure has optimized source/drain extension regions under the side-wall spacer and normal Co-Salicide on the source/drain and gate silicon. A silicon nitride layer is formed over the Co-Salicide layer. Metal-1 contact etching is stopped at the silicon nitride layer, and then the silicon nitride layer is removed, providing a borderless contact to active regions. **Figure 4** shows a cross-sectional SEM of an interconnection. As can be seen, the stacked vias and borderless contacts are well formed. Tungsten plugs and Al-Cu sandwiched by TiN/Ti are used to prevent stress and electro-migration.

4. Compatibility between macro cells with and without optional elements

As mentioned above, the basic concept of the technology is that macro cells should be fully inter-compatible in any kind of SOC. To achieve this, the I/O electrical parameters of all macro cells, especially analog and DRAM macro cells, should be the same. **Figures 5** and **6** show the dependences of Vt and Ion on the gate length in macro cells with and without embedded analog and DRAM elements. The difference between

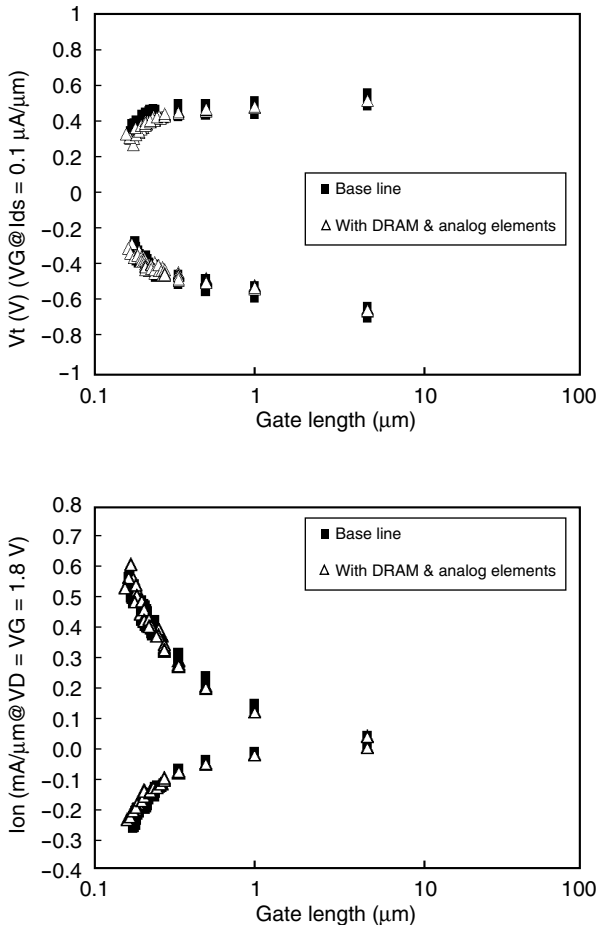


Figure 6
Vt/Ion versus gate length in macro cells with and without analog and DRAM elements: 0.18 μm technology.

the base-line and analog/DRAM-embedded technologies is small enough to assure full inter-compatibility of macro cells.

The key to achieving full inter-compatibility is how to form analog elements and DRAM stacked-capacitors with a lower thermal budget. After transistor formation, we use a maximum heat-treatment temperature of 700°C in the 0.25 μm technology and 650°C in the 0.18 μm technology. This prevents a degradation of transistor performance due to, for example, the penetration of gate boron into the channel, gate electrode depletion, and excessively deep junctions. The detailed process flow is described later.

Table 3
Main features and purposes of analog elements.

Transistor	
Normal transistor (2.5/3.3 V)	General use: e.g., for 10-bit 220 MS/s D/A for digital television.
• Low-Vt transistor	High-speed A/D, D/A
Capacitor	
• Double-poly	Linear (low ΔC-V), low stray capacitance: e.g., for 14- to 16-bit A/D, D/A for PDC base-band LSI.
• Poly-diffusion	Low cost: e.g., for general A/D, D/A.
Resistor	
• Silicided poly-Si	Low resistance for high-speed A/D: e.g., for 6-bit 500 MS/s A/D for digital video disks
• Poly-Si	Middle resistance for general A/D, D/A, etc.
• LDD diffusion	High resistance for biasing circuit, etc.
Triple well	VSS separation for low-noise applications

5. Key processes and features of embedded analog elements

Table 3 shows the main features and uses of the available analog elements. Two types of analog capacitors are available to satisfy various requirements: double poly-silicon capacitors for high accuracies such as a 300/ppm/V linearity and poly/diffusion capacitors for low-cost applications. There are three types of resistors: Co-silicided poly-silicon resistors for high-frequency operation and high accuracy; poly-silicon resistors for medium resistance values; and a high-accuracy, lightly doped drain structure (LDD) for low-cost purposes. The triple-well structure is available to electrically separate analog circuits from digital circuits and to minimize noise problems in analog circuits.

Figure 7 shows the process flow for forming a double poly-silicon analog capacitor. After poly-silicon is deposited on the gate insulator, silicon dioxide and poly-silicon are deposited by CVD. Then, the upper poly-silicon is patterned to form the upper capacitor plate as shown in Figure 7 (a). The lower poly-silicon is patterned to form the gate electrode of the logic transistor and the lower plate of the analog capacitor as shown in Figure 7 (b). After the transistor extension im-

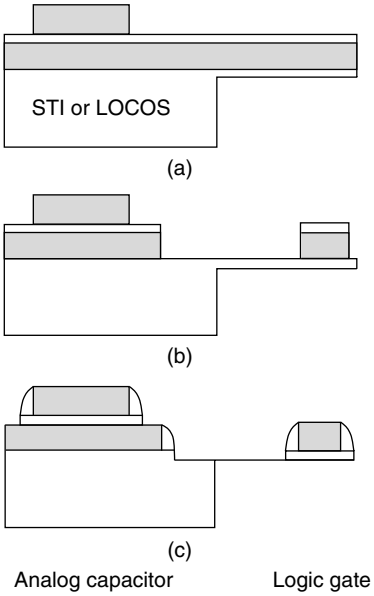


Figure 7
Process for double poly-silicon analog capacitors.

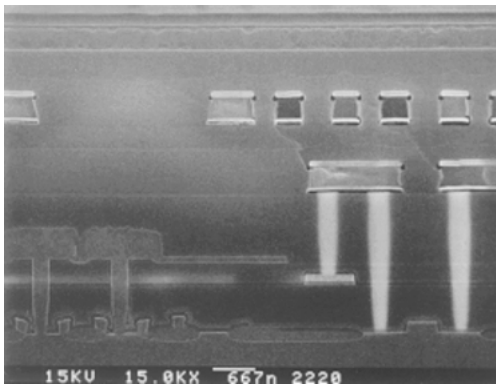


Figure 9
Cross-sectional SEM of 0.25 μm embedded DRAM.

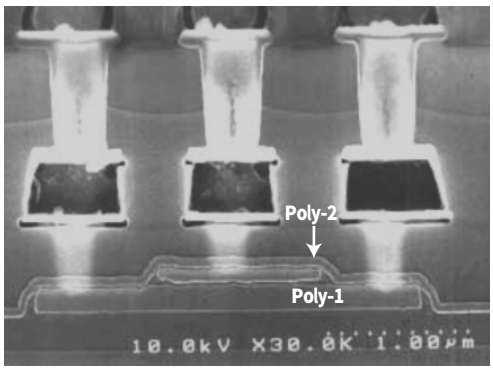


Figure 8
Cross-sectional SEM of double poly-silicon analogs capacitor.

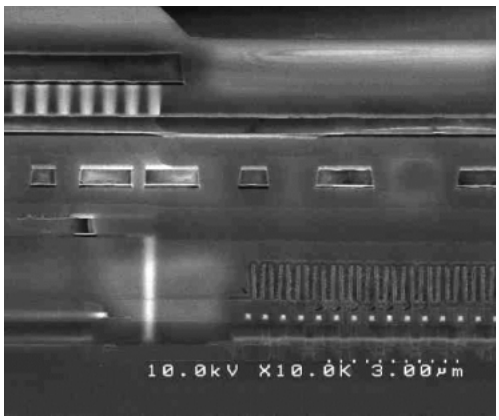


Figure 10
Cross-sectional SEM of 0.18 μm embedded DRAM.

plantation, a side-wall spacer is formed as shown in Figure 7 (c). Then, source/drain implantation and Co-Salicide formation are done in the normal way to complete the structures. The main advantage of this process is that the logic transistors are not affected by embedding analog elements, because the analog capacitors are formed before the transistor source and drain. **Figure 8** shows a cross-sectional SEM of a completed analog capacitor.

6. Key process and features of embedded DRAM

Figure 9 shows a cross-sectional SEM of a 0.25 μm embedded DRAM near the cell boundary. The 0.25 μm DRAM cell has stacked capacitors over poly-silicon word lines and tungsten polycide (WSi) bit lines. **Figure 10** shows a cross-sectional SEM of a 0.18 μm embedded DRAM. We adopted WSi for word lines and tungsten (W) for bit lines to decrease the resistance and reduce the number of word decoder and sense amplifier circuits. We

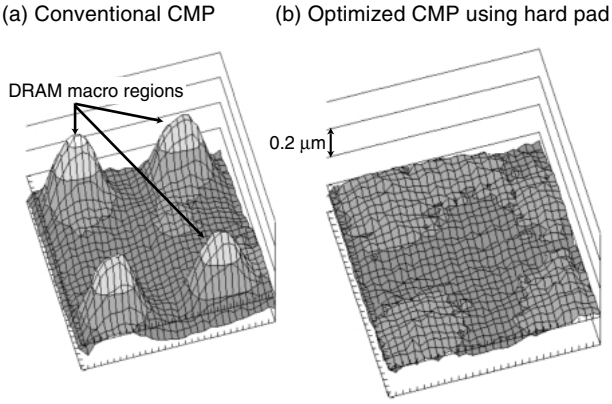


Figure 11
Global topographies of a 20 mm^2 chip after CMP.

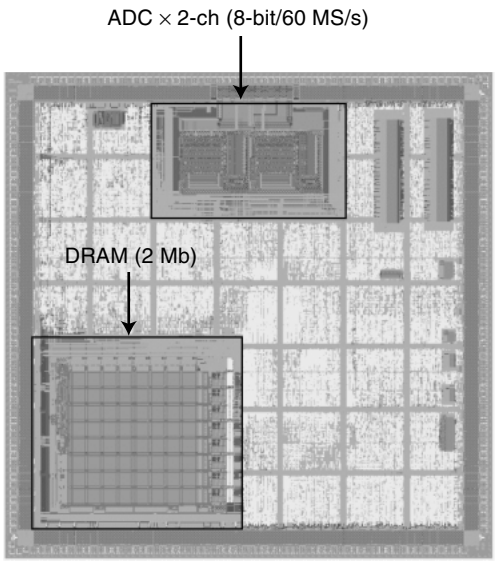


Figure 12
Photograph of SOC with embedded analog and DRAM macros.

also adopted cylinder type stacked capacitors to maintain the cell's storage capacitance.

Because adding a mask during the transistor side-wall formation degrades the refresh characteristics, there is no Co-Salicide in the DRAM cell area in the 0.25 μm and 0.18 μm technologies. The temperature of the heat treatment for forming the stacked capacitor has been decreased to 650°C by tuning the parameters of the in-situ doped poly-silicon and slightly oxidized silicon nitride.

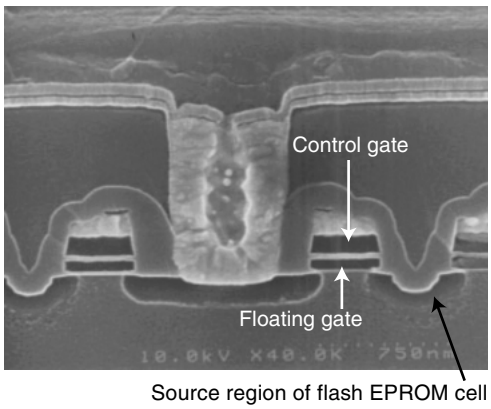


Figure 13
Cross-sectional SEM of 0.35 μm embedded flash EPROM.

To planarize the topography above the DRAM stacked capacitors and bit lines, the CMP pad condition has been optimized as shown in **Figure 11**. Because the surface is both locally and globally planarized, the depth of the metal-1 contact through-hole is increased. High-density plasma etching and CVD Ti and TiN are used to overcome the deep metal-1 contact problem.

Figure 12 shows a photograph of an SOC with embedded analog and DRAM macros and 120k-gate logic macros.

7. Key processes and features of embedded flash EPROM[4)]

Figure 13 shows a cross-sectional SEM of a 0.35 μm embedded flash EPROM cell. It is very difficult to embed a flash EPROM while maintaining inter-compatibility of macro cells. The reasons for this are that 1) although the thermal oxidation of the side surfaces of floating and control gates after source and drain implantation is essential for good retention characteristics, it also degrades the logic transistor; 2) a thicker side-wall spacer is needed for good retention characteristics, but this also degrades the logic transistor; and 3) the flash EPROM source region should be spread out under the floating gate to maintain good data erasing characteristics, but excess thermal treatment to spread out the source region degrades the logic transistor.

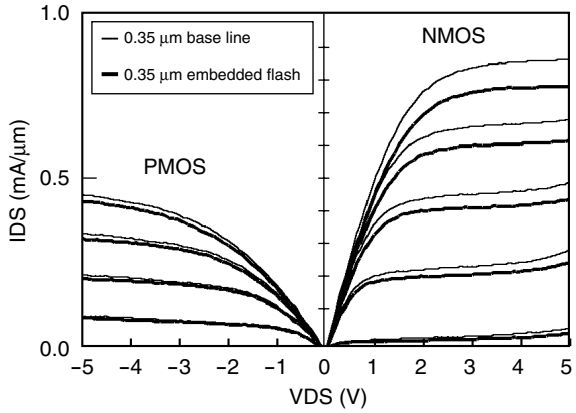


Figure 14
Transistor characteristics of embedded flash EPROM.

Figure 14 compares the characteristics of the transistors in the 0.35 μm embedded flash FPROM with those of the 0.35 μm base-line transistor. By careful optimization of the process conditions and the EPROM programming circuits, the deviation has been improved by 8% with no penalty in the flash EPROM characteristics. Although the flash EPROM is currently embedded only in specific 0.35 μm MCUs, we think we can overcome the above problems to make the flash EPROM fully inter-compatible with all other macro cells.

8. Conclusion

This paper introduced the main features of our process technologies for SOCs. Analog and DRAM elements have been successfully embedded in the base-line 0.25 μm and 0.18 μm technologies with full compatibility with other macro cells. A flash EPROM has been successfully embedded in specific 0.35 μm MCUs. The most important requirements are to reduce the thermal budget in optional process modules and planarize the topography above optional elements. Based on the experience we have gained in this work, we will further develop the process technology, not only to achieve further miniaturization and the best performance in the world, but also to embed fully compatible flash EPROMs and other elements.

References

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