UDC 621.3.049.771.14:621.377

Dual-Vth 0.25 μm CMOS Cells and Macros for 1 V Low-power LSIs

●Isao Fukushi ●Ryuhei Sasagawa ●Wataru Shibamoto

(Manuscript received December 8, 1999)

Dual-threshold-voltage (dual-Vth) 0.25 μm CMOS 1 V cells and macros were developed which use a low Vth MOSFET to achieve high speed at a low voltage and a high Vth MOSFET to keep the leakage current low in standby mode. The line-up of 1 V characterized logic standard cells, a fast signal level converter, a 1 V-to-1.5 V supply voltage converter, and a 1 V SRAM and 1 V ROM consume on average 1/5 of the power consumed by their equivalents in a conventional 0.25 μm 2.5 V CMOS library yet are only 50% slower and have almost the same amount of leakage current in standby mode.

1. Introduction

The low-power LSI is a key device in battery-operated portable equipment such as cellular phones and solid-state audio players. This equipment requires high-performance digital signal processing for the compression and expansion of voice and other audio signals. For any given LSI, a simple but effective way to reduce the power consumption is to lower the supply voltage (VDD) and clock-rate to the minimum levels that allow sufficient performance.

In a logic library for CAD synthesis and layout, which consists of components such as standard cell inverters and NAND and NOR gates, high-speed operation at low voltage helps reduce the power consumption. One way to attain high-speed operation at low voltage is to wait for the next generation of a migrated process that has improved MOSFETs. Another solution is to lower the MOSFET's Vth and accept the penalty of an increased leakage current. This involves a relatively easy process modification and is currently possible. The leakage current penalty can be eliminated by using multiple-threshold (MT) CMOS[1] or variable-threshold (VT) CMOS[2] circuit techniques with a standby mode control signal. After intensive study, for the logic part, we decided to use an MT-CMOS technique that uses low-Vth cells and high-Vth leak-cut switches. We developed a method in which conventional high-Vth cells can easily be converted to low-Vth cells. This method is described in Section 2.2.

When designing a 1 V-operated top core block for an LSI, we also need high-speed 1 V memory macros such as SRAM and ROM, a fast I/O level-converter that converts from 1 V to a higher voltage, and a voltage-up converter for memory macros. In these macros, low-Vth and high-Vth MOSFETs are used in different ways from MT-CMOS. The circuit techniques used here, including the MT-CMOS logic techniques, can be called "dual-Vth CMOS techniques." In the following sections, we describe the dual-Vth 1 V CMOS cells we have developed and some macros that are based on the techniques.

2. Standard logic cells for 1 V high-speed operation

A 0.25 μm dual-Vth logic cell library was developed to achieve high speed at the low VDD of

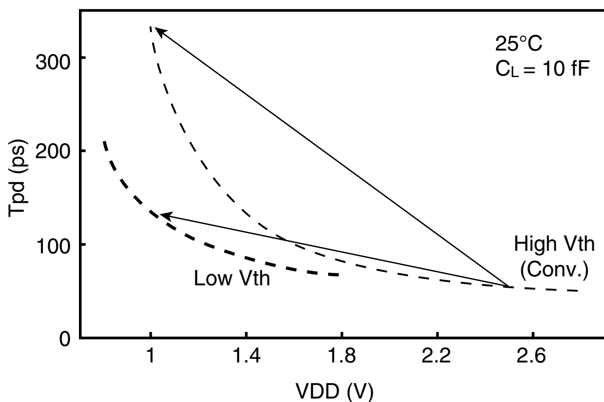

Figure 1
VDD dependence of delay in high-Vth and low-Vth inverters.

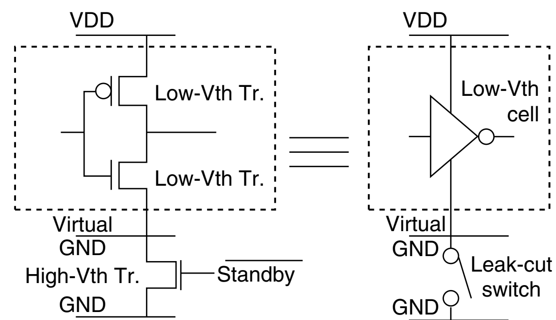

Figure 2
MT-CMOS basic structure.

Table 1
MOSFET characteristics.

	Low Vth	High Vth
pMOS		
Ids (μA/μm)	−57	−19
Vth (V)	−0.20	−0.55
Ioff (A/μm)	−8E−10	−2E−13
nMOS		
Ids (μA/μm)	152	47
Vth (V)	0.20	0.55
Ioff (A/μm)	6E−10	2E−13

(L = 0.25 μm Gox = 5.5 nm @Vds 1 V)

1 V. This library allows us to design 1 V-operated, low-power, high-speed logic circuits using conventional CAD tools and flows. **Figure 1** shows the cell delays of the high-Vth and low-Vth inverters according to HSPICE simulation. A conventional 0.25 μm library that uses a 0.45 V high-Vth MOSFET is best tuned for 2.5 V operation. Lowering VDD down to 1 V, which is below the standard voltage condition, drastically reduces operating power to 1/6 of that at 2.5 V; however, high-Vth MOSFET cells operated at 1 V are six times slower than they are at 2.5 V. A 0.2 V low-Vth MOSFET can be employed to improve the speed. This MOSFET operates only two times slower than conventional cells at 2.5 V. The low-Vth cell delay tables are tuned for a VDD of 1 V.

High-Vth nMOS leak-cut switches are also inserted between the low-Vth leaky cell block and GND to reduce the standby leakage power. This requires physical layout changes in the conventional library. Using a computer and a conventional library, one person completed the delay, power, and layout of a dual-Vth library of 350 cells in just three months.

2.1 Dual Vth CMOS process

Sub-quarter-micron MOSFETs have a drivability proportional to (Vgs – Vth), where Vgs is the applied gate-to-source voltage. This proportionality affects the cell delay. They also have an off current that is proportional to $10^{-Vth/S}$, where S is the subthreshold swing (S factor) and is around 80 mV/decade. This proportionality of the off current affects the standby leakage current. In conventional high-Vth MOSFETs, lowering VDD to around 1 V leads to a reduction of Vgs and causes a prominent speed degradation. To improve speed at a lower VDD without increasing the standby current, MT-CMOS[1)] was proposed. MT-CMOS uses a low-Vth CMOS for logic and high-Vth leak-cut switches inserted between the logic block's virtual GND and the GND power supply line, as shown in **Figure 2**. In standby mode, the /Standby signal goes Low and the high-Vth leak-cut switch maintains a very small leakage current. The MOSFET's characteristics are shown in **Table 1**.

The guidelines for the low-Vth and the power switch dimensions were studied. In consideration of the process fluctuation margins and temperature dependence, we decided on a low Vth

of 0.2 V. Then, after intensive study, we designed the leak-cut switches so that they have a drive current that keeps the virtual GND noise below 50 mV even at the onset of the CMOS switching current, which is estimated to have a current peak 10 times larger than the logic block's average current.

2.2 Low-Vth standard cells for MT-CMOS logic circuits

The conventional standard cells were converted to dual-Vth cells by one person in only three months, whereas creating entirely new standard cells would have taken five people three months. This big difference in work arises because the slight modifications in layout and delay calculations required for low-Vth MOSFET 1 V operation were mostly done by computer. The physical-layout files for placement and routing were used unchanged and were already certified in the CAD flow.

Starting with conventional 0.25 μm standard cells, we created low-Vth and high-Vth cells and characterized their delays and powers. In terms of changes in the physical layout, we removed the substrate-contact pattern when making the low-Vth cells from the conventional ones, as shown in **Figure 3**. This was done because the MT-CMOS requires a virtual GND line that is separated from the GND level in standby. If the substrate-contact was placed on the virtual GND line in each cell, it would have been short-circuited to the substrate GND level and the leak-cut action would not work. For the substrate contact of the low-Vth cells, an additional contact cell (Figure 3 right) was created and laid out at the power-supply line design phase for the floor plan as shown in **Figure 4**. This method allows us to keep the cell size exactly the same as the conventional cell size because the GND line patterns of a conventional cell can be used as the virtual GND. Moreover, placement and routing can be performed using conventional CAD tools by regarding the virtual GND as the conventional GND. For the high-Vth cells, we simply added a high-Vth dose layer to the conventional cells. These layout changes were performed with a CAD script and only took a few days.

The delay library of each low-Vth cell was characterized at 1 V. The power consumption at 1 V was reduced to 1/4 to 1/6 the power consumption of conventional 2.5 V VDD cells. The 350 low-Vth cells were therefore characterized at a Vth of 0.2 V and a VDD of 1 V to create a delay library and a power library. This characterization provides a precise delay library and is necessary for tuning low-voltage, high-speed logic circuits.

3. Custom macros

MT-CMOS outputs an uncertain logic level while in standby. This causes a transient current in pMOS and nMOS transistors that are in the on

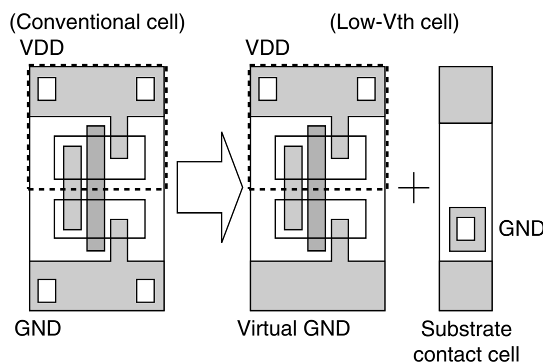

Figure 3
Making a low-Vth MT-CMOS cell.

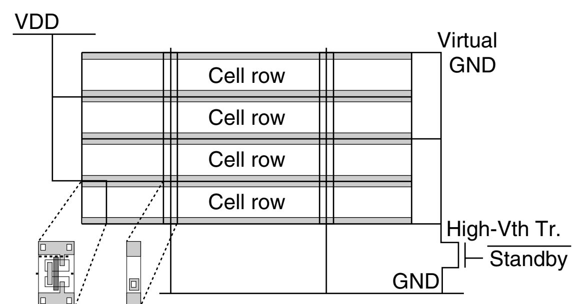

Figure 4
Layout of virtual GND lines and leak-cut switch MOSFET.

state in a receiver. Also, MT-CMOS needs a 1 V-to-2.5 V level converter to connect a standard I/O macro of an LSI. A fast level-converter with a standby clip was developed to meet these requirements. Also, to supply 1.5 V power for a SRAM macro, a high-efficiency voltage-up converter with a standby mode was developed. These two macros are indispensable for designing practical LSIs that have a low-voltage core.

3.1 Fast level-converter with standby clip

The 1 V MT-CMOS logic core must be connected to the existing conventional 2.5 V or 3.3 V I/O. A fast, dual-Vth 1.0 V-to-2.5 V level converter was developed. **Figures 5** and **6** show a conventional level converter and a new proposed one with a standby clip, respectively. In the conventional converter, a NAND control using a high-Vth MOSFET with a standby signal input is placed in front of a simple level-converter in order to suppress the input pMOS and nMOS transient on-current in standby mode. However, as shown in **Figure 7**, the circuit delay is significantly increased when VDD goes as low as 1 V. This is because a high-Vth inverter supplied at 1 V is used in the level converter. On the other hand, the proposed level converter shown in Figure 6 performs a NAND function at the 2.5 V VDD level-converter stage using low-Vth MOSFETs. As a result, as shown in Figure 7, the new converter has a 450 ps delay at 1 V and a reduced power consumption.

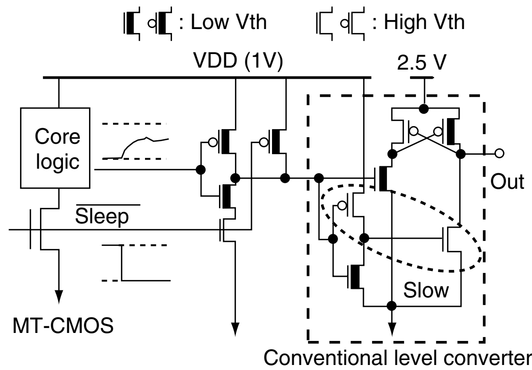

Figure 5
Conventional level conversion from MT-CMOS to high-voltage signal.

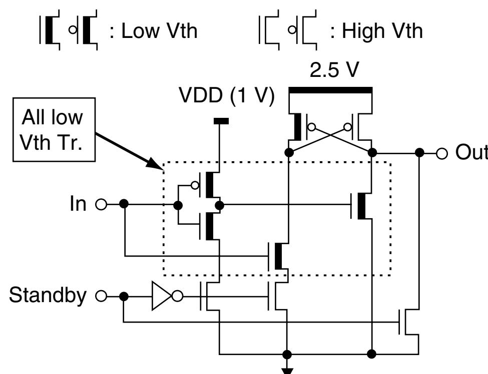

Figure 6
New level converter with standby clip.

3.2 High-efficiency 1.5 V voltage-up converter for SRAMs

Most LSIs need SRAMs. A 1 V, low-power 7.0 ns 2 Kw SRAM[3)] has been developed which needs a VDD of 1.0 V and a VDDH of 1.5 V. The VDDH word line and the BL precharge source levels enhance speed and maintain a low leakage current of 1 μW in standby mode. To generate VDDH from the supplied VDD, a 1.0 V-to-1.5 V voltage-up converter with an efficiency of up to 59% was designed. When this converter is incor-

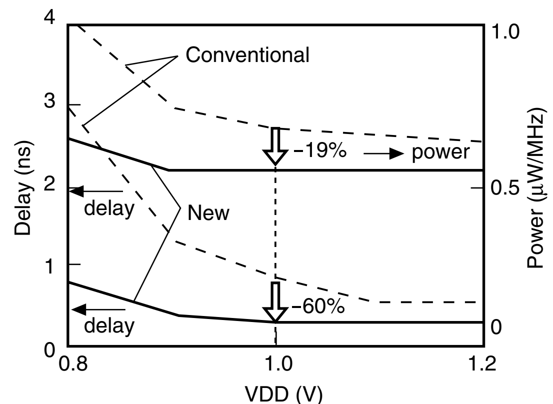

Figure 7
Delay and power consumption of conventional converter and new level converter with standby clip.

porated into the SRAM, the SRAM consumes 2.49 mW at 50 MHz and VDD = 1.0 V, which is less than the 2.68 mW consumed by the SRAM when a 1.5 V-to-1.0 V series regulator is used. The block diagram of this converter is shown in **Figure 8**. In the active mode, the VCO is controlled by the charge pump output to maintain it at 1.6 V and a regulated VDDH of 1.5 V ± 20 mV is supplied through the voltage regulator. The high efficiency is due to the cross-couple switches of the charge pump, which are gated above the 1 V level to avoid a Vth loss.[4] Using a large 1700 pF gate capacitance for high-speed load noise allows the voltage regulator and the VCO to operate slower at low power. In the standby mode, the VCO and the regulator are disconnected and turned off because they use current mirror comparators which consume roughly 200 µW. A slow ring-oscillator that operates at 10 MHz periodically activates the dynamic Vref generator[5] and the dynamic comparator in order to monitor the charge pump output and to impulse the charge pump when VDDH decreases. This scheme reduces the standby power to 11 µW to maintain VDDH at 1.6 V ± 50 mV when the load leakage is 1 µA. **Figure 9** shows the active mode efficiency versus load current when the load is a 50 MHz SRAM.

4. Low-power 1 V SRAM macro

Reducing the power of SRAM macros is also necessary for low-power LSIs. We therefore focused on reducing the total cell read current of the SRAM. To reduce the cell read current, it is advisable to use a divided word line structure that activates only a single cell for each I/O bit and a column-pitch sense amplifier (S/A) such as the one used in a DRAM. To obtain this column-pitch S/A, it is also desirable to use the minimum gate length of the applied technology, although this causes a threshold voltage mismatch between the MOSFET pair in the S/A. We therefore designed a new charge transfer S/A for the SRAM that can compensate for the threshold voltage mismatch.[3]

4.1 Concept of charge transfer pre-sense

Figure 10 shows the concept of the charge transfer pre-sense amplification.[6] A key device in this amplifier is an nMOS FET (CT in the fig-

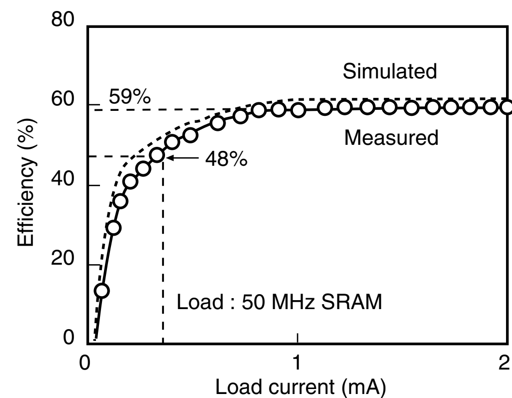

Figure 9
Active mode efficiency of voltage-up converter.

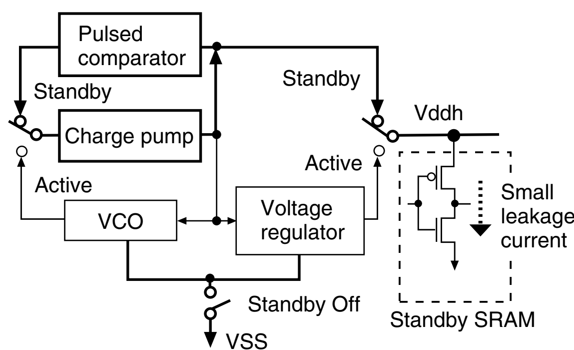

Figure 8
Voltage-up converter with standby mode.

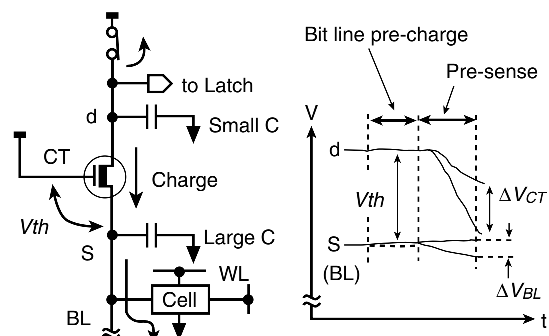

Figure 10
Charge transfer pre-sense amplification.

ure) with its source (s) connected to a bit line (BL). The drain (d) of the nMOS is connected to a switch for pre-charging. The operation is as follows. During the BL pre-charge phase, the switch is turned on and the CT allows the BL voltage to rise until it reaches (supply voltage – Vth), where Vth is the threshold voltage of the CT. Then, in the pre-sense phase, the switch is turned off and the word line (WL) is set to a high voltage. When the BL voltage starts to fall, the CT begins to turn on and transfers the charge from the drain to the source. The voltage of the drain falls much faster than the BL voltage because the capacitance of the drain is much smaller than that of the BL.

There is an identical circuit on another BL whose level is not lowered by the cell. On this side, the voltage of the drain is lowered slowly by the CT's leakage current because the CT has not completely finished its pre-charging. As a result, the voltage difference between the two drains (ΔVCT) is much larger than the BL drop (ΔVBL). After the charge transfer pre-sense, the latch amplifier amplifies the voltage difference, ΔVCT, to full-swing.

4.2 Vth mismatch-free charge transfer sense amplifier

Figure 11 (a) shows the new charge transfer S/A. In this amplifier, the CTs perform charge transfer pre-sensing and are configured as a cross-coupled latch.[7] If the two CTs have different Vth values, Vth1 and Vth2, the BL voltages are set at the respective beginning point of charge transfer in the pre-sense phase. As a result, the amplifier compensates for the Vth mismatch in the pre-sense phase.

Figure 11 (b) shows how Vth mismatch affects the S/A in the latch phase. The pre-amplified voltage difference, ΔVCT, is already established between the two drains. Also, the source voltages already have a difference of ΔVs = |Vth1–Vth2| + ΔVBL, where ΔVBL is the BL voltage drop caused by cell access. Therefore, the latch operation is also free from the Vth mismatch between the MOSFETs.

4.3 Features of SRAM macro

Using the new charge transfer S/A, a 2K × 16-bit SRAM macro was designed with the dual-Vth 0.25 μm process. **Figure 12** shows a photograph of the SRAM; it measures 1.80 × 0.73 mm^2.

The access time of this SRAM is 7.0 ns at a power supply voltage of 1 V at 85°C. The access time at 85°C is only 6% slower than that at 25°C and is consistent with the temperature dependence of the MOS Ids characteristics. At 50 MHz, the SRAM consumes 1.95 mW at a VDD of 1 V and a VDDH of 1.5 V. The boosted voltage, which is used in S/As, word lines, and leak-cut switches, is supplied by the previously described voltage-up converter and is always kept 0.5 V higher than

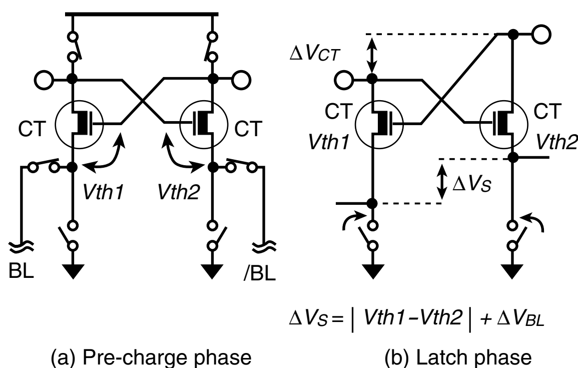

Figure 11
Vth mismatch in cross-coupled CT amplifier.

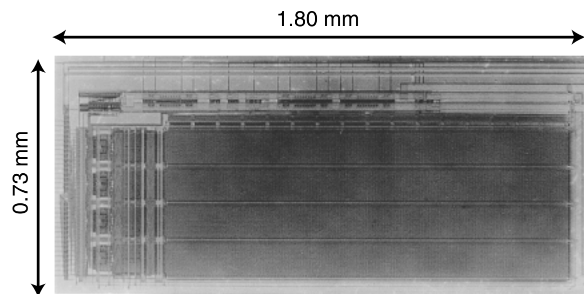

Figure 12
Photograph of SRAM macro.

Table 2
Main features of SRAM macro.

Cell size	3.2 × 5.5 µm²
pMOS width	0.75 µm
Driver nMOS width	1.5 µm
Access nMOS width	0.75 µm
Metal	2-layer
Organization	2K × 16-bit SRAM
Macro size	0.73 × 1.80 mm²
Supply voltage	1 V (Boost: 1.5 V)
TAA	7.0 ns
Power	1.95 mW @50 MHz
Cell power	5% of total power
Leakage power	1 µW in standby

VDD.

By using the divided word line structure and charge transfer S/A, the cell read power has been reduced to only 5% of the total power. All peripheral circuits of the SRAM employ the dual-Vth CMOS circuit. On the other hand, the memory cells consist of high-Vth MOSFETs to reduce the leakage current in standby mode. The SRAM achieves a low leakage power consumption of 1 µW in standby mode. The main features are summarized in **Table 2**. Compared to the conventional SRAM at 2.5 V, the new SRAM at 1.0 V consumes 1/4 of the power and operates at half the speed.

5. ROM macro

Contact-programming mask ROMs are accommodated in LSIs for the boot sequence and lookup code tables.[8)-10)] Compared with logic circuits, in memory macros such as SRAMs and ROMs it has been more difficult to lower the supply voltage (VDD) while maintaining high-speed operation. This is because these macros have an analog S/A. This chapter presents a novel sensing scheme for operating a ROM quickly at a low VDD. We have developed 2K × 16-bit and 4K × 8-bit ROM macros using a dual-Vth CMOS 0.25 µm technology.[11)] At 25°C, 1.0 V, and 50 MHz, the access time and power consumption are 7.0 ns and 1.4 mW, respectively.

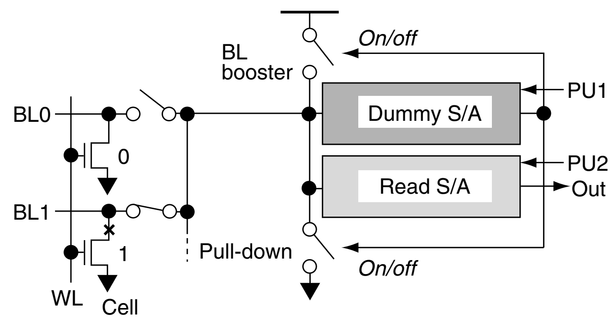

Figure 13
Self-controlled pre-charging sense circuit in the ROM.

5.1 Self-controlled pre-charging scheme for sense amplifiers

When the programmed data is read, the sense amplifier (S/A) of a ROM amplifies the small bit-line (BL) swing driven by the cell to the VDD output swing. Thus, a high-speed S/A is an important requirement in a low-power ROM.

In the conventional low-power sensing scheme of a ROM, multiple BLs are connected to a sense circuit and only one BL is selectively pre-charged, while the others are left at 0 V.[8),10)] When the selected BL is charged to a sense level only slightly higher than the threshold of the S/A, the BL level can easily be pulled down below the threshold by the cell and the high-gain S/A can operate faster. We have developed an S/A in which a cell, a charge-transfer gate, and a pull-up pMOS have a cascode connection with a following inverter.[11),12)] This S/A has a threshold level sufficiently lower than 1/2 VDD, which leads to a reduction in pre-charging current.

Precise precharge level control is essential for utilizing a high-gain cascode S/A, and it is necessary to pin the BL level quickly to the sense level. However, when programming a 0, the cell transistor's drain contacts the BL, and its diffusion capacitance is added to the BL capacitance. The more 0-programmed cells there are per BL, the larger the BL capacitance and the longer it takes to charge the BL to the sense level.

Figure 13 shows the block diagram of the sense circuit using a self-controlled pre-charging

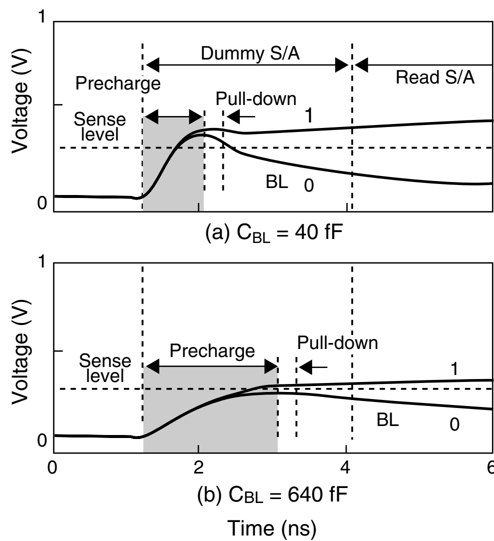

Figure 14
Waveforms of bitline pre-charge by dummy S/A feedback.

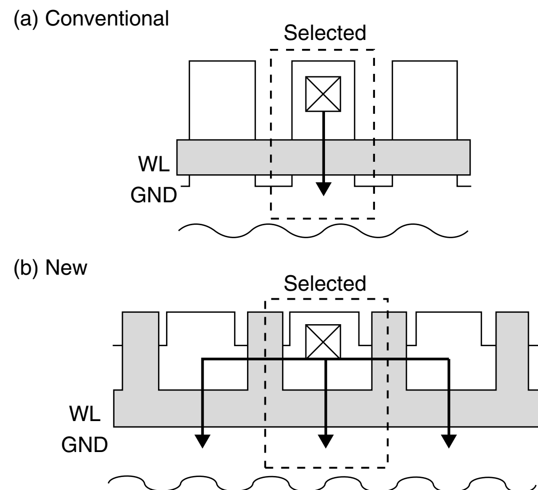

Figure 15
ROM cell patterns of conventional and new cells.

scheme. The sense circuit consists of a read cascode S/A, a dummy cascode S/A, a BL booster, and a pull-down circuit. First, the dummy S/A is turned on by the control signal PU1 and the BL booster starts to charge the BL rapidly. The dummy S/A is a replica of the read S/A; it monitors the BL level and turns the BL booster off when the BL reaches the sense level. When the BL capacitance is large, the dummy S/A delays the completion of pre-charging as shown in **Figure 14**.

The pull-down circuit is on only while the BL booster is being switched off and compensates for the excess pre-charge level of the BL induced by the feedback delay. After the BL booster is turned off, the BL level is pulled down by the cell by a 0-read or is weakly charged by the pull-up pMOS of the dummy S/A by a 1-read. Then, the read S/A is turned on by the control signal PU2, turning the dummy S/A off, and the output of the sense circuit responds.

A series of these self-controlled pre-charging operations minimizes the effect of the variation of the pre-charge level on the BL capacitance and provides high-speed sensing.

5.2 ROM cell layout for current enhancement

A ROM's cell current should be large enough to avoid sensing errors at a low VDD. However, it is difficult to enhance the current by lowering the Vth of the cell transistor because the leakage current should be kept small. Without the boosted high-voltage WL to simplify the circuit, one solution is to increase the channel width of the cell transistors with little increase in cell area.

Figure 15 shows the layout patterns of contact-programming NOR-type mask ROM cell arrays of conventional cells and the new proposed cell. For low-power sensing, only one BL is selectively pre-charged, while the others are left at 0 V. The WL of our new cell has a branch between neighboring cells, and the cell current is enhanced by the additional current path between the selected BL and the next cell. In 0.25 μm technology, the cell current of the improved cell can be more than twice that in the conventional cell with only a 20% increase in area.

5.3 ROM macro performance

We have developed 4K × 8-bit and 2K ×

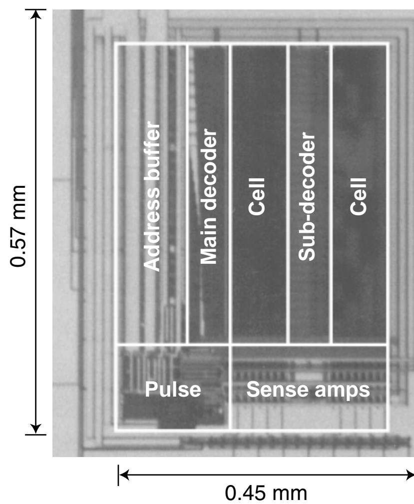

Figure 16
Photogragh of ROM macro.

Table 3
Main features of ROM macro.

Cell size	1.45 × 1.10 μm²
Metal	2 layers
Organization	2K × 16-bit/4K × 8-bit ROM
Macro size	0.45 × 0.57 mm²
Supply voltage	1.0 V
TAA	7.0 ns (2K × 16-bit)/6.9 ns (4K × 8-bit)
Power (50 MHz)	1.4 mW (2K × 16-bit)/1.1 mW (4K × 8-bit)

16-bit ROM macros. **Figure 16** shows a photograph of the 4K × 8-bit ROM; it measures 0.45 × 0.57 mm². **Table 3** summarizes the main features of the ROM. The access time and power consumption of the 2K × 16-bit ROM at 25°C, 1.0 V, and 50 MHz are 7.0 ns and 1.4 mW, respectively. The ROM consumes half the power of the conventional ROM at 2.5 V but is only 2.3 times slower. These macros operate down to 0.8 V.

6. Summary

Dual-Vth 0.25 μm 1 V low-power CMOS macros were developed. Using the dual-Vth CMOS process, 350 low-Vth logic cells for MT-CMOS were created and characterized at 1 V. A fast signal-level converter, 1 V-to-1.5 V supply-voltage converter, 1 V SRAM, and 1 V ROM were also developed. Compared to the components of a conventional 0.25 μm 2.5 V CMOS library, all of these components consume an average of 1/5 of the power, operate at half the speed, and have almost the same amount of leakage current in standby mode.

References

1) S. Mutoh, S. Shigematsu, Y. Matsuya, H. Fukuda, T. Kaneko, and J. Yamada: A 1V multithreshold-Voltage CMOS digital signal processor for mobile phone application. *IEEE JSSC*, **31**, pp.1795-1802 (Nov. 1996).
2) T. Kuroda, T. Fujita, S. Mita, T. Nagamatsu, S. Yoshioka, K. Suzuki, F. Sano, M. Norishima, M. Kurota, M. Kato, M. Kinugawa, M. Kakumu, and T. Sakurai: A 0.9V, 150 MHz, 10 mW, 4 mm², 2D discrete cosine transform core processor with variable threshold voltage (VT) scheme. *IEEE JSSC*, **31**, pp.1770-1779 (Nov. 1996).
3) I. Fukushi, R. Sasagawa, M. Hamaminato, T. Izawa, and S. Kawashima: A low-power SRAM using improved charge transfer sense amplifiers and a dual-Vth CMOS circuit scheme. Symp. VLSI Circuits Dig. Tech. Papers, June 1998, pp.142-145.
4) P. Favrat, P. Deval, and M. J. Declercq: A high-efficiency CMOS doubler. *IEEE JSSC*, **33**, pp.410-416 (Mar. 1998).
5) H. Tanaka, Y. Nakagome, J. Etoh, E. Yamasaki, M. Aoki, and K.Miyazawa: Sub-1mA dynamic reference voltage generator for battery-operated DRAMs. *IEEE JSSC*, **29**, pp.448-453 (Apr. 1994).
6) L. G. Heller, D. P. Spampinato, and Y. L. Yao: High sensitivity charge-transfer sense amplifier. *IEEE JSSC*, **SC-11**, pp.596-601 (Oct. 1976).
7) M. Izumikawa and M. Yamashina: A current direction sense technique for multi-port SRAMs. I*EEE JSSC*, **SC-31**, pp.546-551 (Apr. 1996).
8) T. Shiraishi, K. Kawamoto, K. Ishikawa, H. Sato, F. Asai, E. Teraoka, T. Kengaku,

H. Takata, T. Tokuda, K. Nishida, and K. Saitoh: A 1.8V 36 mW DSP for the half-rate speech CODEC. Proceedings of IEEE CICC, 1996, pp.371-374.

9) H. Takahashi, S. Muramatsu, and M. Itoigawa: A new contact programming ROM architecture for digital signal processor. Symp. VLSI Circuits Dig. Tech. Papers, June 1998, pp.158-161.

10) W. Lee, P. E.Landman, B. Barton, S. Abiko, H. Takahashi, H. Mizuno, S. Muramatsu, K. Tashiro, M. Fusumada, L. Pham, F. Boutaud, E. Ego, G. Girolamo, H. Tran, C. Lemonds, A. Shih, M. Nandakumar, R. H. Ekiund, and Ih-Chin Chen: A 1 V programmable DSP for wireless communications. *IEEE JSSC*, **32**, pp.1766-1776 (Nov. 1997).

11) R. Sasagawa, I. Fukushi, M. Hamaminato, and S. Kawashima: High-speed cascode sensing scheme for 1.0 V contact-programming mask ROM. Symp. VLSI Circuits Dig. Tech. Papers, June 1999, pp.95-96.

12) R. J. Baker, H. W. Li, and D. E. Boyce: CMOS – Circuit Design, Layout, and Simulation. IEEE press, 1998, pp.506-510.

Isao Fukushi received the B. S. degree in Applied Physics from Tohoku University, Sendai, Japan in 1982. He joined Fujitsu Ltd., Kawasaki, Japan in 1982, where he developed high-speed ECL/BiCMOS SRAMs for supercomputers. In 1994, he transferred to Fujitsu Laboratories Ltd., Kawasaki, Japan, where he has been researching low-power, low-voltage LSI design. Currently, his main area of research is low-power embedded SRAMs. He is a member of the IEEE.

Ryuhei Sasagawa received the B. S., M. S., and Ph.D. degrees in Electronic Engineering from the University of Tokyo, Tokyo, Japan in 1990, 1992, and 1999, respectively. In 1996, he joined Fujitsu Laboratories Ltd., Kawasaki, Japan, where he has been engaged in research of low-power, low-voltage CMOS for SRAMs and ROMs embedded in VLSIs. He is a member of the IEEE, the Japan Society of Applied Physics (JSAP), and the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.

Wataru Shibamoto received the B.S. and M.S. degrees in Electrical Engineering from Tokyo Institute of Technology, Tokyo, Japan in 1994 and 1996, respectively. In 1997, he joined Fujitsu Laboratories Ltd., Kawasaki, Japan, where he has been researching low-power CMOS circuits for VLSIs.