

# Low Power Consumption Digital Signal Processor: Hi-Perion

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**A low power consumption 16-bit fixed-point Digital Signal Processor (DSP) was developed for mobile handy terminals. Two MACs are employed and operated alternatively. This architecture enables high-speed processing at a low supply voltage, effectively reducing operating power. Compatibility of the firmware is maintained. An experimental chip consumed 11 mW at a 1.2 V  $V_{dd}$  when the PSI-CELP CODEC firmware was run at 40 MHz.**

## 1. Introduction

Because of its excellent characteristics, digital signal processing technology is widely used in many areas of consumer electronics, for example, communications, audio, and servo control. A DSP is a special processor that efficiently handles digital signal processing. The programmability of a DSP also makes it more advantageous than hard-wired logic devices in terms of the time to market. DSPs have the advantages of real-time processing and low power consumption compared to a general-purpose MPU. This makes them indispensable, especially for mobile handy terminals, which must operate at a low power consumption to increase the battery lifetime.

We have developed a 16-bit low power consumption DSP called "Hi-Perion" that is capable of processing the voice signals of PDC terminals and W-CDMA terminals. The Hi-Perion series provides an evaluation chip and hardware/software tools for program development. The series also provides a System-on-a-Chip (SOC) that has an embedded DSP core and other dedicated circuits.

## 2. Architecture

The block diagram of the DSP we developed

is shown in **Figure 1**. It consists of a DSP core and peripheral circuits. The basic architecture is an improved Harvard architecture, which is a very simple structure for minimizing power consumption. This DSP has an instruction word length and data word length of 16 bits. The instruction set has been designed for digital signal processing and includes instructions such as dual-data move, ALU with saturation, and a loop instruction and the instructions for processing Viterbi decoding in channel decoding. The instruction memory and data memory each have a 64K-word space.

### 2.1 DSP-CORE

The core consists of units for clock generation, sequence control, data-address generation, and bus interface and the data ALU unit.

The clock generation unit generates the system clock. The DSP has a power-saving sleep mode which stops the system clock. The DSP exits the sleep mode immediately after an interruption request occurs. The power consumption in sleep mode is 0.78 mW at 1.2 V and 40 MHz.

The sequence controller unit controls the program flow of the branch, loop, repeat, and other

instructions. With its two repeat counters (REP and REP2), the DSP can execute a single repeat instruction nesting in a block repeat loop. By replacing the three-cycle branch instruction with a repeat or loop instruction, the one or two cycles required for counter and loop size settings can be eliminated, thereby improving performance.

The data-address generation unit has eight 16-bit registers (X0 to X7) for the address pointer. The unit generates two data addresses simultaneously. The address pointers are updated according to an immediate value from -3 to +3 or an update value held in 16-bit registers Y0 and Y1. Thus, a wide range of updates is covered. The address pointers also handle the operation for circular addressing by setting start point = BV width = MD to any section. The pointer value is folded and is returned automatically by hardware within the range of the specified address when an updated pointer value exceeds the range. When

digital filtering is running, this operation improves the efficiency of processing and data memory usage.

The bus interface unit interfaces the peripheral circuits with the DSP core. This unit can insert a wait cycle to prevent a memory access conflict.

The data ALU unit has register files, an ALU, a barrel shifter, and a multiply-accumulator. A register file is composed of two 32-bit registers (AX, BX) and two 40-bit accumulators (CX, DX). These can be used as eight 16-bit registers. The 40-bit barrel shifter performs an arithmetic shift or a logical shift to the left or right by one cycle. The accuracy of the sum-of-products operation is  $40b = 16b \times 16b + 40b$ .

The multiply-accumulator is based on the Dual MAC architecture. The hardware and sequence difference in the sum-of-products processing from the previous DSP is absorbed by an instruction decoder and a sequencer, for example,

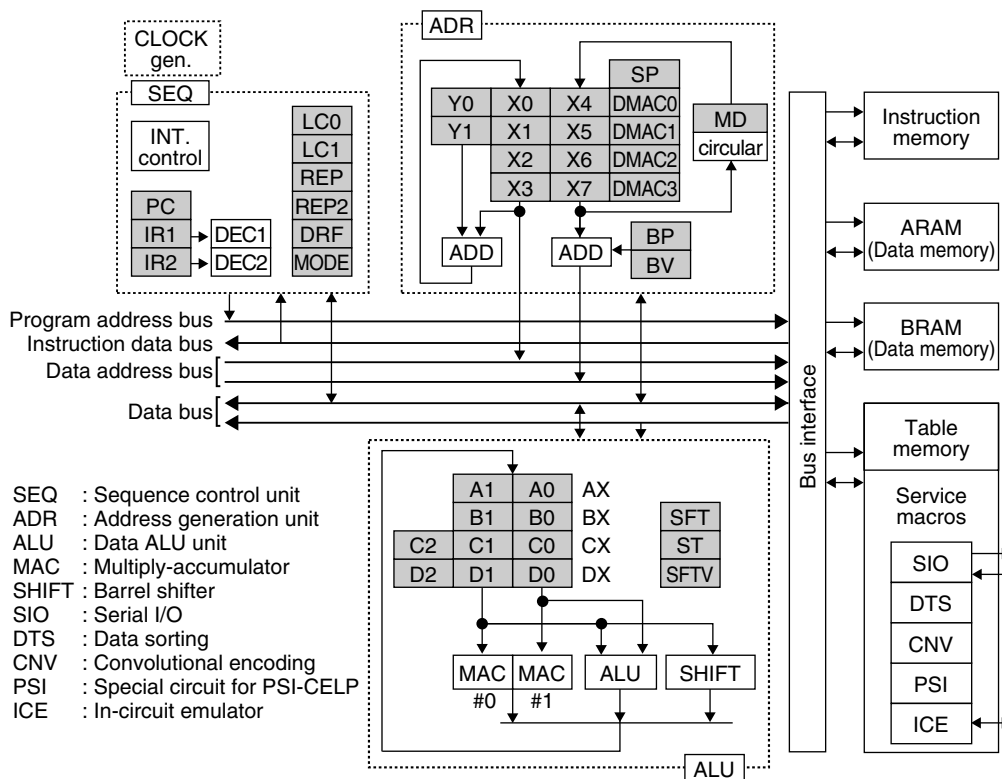


Figure 1 DSP block diagram.

an interlock system. Therefore, the firmware written for the single Mac architecture can be directly executed in this DSP. This Dual Mac architecture, in which two MACs operate alternately, can be handled almost the same as a single Mac architecture in firmware coding by the programmer. This will be explained in detail later.

### 2.2 Peripheral circuits

The peripheral circuits are an instruction memory, data memory, PLL, and the service macros. This chip is an evaluation chip for firmware development, so it has embedded SRAMs for the instruction and table memory. (On an SOC, such as one for mobile handy terminals, the DSP core has ROMs for the instruction and table memory.) In the peripheral circuits, data memories are connected with three buses that are independent of each other. Therefore, in the case of a double data load operation, two data sets from ARAM, BRAM, or Table RAM can be simultaneously moved to the registers in the DSP core in one cycle.

For standard service macros, the peripheral circuits include a serial I/O circuit that interfaces between internal data and external asynchronous data and an in-circuit emulator (ICE) that interfaces with external ICE equipment.

### 3. Power reduction

Power consumption can be reduced by reducing the circuit scale, decreasing the operation frequency, or supplying the lowest voltage possible. Reducing the supply voltage has immediate results and is the most effective of these three methods.<sup>1),2)</sup> The key point for achieving a low power consumption DSP with this strategy is to have a high processing performance at a low supply voltage. Therefore, a mechanism is required to maintain a high processing performance while overcoming the circuit delays that are common with a low supply voltage. Also, in conventional power reducing methods, the circuit scale and frequency are reduced. Because reducing the scale

of the most frequently switched circuit is effective, we reduced the scale of the core circuit. Further reductions in power consumption were obtained by using dedicated service macro circuits and adding special instructions to reduce the required number of processing cycles so that the operating frequency could be reduced or the stand-by duty increased.

### 3.1 Improved operation frequency

The maximum operation frequency of a DSP is limited by the critical path, which is the instruction with the longest processing time. The processing times of each instruction are different, so the higher speeds of some instructions are wasted. However, the operation frequency can be improved if instructions with long processing times are handled as two-cycle instructions. The relative processing times of the instructions are shown in **Figure 2**. The processing times of the sum-of-products instruction and the 40-bit addition instruction are especially long, but the processing times of the other instructions are well balanced. Therefore, the execution cycles of the sum-of-products and 40-bit addition were handled

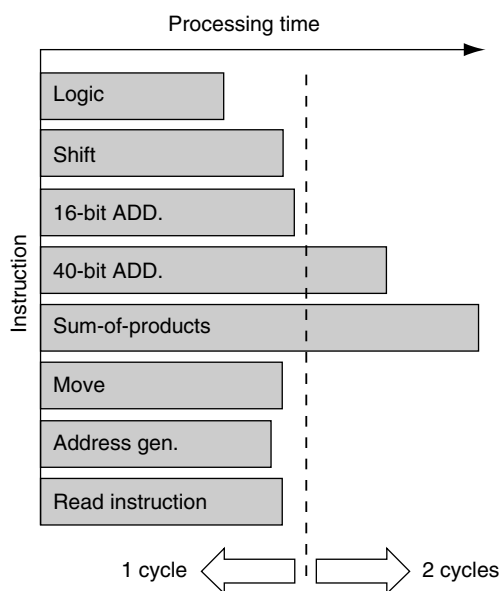


Figure 2 Processing times of instructions.

in two cycles and the remaining instructions were handled in single cycles. This resulted in about a 41% reduction in the cycle time compared to when the sum-of-products operation was handled in a single cycle.

### 3.2 Pipeline structure

The coexistence of two-cycle and single-cycle instructions is controlled as follows. As shown in **Figure 3**, the basic pipeline phase is composed of five stages. In the PC stage, the instruction code from the instruction memory is read and stored in the instruction register (IR). In the DEC stage, the instruction code in the IR is decoded and control signals connected to each circuit block are generated. In the ADR stage, addresses for the memory or I/O are generated. In the EX1 stage, a one-cycle instruction is executed. The one-cycle instructions are the move, 16-bit ALU, and shift instructions. Two-cycle instructions are executed using both the EX1 and EX2 stages. The two-cycle instructions are the multiplication, sum-of-products, and most of the 40-bit ALU instructions except for the shift instruction.

Two kinds of pipeline hazards can occur in

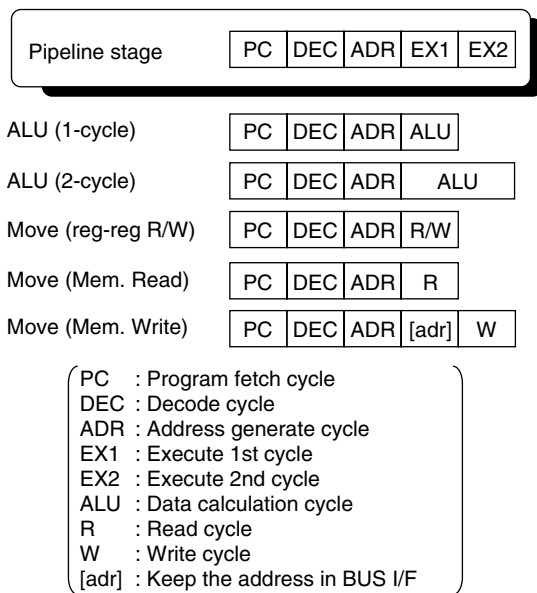


Figure 3 Pipeline structure.

this pipeline structure. One kind is a register conflict between a two-cycle instruction and a one-cycle move instruction. The other kind is a memory conflict in which data is written to a memory space and then read from that space in the same cycle. The hardware avoids both of these conflicts by inserting a wait cycle and then accessing the data in the next cycle. Therefore, the programmer need not consider pipeline hazards when coding.

The number of execution cycles for the branch instruction was three cycles, although the pipeline has five stages. The next two instructions on a branch out and branch through destination are fetched ahead of the condition being judged.

### 3.3 Dual MAC operation at low supply voltage

The sum-of-products is the most frequent operation in digital signal processing.

The processing performance of the sum-of-products operation is improved by installing two or more multiply-accumulators and operating them in parallel.<sup>3)</sup>

Executing a sum-of-products operation in two cycles improves the clock frequency and the performance of other processing. However, the performance of signal processing would decrease if the frequently executed sum-of-products operation were simply adjusted to two cycles. Therefore, in this DSP, there are two multiply-accumulators that are controlled alternately. As a result,  $n$  sum-

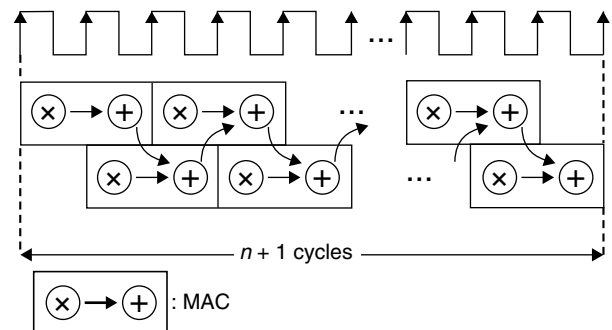


Figure 4 Continuous  $n$  sum-of-products in  $n + 1$  cycles.

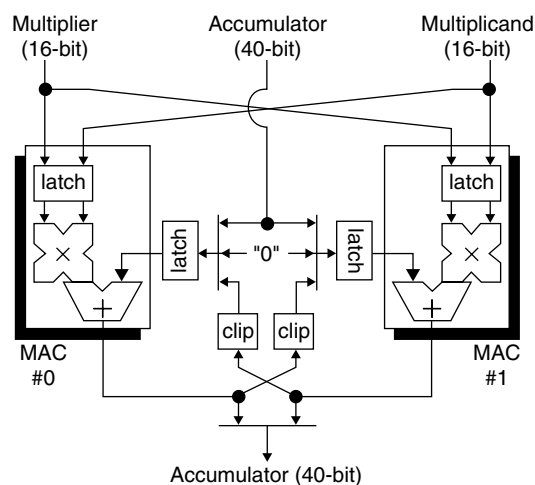


Figure 5  
Dual MAC block diagram.

of-products operations are continuously executed in  $n + 1$  cycles (Figure 4).

The block diagram of the Dual MAC operation is shown in Figure 5. Each multiply-accumulator completes its operation in two cycles. A pair of multiplier data and multiplicand data is loaded from memories every cycle. Then, the data pair is fed to MAC#0 in one cycle and to MAC#1 in the next cycle. After the two cycles, the two completed results are stored in the accumulator and then sent directly to another multiply-accumulator. Because of this by-pass configuration, the accumulated data need not be brought through the accumulator again. The accumulated results can be accumulated immediately on the other side of the multiply-accumulator. This results in continuous high-speed sum-of-products operation.

### 3.4 Circuit scale reduction

Verilog-HDL was used in the design of this DSP, and the net-list was generated by RTL coding and logical synthesis. The logical synthesis was conducted with an area reduction constraint and a speed constraint. Depending on the efficiency and performance of the synthesis, the area has a tendency to increase when the speed constraints are made more strict. Therefore, it is difficult to obtain both a high speed and small area.

Moreover, the critical path should be optimized for a specific number of logical gate steps and a specific load capacity. However, because detailed tuning is difficult in logical synthesis, we divided the block into a data path part, in which the speed was constrained, and a random logic part, in which the area was constrained. The RTL for the data path block was coded so that only the expected net-list was synthesized. The data path net-list was optimized manually while considering the number of logical steps and the load capacitance. Then, several kinds of soft macros were prepared to describe the RTL so that the target net-list was synthesized almost uniformly. The random logic block net-list was synthesized from the RTL with the area constrained.

At the beginning of the DSP design, the main decoder was an independent module, so instructions were decoded in a centralized way. However, the number of control signals generated with the decoder exceeded 250 and the amount of wiring between modules grew. Therefore, we used a local decoding method and each module has its own decoding circuit.

The above measures reduced the circuit scale of the core by about 16% and improved the operation speed of the chip by about 21%. To examine the effect of the circuit scale reduction on the power consumption, the power consumption was estimated by a gate-level power simulation. Part of the PSI-CELP CODER program was used for the estimate. According to the simulation, the power consumption was reduced by 15% and the circuit scale was reduced by 16%, which is an almost proportional relationship.

### 3.5 Performance improvement by service macros

To reduce the power consumption, it is also important to reduce the number of processing cycles for applications. Because the frequency of the system clock can be decreased, operating at a lower voltage becomes possible. This DSP has extended instructions for Viterbi decoding and

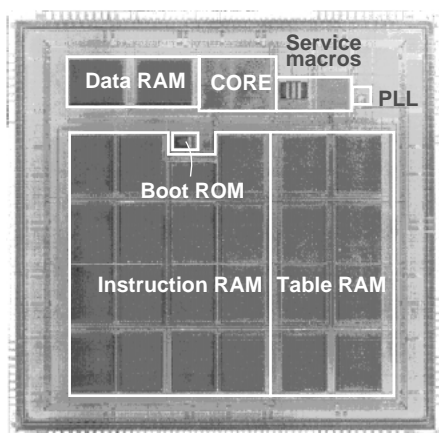


Figure 6  
Photograph of the chip.

Table 1  
Features of the DSP.

Power consumption	11 mW@1.2 V, 40 MHz
Technology	0.25 $\mu$ m CMOS 1-poly, 3-metal
Die size	Chip : 9.11 mm $\times$ 8.41 mm Core : 1.48 mm $\times$ 1.00 mm
Number of transistors	Core : 188.3 kTr ROM : 2K-word $\times$ 16-bit RAM : 102K-word $\times$ 16-bit
Memory	6.4K-word $\times$ 8-bit
Package	208-pin QFP, 3.3 V I/O

small-scale hardware in its peripheral. The peripheral circuits have a great impact on reducing the number of processing cycles because they assist in program processing and execute hardware processing concurrently with the operation of the core.

The peripheral circuits include a data sorting circuit (DTS) which arranges data in ascending or descending order automatically, a CNV circuit which executes convolutional encoding for channel encoding, and a PSI circuit specialized for the PSI-CELP of PDC which assists the codebook search function.

#### 4. Experimental results

The chip photograph of the developed DSP is shown in **Figure 6**, and some of the chip's fea-

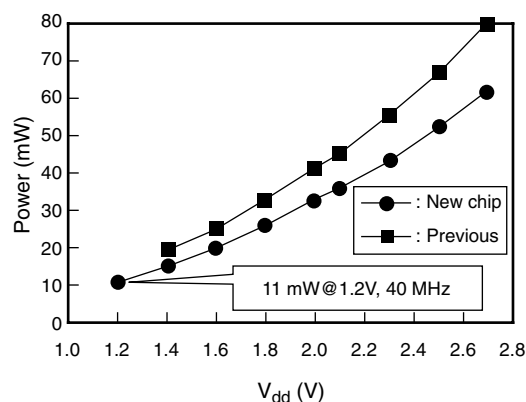


Figure 7  
Power consumption.

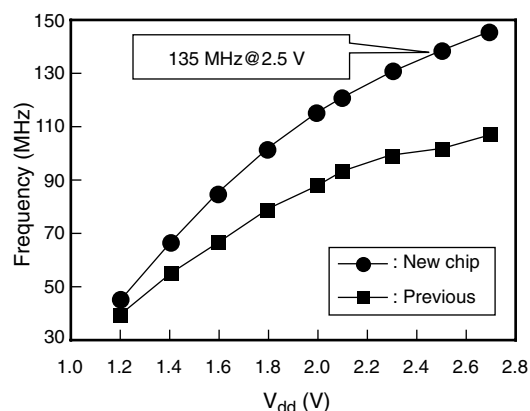


Figure 8  
Operating frequency.

tures are shown in **Table 1**. This DSP was fabricated experimentally with a 0.25  $\mu$ m CMOS process. The DSP operates stably at 40 MHz and a supply voltage of 1.2 V. **Figure 7** shows the power consumption when the PSI-CELP CODEC is executed at 40 MHz. The lowest power consumption at a supply voltage of 1.2 V was 11 mW. The DSP can operate at the high frequency of 135 MHz at a typical supply voltage of 2.5 V (**Figure 8**). The DSP features both a low power consumption and a high performance.

#### 5. Conclusion

A low power consumption DSP (16-bit fixed-point) was developed for mobile handy terminals. To obtain a high processing performance at a low supply voltage, instructions that require a long

processing time were changed into two-cycle instructions. To improve the throughput for the sum-of-products operation and to maintain the compatibility of the firmware, a Dual MAC architecture that consists of two multiply-accumulators operating alternately was adopted.

## References

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