IPHighway: Infrastructure for IP Macro Distribution

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Recent sub-micron technology has made it possible to realize system LSIs which integrate various system functions. However, system-level integration brings enormous difficulties to LSI designers. It has been pointed out that the reuse of IP macros is a very effective way to overcome these difficulties. This paper describes the issues that are necessitating the reuse of IP macros and our IPHighway system, which we have constructed internally for promoting the reuse of IP macros. Also, recent activities in the industry for distributing IP macros between companies are described.

1. Introduction

1.1 Shift to system LSIs

The steady advance of semiconductor technology has managed to meet the market demands for higher performance, lower power consumption, more sophisticated, and lower-cost LSI devices. Integration of logic LSI devices has been increased by 58% per year (approximately a four-fold increase every three years), and it is expected that the integration will continue to be improved at this rate in the future. Now, with the recent mainstream 0.18 µm technology, logic elements of up to 20 million gates and memory elements of up to 128 Mb can be integrated into a single LSI device. This new level of integration makes it possible to integrate the functions needed for DVD and DSC equipment into a single chip. The system LSI (System-on-a-Chip [SOC]) and system level integration will become a reality in the near future.¹⁾

1.2 Design crisis

One of the most significant challenges for LSI designers is finding a way to design and verify an LSI device containing such a large amount of elements. **Figure 1** shows the number of elements

that can be integrated into a single chip and the person-hours required to design such chips (this figure is provided by SIA). According to this road map, as the number of elements that can be integrated into a chip increases, the number of person-hours required to design a chip using those elements becomes bigger and bigger. It is expected that thousands of person years per chip will be required in 2001 unless a major breakthrough is achieved in this area. It will therefore be virtually impossible to fully exploit the progress that has been made in process technology unless there is a major innovation in design methodology.

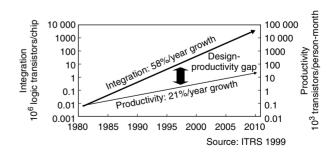


Figure 1 Design productivity versus integration scale.

2. Reuse and distribution of IP macros

2.1 Importance of IP macros

The best way to solve this design crisis is to design and verify the functional blocks in an LSI device as macros that are recognized as containing intellectual property (IP) and to reuse these macros – referred to as IP macros – for faster and more reliable design work. By reusing predesigned and verified functional blocks whenever possible, it is possible to reduce risks in system LSI development.

System LSIs can contain multiple IP macros for various functions, for example, a CPU, memory blocks, and function blocks for implementing industry standards such as USB; key functional blocks such as MPEG and JPEG blocks; and mixed signal blocks such as ADC and DAC. Recently, many innovative technologies, for example, Bluetooth and USB, have been proposed and are being realized one after another. LSI designers need to use these new technologies in their LSI design work so they can promptly meet the needs of their customers. However, it is not possible for a single designer to learn such extensive techniques and implement these functions in an LSI device. In the development of a system LSI, therefore, it is necessary for the designer to construct a horizontal co-working relationship with third parties in which the designer can focus on developing the functions that are unique to the LSI and to procure functional blocks from sources having the required skills and then integrate them into a chip.

In addition, to reuse IP macros, it is necessary to establish innovative design methods such as system-level design, timing design, hardware/ software co-design, and formal verification. Many semiconductor vendors and EDA tool vendors are putting a lot of effort into developing new methods. We think that the design and development period can be reduced by half by reusing design resources that are available from both inside and outside the company and by creating new design methods for system LSIs.

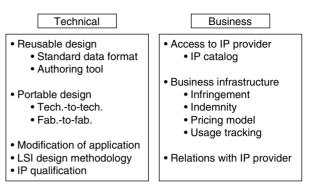


Figure 2 Factors affecting IP reuse.

2.2 Problems with reuse and distribution of IP macros

Design resources can be reused at several levels. The initial level is to reuse resources within the same department. At this level, the provider and user of the IP macros share some of the information about the state of development, technologies, and use. Also, at this level, face-to-face communication is possible. Therefore, there are no significant difficulties as long as the documents are filed. At the second level, IP macros are shared between departments. At this level, both parties have little information in common and the design methods may differ from department to department. Therefore, it is necessary to carefully file the documents, unify the design rule, and collect information such as which IP macros are available. At the third level, IP macros are shared among companies. This level of reuse is performed in the form of IP macro trading among third-party IP providers, ASIC vendors, and system vendors. Particularly, more and more third-party IP providers are providing attractive IP with original architectures and are stimulating innovations in system LSI design. In addition to technical problems, IP trading between companies brings up legal and business problems regarding the guarantee of performance and functions, handling of infringements of the rights of third parties, and the license model. The factors that affect IP distribution are listed in Figure 2.

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iane I	PID Company/Compan_	Company (Division)	Function(Larg_	Function/Medium	Function/Detail	
POOREC	Fujitou Limited	Logic LSI Group/LSI Products	NCU	RUSC	32bit	
PCORE1	Fujiteu Limited	Logic LSI Group/LSI Products	NCU	RISC	3267	
POORE3	Fujitau Limited	Logic LSI Group/LSI Products	MOU	RISC	3257	
POORE4	Fujitou Limited	Logic LSI Group/LSI Products	NOU	RISC	32bit	
	English Deta[Register NewSPOORE1]					
				_		
	1PID					
	IP Name SPOORE1					
	Operation Condition	Technology CAD Tool	Deliverables 1	Option Busines	a Condition] User Si	
	Company			Performance]	Physical Specificat	
	Large Category MCL		Bus Width 32	bit E	quivalent Product	
	Midium Category RISC	• •	ache Size 8	KB	MB95632	
	Detail Category 325r	* *	(encrybit)	E F	FD Size	
	Other Category	_	(emory/word)	N	unter of channels	
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According to Dataquest's survey of LSI developers, they expect that 30% of the area of chips in 2000 will be IP – the figure for 1998 was 20%. It is therefore expected that design resources will be reused more and more.

3. IPHighway system

3.1 Constructing the IPHighway system

Based on the above discussion, as a first step we constructed an infrastructure for promoting the reuse of IP macros on the IPHighway intranet. The primary purpose of the IPHighway is to share the IP macro information that is maintained and developed by Fujitsu's LSI development group, which includes subsidiaries located all over the world. By using this system, the developers can easily retrieve various types of information such as what is available in Fujitsu, what features an IP has, and the person/s who should be contacted in order to obtain an IP.

3.2 Features of IPHighway system

Some of the features of the IPHighway system are described below.

• Easy registration of catalogs

We provide a Windows-based editor specially designed for catalogs (**Figure 3**) so that catalogs can be easily created. The created catalogs can be easily registered as CSV files on the IPHighway by a single operation on a Web browser.

IP Outline Compared-lists					
n IPID	000010@ed intra fujtra	000011@ed.intra.fuitzu	000013@ed intra flajtru		
" IP Name	SPCOREC	SPCOREL	SPCORE3		
Company	Fujitsu Limited	Fujitau Limited	Fujitau Limited		
Division	Logic LSI Group)LSI Prod	hacts Logic LSI Group)LSI Products	Logic LSI Group M.SI Products		
Large Category	MCU	MCU	MCU		
Medium Categ	ary RISC	RISC	RISC		
* Detail Category	3200	32bit	3204		
Bit Width	32	32	32		
Compliance St	andard Integer UnitSPARC VSE	Integer UnitSPARC VIE	Integer UnitSPARC V8E		
* Equivalent Pro	duct MB86831	MB86832	MB86831		
Clock Frequen	cy(MIN) 66	40	66		
Clock Frequen	CY(MAX) 80	80	<u>80</u>		
LSI Vender na	me Fujtru Limited	Fujtru Limited	Faikes Limited		
" Technology Co	de CE61	CE71,CE61	CE61		
CAD Teol	LCADFE	LCADFE	LCADFE		
VSI Compliant	e YES	YES	YES		
Qualification L	evel Evaluated by MB86831	Evaluated by MB86832	Evaluated by MB86831		
" External Availa	ble 1998/08	1998/08	1993/03		
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Adoption of standard catalog specification

The catalog format we adopted conforms to the Reusable Application Specific Intellectual Property Developers (RAPID) specification. This is a standard, open specification which allows catalog information from a third-party IP provider and internal IP catalog information to be stored in the same database so that users can easily search and compare these two bodies of information.

Highly functional retrieval

By placing the registered catalogs into several classes, catalogs can be easily retrieved using class names. The approximately 80 information items used for catalog retrieval are categorized into six classes. The number of IP macro registration items in each class is displayed before retrieval, and various retrieval conditions can be entered. In addition, multiple catalogs that are hit in a retrieval are listed horizontally for each item (**Figure 4**) and the IP macro characteristics are displayed for comparison so that suitable IP macros can be easily selected.

• Security of IP macros

Each catalog can be classified as "Specified registrant only," "Specified user group only," or "Specified server only." Each technical document and piece of design data can be classified as "Specified user only" or "Specified user group only." By setting these levels, the required security can be

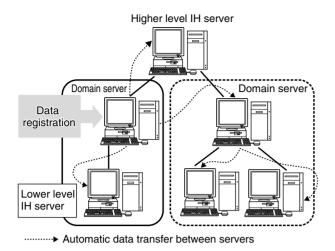


Figure 5 Automatic IP data exchange between IH severs.

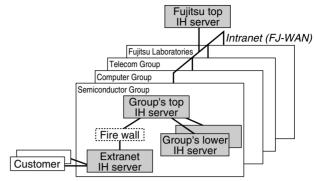
maintained for IP macros that are disclosed to the whole company.

Automatic updating of catalogs by server-to-server linkage

Multiple servers can be hierarchically organized, and catalogs are automatically transferred between the upper and lower servers. For example, when catalogs are disclosed to the upper server, they are automatically transferred to the lower servers (**Figure 5**). Therefore, catalogs can easily be disclosed to the whole company. Users in other departments can efficiently retrieve all the disclosed catalogs from their local servers.

3.3 Actual examples

The IPHighway was made available to the entire company on the Fujitsu intranet in August 1998. IP macro catalogs are registered by the development departments in Fujitsu and the third-party IP providers. At present, the catalogs contain information on about 300 types of IP macros. Of these about 100 are IP macros developed by Fujitsu and about 200 are IP macros provided by third parties. The IP macros developed by Fujitsu and the third parties can be retrieved and displayed for comparison at the same time from anywhere within Fujitsu. In addition, any available technical documentation and



IH server: IPHighway server

Figure 6 Structure of servers on Fujitsu Intranet IPHighway.

design data can be provided to designers. Currently, IP macro information that is provided from the semiconductor group is distributed to the information processing group, communications group, and laboratories for company-wide information sharing in Fujitsu.

The top server of each group is placed under the top intranet server of the entire company, and the lower servers are placed under each top server (**Figure 6**). The catalogs registered to a server are disclosed to a specific group or to the whole company. The catalogs disclosed only within a group are not disclosed to the other groups. By installing dedicated servers for the dealers on an extranet, IP macros developed by Fujitsu can be disclosed to outside the company.

4. Inter-company trading of IPs

Although operation of the IPHighway system within Fujitsu was started in 1998, many difficulties are expected to arise in the future when this system is used for IP distribution among companies. For example, the protocol for IP information exchange has not been defined, the formats of the data to be exchanged differ from company to company, and the security philosophy has not been decided. To solve these problems and establish an environment in which IP catalog information and design data can be exchanged between companies on the network without

Item	Comment
What to transfer	Catalog contents Documents such as datasheets and application notes Evaluation model IP design data such as RTL, test bench, and netlists
Security	During transfer: SSL Authentication: IP address, user ID & password Design data should be encrypted by IP provider
Format of catalog	Character set is ASCII Common language is English (Japanese option) Catalog items are compliant with VSIA with extension Catalog data format is original one based on CSV
Media	Internet
Data transfer/ exchange protocol	HTTP for transferring IP catalog and data SMTP for communication between servers

Table 1Consortium specification for IP information exchange.

difficulties, in May 1999 we established the IPHighway consortium together with Matsushita Electric Industrial Co., Ltd., Sony Corporation, Toshiba Corporation, and Mentor Graphics Japan Co., Ltd.

The activities of the IPHighway consortium include:

- 1) Establishing common specifications and techniques for IP macro information exchange (**Table 1**).
- 2) Developing software for IP macro information exchange based on the above specifications.
- 3) Checking the effectiveness of this technique by conducting an operational suitability test using this software.

We are willing to disclose the specifications for the inter-company information exchange conducted in these activities and to invite other companies to adopt this system. At present, the common specifications are fixed and the system development is under way. A trial test will be started in March 2000, and the results will be reported in September 2000. In addition, much effort has been made in the industry to invigorate IP trading among companies. The virtual component exchange (VCX) promoted by Scottish Enterprise intends to provide IP catalogs, define a standard IP licensing contract, and support settlements. The VSI Alliance, which is trying to standardize the IP design interface, is promoting the standardization of the contents and formats of IP catalog information to be exchanged among companies. In Japan, the Semiconductor Industry Research Institute Japan and other bodies are doing studies aimed at promoting IP distribution. We want to establish an infrastructure for IP distribution among companies as soon as possible. For this purpose, we will exchange information and promote cooperation with these other bodies.

5. Conclusion

System level integration brings various difficulties in system LSI development. LSI designers face higher risks and longer design turn-around times. To overcome these problems, the reuse of IP macros is a key requirement. Fujitsu has designed and constructed the IPHighway system as an infrastructure for the internal reuse of IP macros. Also, Fujitsu proposes an environment in which each company in the industry can easily exchange IP macros with the IPHighway system and is now collaborating with various entities in the industry to establish such an environment.

Reference

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er of the System LSI Development Labs., Fujitsu Laboratories Ltd., where he developed IPs such as low-power DSPs and IPs for MPEG2. He has also served as the General Manager of the Marketing Division, Fujitsu Ltd. and is the Vice Chairman of the IP Highway Consortium.