Preface
Special Issue on System-on-a-Chip (SOC)

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The continuous down-scaling of CMOS transistors has enabled ever-increasing numbers of transistors to be integrated on a single chip. Now, various kinds of functional blocks such as logic, memory, and analog blocks can be integrated on a chip called a System-on-a-Chip or SOC to build a system that formerly had to be realized on a printed circuit board. This feature of SOCs has been contributing to the power reduction, cost reduction, and miniaturization of various systems, especially mobile battery-powered systems.

The turnaround times for design and verification have become major obstacles in SOC development. In fact, the design methodology needs to be drastically improved to cover a system containing more than 10 million transistors. One way to overcome this design crisis is to construct a system from already existing IP macros. This method, which is called IP reuse, can drastically cut the development time and cost.

This special issue on SOCs describes the results of recent research on design methodologies, some key IP cores and circuit macros, and the infrastructure of device processes and packaging technologies for SOCs.

The first four papers of this issue cover design and verification methodologies. The first paper introduces the IP reuse approach for SOC design and the remaining three describe various verification methodologies for SOCs.

Next, we present four papers on processor cores for SOCs. The first of these describes a general-purpose embedded processor that has an enhanced performance due to its VLIW architecture. Then, the remaining papers in this section describe three special-purpose processing cores: a geometry engine for 3D graphics, an MPEG2 decoder for Digital TV, and a low-power digital signal processor (DSP) for cellular phones.

The next section contains three papers about circuit technologies. The first two papers describe a low-power scheme that uses dual-threshold-voltage transistors for portable battery-powered systems. The first paper describes the application of this scheme to a DSP for cellular phones and the second describes its application to low-power libraries. The third paper in this section describes a Gbit-rate parallel interconnect circuit macro that can drive twisted Cu wires with a low level of signal skew. This technique is expected to become very important in communications and information processing.

Lastly, we cover the infrastructure for SOCs, for example, module process approaches for implementing analog and DRAM elements on a chip and packaging techniques for miniatuarization and higher speeds.

The infrastructure for IP reuse for SOCs is rapidly being improved in both the business and CAD tool environments. For example, the world's first virtual component (IP) exchange market has recently been opened in Scotland and some CAD tool vendors have started to provide tools for quick IP verification and automatic IP redesign. These developments are bound to accelerate the worldwide SOC business.

We hope that this special issue will help readers grasp the various technical aspects of SOCs and help promote this new area of technology.