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Silicon Single-electron Memory Using Ultra-small Floating Gate

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A single-electron memory having a ultra-small floating gate on a narrow channel is studied theoretically and experimentally. This device is fabricated based on Si by using self-aligned process, and exhibits quantized threshold voltage shifts and hysteresis curves in the electrical characteristics at room temperature. These are basic operation of the single-electron memory. A novel method to form small metal dots is also developed. Sn nanocrystals are formed in thin, thermally grown SiO_2 layers by using low energy ion implantation followed by thermal annealing. Current-voltage characteristics of a diode in which Sn dots are embedded show a clear Coulomb gap and Coulomb staircases. These techniques are promising for making single-electron memories to be practical.

1. Introduction

Single electron memory is an ultimate device that can store one-bit information by charging an single electron. This device is one of promising candidates for basic elements of future electronics because its power dissipation is expected to be exceedingly small with a conventional semiconductor memory like a DRAM and a flash memory, which need to charge hundreds of thousands of electrons for one-bit information.

Single electron memories have been fabricated based on various materials such as GaAs and Al.[1),2)] The operation of these devices is limited at quite low temperature (~ 4. 2 K), however. To realize room temperature operation, reduction of the feature size down to nano-meter scale is necessary. Moreover, Si is preferable as a basic material from a practical point of view, thus mature fabrication technologies for large scale integration (LSI) circuits are available.

Recently, room temperature operation of a single-electron memory based on Si was achieved by applying nanometer-sized poly-Si fine-grains to a floating gate and a channel.[3)] With this device being sophisticated, an early prototype of gigascale single electron memories was demonstrated.[4)-6)] This device has difficulty, however, in controlling the size, number, and position of the poly-Si fine-grains, resulting in poor uniformity of the device characteristics. Hence, the technology to fabricate nanoscale features with precise control over their size and position is strongly required.

We developed a new Si single-electron memory having a ultra-small floating gate, what is called floating dot, stacked on a channel by a self-aligned process,[7)-8)] thereby the size and the position of the floating dot are precisely controlled. Similar devices have been reported by Guo[9)] and Welser.[10)] In this paper, the basic concept, the fabrication method, and the room temperature operation of this single-electron memory is reported. In developing single-electron memories, it is necessary to fabricate nanoscale structures in high throughput with good size and position uniformity. Hence, we describe a novel method that we

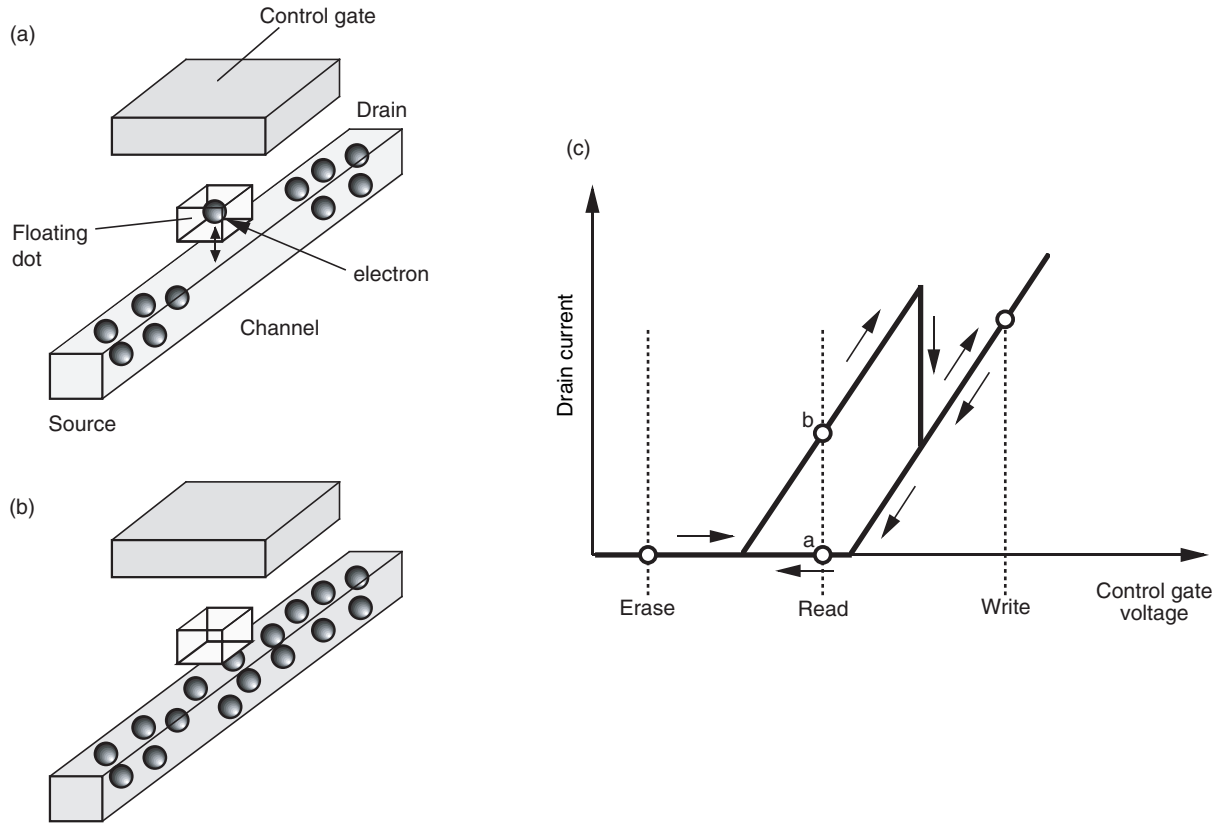

Figure 1
Operation principle of single-electron memories. (a) and (b) elucidate current modulation by charging or discharging single-electron, (c) drain current versus control gate voltage characteristics.

have recently developed to form nanoscale dots. This method satisfies these requirements.

2. Basic concept of single-electron memory

2.1 Operation principle

The single-electron memory we developed consists of a floating dot, where electrons are stored, and a narrow channel field-effect transistor (FET), which acts as an electrometer. **Figure 1** elucidates the device structure and its operation principle. An electron is transferred between the floating dot and the channel through a tunneling barrier by applying a proper voltage to the control gate. The current in the channel is modulated by charging or discharging a single-electron as shown in Figures 1 (a) and (b). If the control gate voltage V_g is increased gradually, the drain current I_d is decreased abruptly at a certain V_g due to charging an electron into the dot.This electron is discharged from the dot at a different V_g while V_g is decreased, and a hysteresis curve is consequently obtained in I_d versus V_g characteristics. Hence, the device can operate as a single-electron memory by settling suitable V_g for erasing, reading, and writing as shown in Figure 1 (c).

This operation principle is quite similar to that of a flash memory except a remarkable difference of the electron number in the dot, and the performance of the single-electron memory strongly depends on the minimum feature size. The controllability of the electron number in the dot and the capability to modulate the drain current by single-electron charging are particularly sensitive to the size.

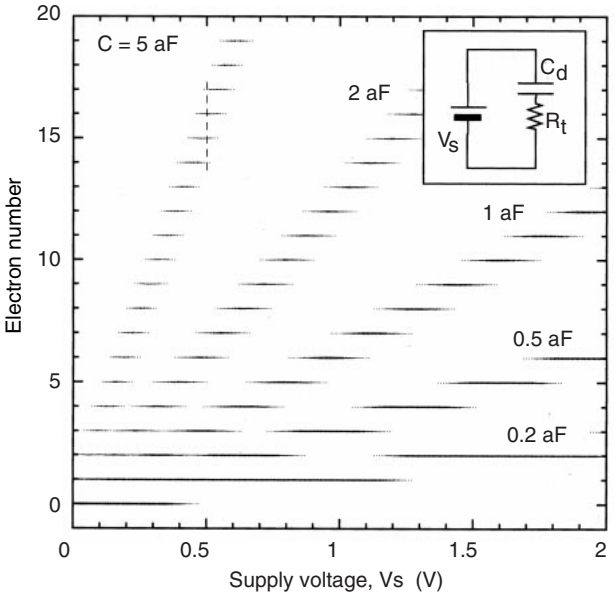

Figure 2
Behavior of stored electron number as function of supply voltage V_s.

2.2 Controllability of electron number

The controllability of the electron number can be estimated by calculating the electrostatic energy of the device.[11),12)] Here, employed for approximate estimation is a simple circuit model represented with the capacitance C_d, the resistance R_t, and the supply voltage V_s, as inserted in **Figue 2**. If the discreteness of electron charge were ignored, the averaged charge Q stored in the capacitor is expressed as $Q = C_dV_s$ and its fluctuation ΔQ is given by

$$\Delta Q = \sqrt{k_B T C_d}\,, \tag{1}$$

where k_B is the Boltzmann constant and T the absolute temperature. Assuming that ΔQ is equal to the elementary charge, e, at room temperature, we obtain C_d of 6.2 aF. Consequently, if C_d is much less than 6.2 aF, the charge fluctuation is suppressed enough to control the number of stored electrons one by one.

The equivalent circuit model in Figure 2 represents the electron transfer between the channel and the floating dot whose total capacitance and tunneling resistance are C_d and R_t, respectively. The relation between C_d and floating dot size can be discussed roughly by replacing C_d with the self-capacitance C_{self} of a Si dot embedded in SiO_2, being expressed as

$$C_{self} = 2\pi\varepsilon_{ox}\phi, \tag{2}$$

where ε_{ox} is the dielectric constant of SiO_2 and ϕ the diameter of the Si dot. Assuming that C_{self} is equal to 6.2 aF, ϕ is estimated to be 29 nm. Thus a nanoscale floating dot is required for room temperature operation. Furthermore the tunneling resistance between the floating dot and the channel, which corresponds to R_t in the circuit model, must exceed h/e^2 (~25.8 kΩ) to suppress the quantum fluctuation of the electron number.[13)]

Figure 2 shows the behavior of the stored electron number as a function of V_s at room temperature (T = 300 K) with the capacitance C_d as a parameter. At this point, the discreteness of the electron charge is taken into account, then the probability $P(n)$ that n electrons are stored is given by

$$P(n) = \frac{1}{Z}\exp\left\{\frac{(ne - C_dV_s)^2}{2C_dk_BT}\right\}, \tag{3}$$

where Z is the partition function, which is necessary for normalization. Dense lines correspond to large probabilities in Figure 2. When C_d = 0.2 aF, corresponding to ϕ of 1 nm, the fluctuation of the electron number is suppressed soundly, and the electron number changes like a staircase as a function of V_s. On the other hand, there are few possible states in the electron number at a certain V_s if C_d = 5 aF. For example, when V_s is 0.5 V, the states whose electron number is 15 or 16 have large probabilities and the states whose electron number is 14 or 17 have small probabilities as indicated by a broken line. The calculated results suggest that a nanometer scale floating dot is necessary to suppress the electron number fluctuation exceedingly.

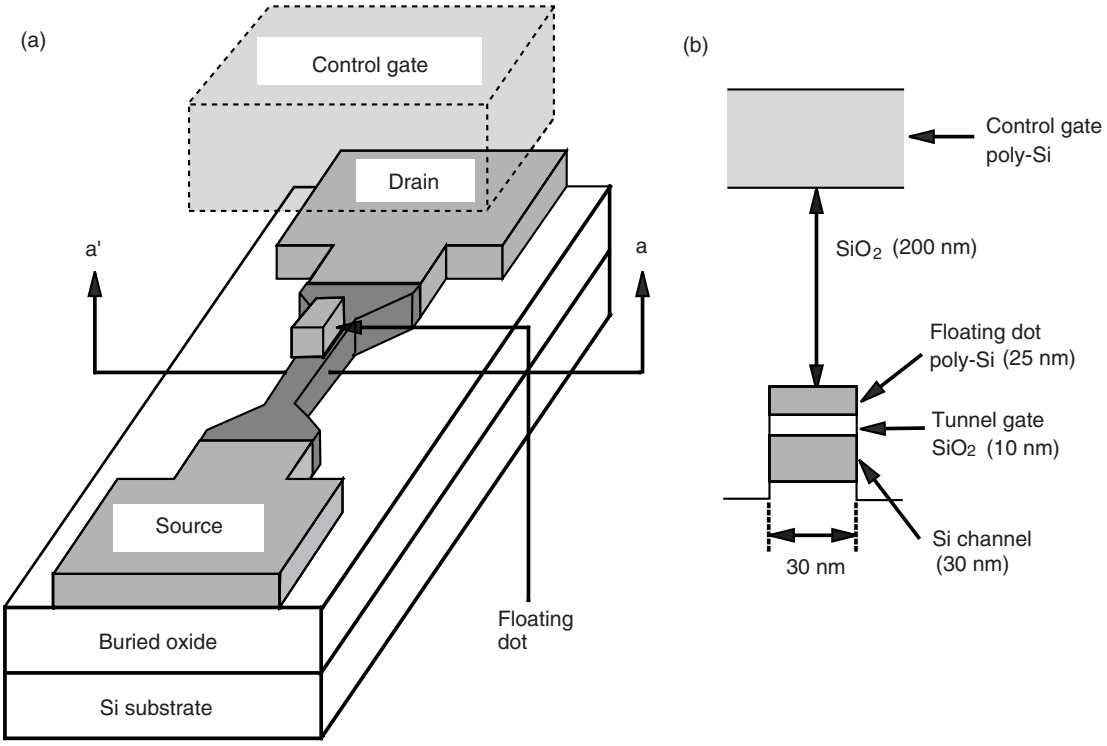

Figure 3
(a) Structure of fabricated single-electron memory, (b) cross-sectional view of structure along a-a' line.

2.3 Current modulation by single-electron charging

The channel width of the single electron memory must be narrow compared with a conventional transistor because the drain current modulation by single-electron charging is smeared out in the case of wide channel. A screen parameter q_s of a two dimensional system is expressed as

$$q_s = \frac{e^2 N_s}{2\varepsilon_{Si} k_B T} \qquad (4)$$

at high temperature, where N_s is the number of electrons per unit area, ε_{Si} the dielectric constant of Si.[14] The inverse of q_s, which has the dimension of length, gives an approximate channel width required for the single electron memory. Assuming N_s of 1×10^{11} cm^{-2}, which is a typical value of our devices, we obtain $1/q_s$ = 34 nm at room temperature. Thus ten-nanometer scale is necessary for the channel width.

3. Experiment of Si single-electron memory

3.1 Fabrication

Figure 3 (a) shows the structure of the single electron memory we fabricated and (b) the cross-sectional view of the structure along the a-a' line.

The process of our device fabrication is as follows. A multilayered structure with Si and SiO_2 layers was formed on a separation by implanted oxygen (SIMOX) Si substrate. First, a 10 nm thick SiO_2 layer, which is used as a gate oxide, was formed by thermal oxidation on the Si channel layer. Subsequently, a 25 nm thick poly-Si layer for the floating dot and a 20 nm thick SiO_2 layer were deposited by low pressure chemical vapor deposition (LPCVD). The top SiO_2 layer was used to prevent vertical etching of the poly-Si layer during an isotropic wet etching process described later.

To obtain a narrow channel FET, a line pat-

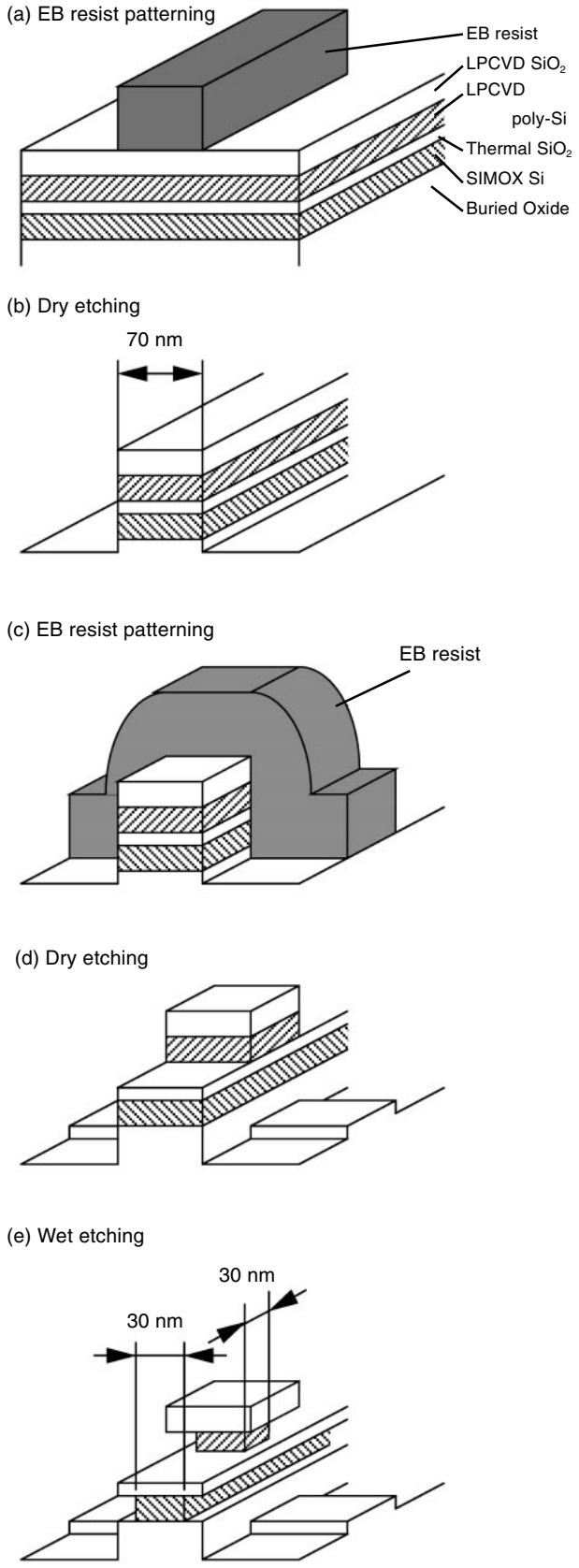

Figure 4
Fabrication process.

tern of the chlomethyl polystyrene (CMS) resist was formed with a width of 70 nm and a length of about 200 nm using electron beam (EB) lithography [**Figure 4(a)**]. The resist was set to be relatively thin (70 nm) in order to easily obtain a fine pattern. Using the resist pattern as a mask, all the layers from the top SiO_2 layer to the Si channel layer were sequentially removed by anisotropic reactive ion etching (RIE). After the resist pattern was removed, a narrow channel structure remained, consisting of a single crystal Si channel layer, a gate oxide layer, a poly-Si floating dot layer, and a top SiO_2 layer [Figure 4 (b)].

Next, a line pattern of the CMS resist with a width of 70 nm was formed perpendicularly crossing over the above mentioned structure using EB lithography [Figure 4(c)]. The thickness of the resist is 70 nm above the structure and about 150 nm elsewhere. Then, the top SiO_2 layer and the subsequent poly-Si layer were removed by RIE. The etching was stopped at the gate oxide layer. Thus, a poly-Si floating dot with both a width and a length of 70 nm was formed on the narrow Si channel. Due to this self-alignment technique, the floating dot is positioned precisely above the channel [Figure 4 (d)].

The obtained size of the floating dot and the channel are still large for room temperature operation of the single-electron memory. Hence, isotropic wet etching was carried out to reduce their sizes further [Figure 4 (e)]. **Figure 5** shows a scanning electron microscope (SEM) image of the structure at this stage. We can see that a floating dot having a side length of about 30 nm is located on a narrow channel. The channel width is equal to or slightly larger than the floating dot (30-40 nm).

After that, a 200 nm thick second gate oxide and a poly-Si control gate layer were deposited by LPCVD, followed by patterning a control gate. Ion implantations of P^+ and As^+ were performed to the control gate and source/drain regions, and the device fabrication is accomplished by forming Ohmic contacts and wiring.

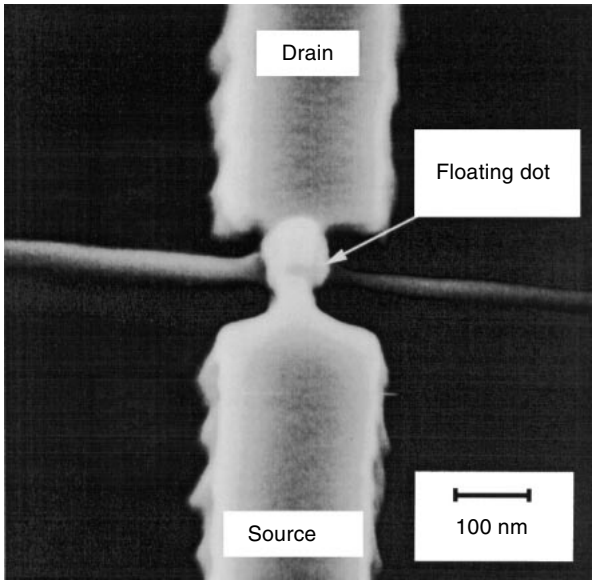

Figure 5
SEM image of fabricated device at stage shown in Figure 4 (e).

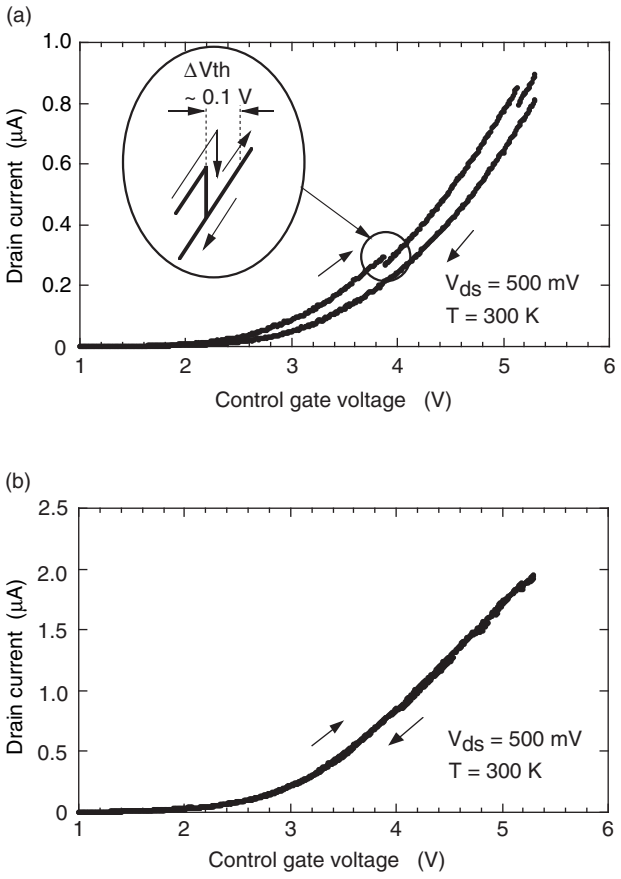

Figure 6
Drain current versus control gate voltage characteristics for (a) device with floating dot and (b) without floating dot.

3.2 Characteristics

Figure 6 shows the typical I_d-V_g characteristics of the fabricated devices. For the device having a floating dot (Figure 6 (a)), the I_d decreases abruptly at V_g of 3.9 V with increasing V_g, while no abrupt I_d change occurs with decreasing V_g, indicating a hysteresis of the I_d-V_g curve as the insertion of Figure 6 (a). With subsequent V_g increase, the second abrupt decrease occurs in the I_d at V_g of 5.1 V. Then, the hysteresis loop in the I_d-V_g characteristics becomes larger.

The control gate voltages at which the I_d changes abruptly are quite reproducible. The threshold voltage shifts ΔV_{th} at V_g of 3.9 and 5.1 V are estimated to be 0.1 V identically. Then the total threshold voltage shift is quantized and expressed by $n \times \Delta V_{th}$, where n is an integer and ΔV_{th} = 0.1 V. This quantized ΔV_{th} indicates that electrons are stored into the floating dot one by one due to the Coulomb blockade effect. Moreover, the apparent hysteresis curve in the I_d-V_g characteristics is valid as a memory function. Thus, this fabricated device exhibits a basic operation of the single-electron memory at room temperature.

On the contrary, a quantized ΔV_{th} nor a hysteresis curve could not be observed in the I_d-V_g characteristics for the device having no floating dot (Figure 6 (b)), indicating that single-electron charging effect did not occur. Slight fluctuation in the I_d may be attributed to electron trapping at defects near the source and drain region, which are wider than the channel, causing the I_d modulation by charging an single-electron to be small. These results support that the quantized ΔV_{th} and the hysteresis are related to the floating dot.

3.3 Analysis and discussion

The experimental results are analyzed using an equivalent circuit model as shown in **Figure 7**. In this model, the separation ΔV_w between the neighboring control gate voltages at which the abrupt Id change occurs is given by

$$\Delta V_w = \frac{e}{C_{gd}} \ , \qquad (5)$$

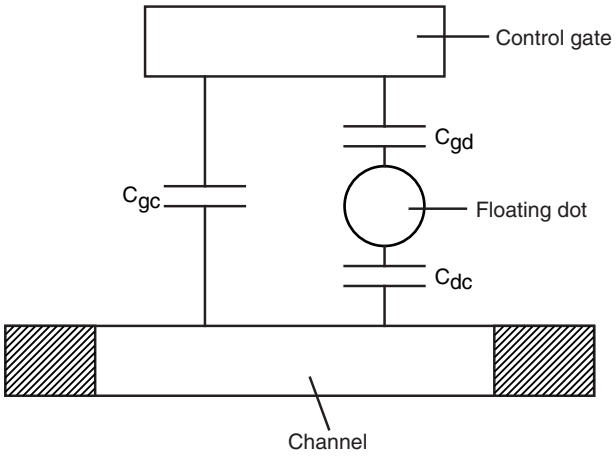

Figure 7
Equivalent circuit model for the single-electron memory.

where C_{gd} is the capacitance between the control gate and the floating dot. Since C_{gd} is estimated to be 0.16 aF from the geometrical factors of this device, ΔV_w is calculated to be 1.0 V. The experimental ΔV_w is 1.2 V obtained from the difference of the two control gate voltages (3.9, 5.1 V) and is close to the calculated result.

On the other hand, ΔV_{th} is given by

$$\Delta V_{th} = \frac{e}{C_{gc} + \dfrac{C_{gd}C_{dc}}{C_{gd}+C_{dc}}}, \qquad (6)$$

where C_{gc} is the capacitance between the control gate and the channel, and C_{dc} the capacitance between the floating dot and the channel. Since C_{dc} is much larger than C_{gd}, ΔV_{th} is simplified to

$$\Delta V_{th} = \frac{e}{C_{gc}+C_{gd}}. \qquad (7)$$

There is some difficulty in the C_{gc} estimation from the geometrical factors because the area of the channel to be taken in the estimation is not clear. Hence, if the area just below the floating dot is taken, C_{gc} is calculated to be 0.16 aF, which gives ΔV_{th} a value of 0.5 V. This is larger than that obtained from the measurement (0.1 V). If the entire area of the narrow channel region (200×40 nm^2) is taken in the estimation, C_{gc} is calculated to be 1.4 aF, resulting in a ΔV_{th} of 0.1 V. Consequently, the latter case is considered to be valid.

The carrier density N_s in the channel region is roughly expressed as $N_s = C_s(V_g - V_{th})/e$, where C_s is the capacitance per unit area between the control gate and the channel, calculated to be 17 nF/ cm^2 geometrically. Assuming $V_g - V_{th}$ of 4 V, we obtain N_s of 7×10^{11} cm^{-2}. Then the screen length $1/q_s$ is estimated to be 5 nm, being an eighth part of the channel width. This value is qualitatively consistent with the amplitude of the I_d modulation which is about 5% in the experiment.

The self-capacitance of a Si dot in SiO_2 with a diameter of 30 nm is calculated to be 6.5 aF. The total capacitance C_d of the fabricated floating dot should be larger than 6.5 aF and the electron number is expected to slightly fluctuate as shown in Figure 2. In the experiment, the reproducibility of the voltages at which V_{th} shifts occur is fairly good. However, the voltages fluctuate slightly in some devices. This result is consistent with the estimated capacitance.

4. Novel method for small dot formation

The key technology for single-electron memories is how to fabricate nanometer scale dots. High throughput and good uniformity in size and position are required for the fabrication method. EB lithography has some difficulty in these points. Hence we developed a novel method making use of ion implantation to form nanoscale dots which satisfies the above requirements. Several groups reported the formation of metal nanocrystals by using ion implantation.[15)-17)] They all implanted metal ions into a thick SiO_2 layer with a relatively high energy and studied these metal dots focusing on their unique optical properties.[15)-17)] We developed this technique to be available for single-electron memories by employing a low energy ion implantation of Sn^+ or Sb^+ into a SiO_2 thin film, resulting in a narrow as-implanted ion concentration profile and successfully obtaining metal nanocrystals with controlling their vertical position.[18)-21)]

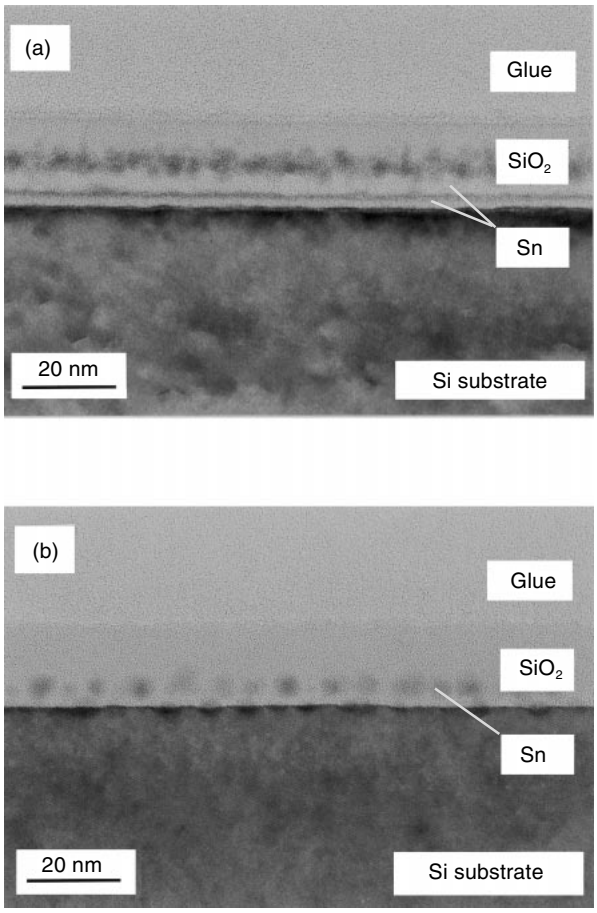

Figure 8
Cross sectional TEM images of Sn implanted thin SiO_2 layer: (a) as implanted, and (b) after annealing.

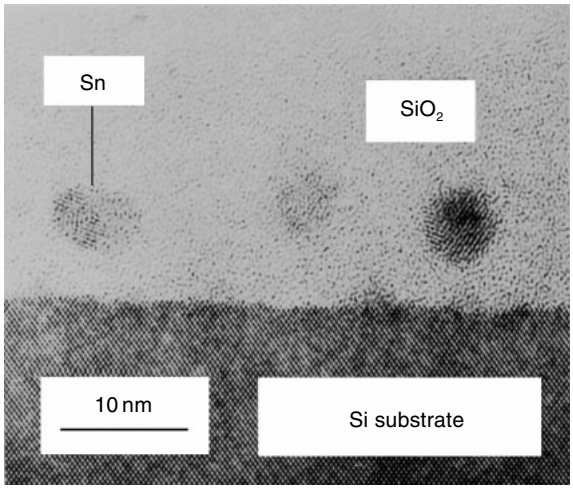

Figure 9
High resolution TEM image of Sn dots.

4.1 Fabrication

The fabrication process of Sn dots is as follows. An n^+-Si substrate with a 15 nm thick thermally oxidized SiO_2 layer was used. Sn^+ ions were implanted into the SiO_2 layer with a low energy of 10 keV and a dose of 5.0×10^{15} ions/cm^2. The calculated projected range was at the center of the SiO_2 layer with the standard deviation of 2.0 nm. After that, the substrate was set face to face on a dummy Si wafer and annealing was done at 900°C for 10 minutes, in N_2 ambient.

Figure 8 shows the cross sectional transmission electron microscopy (TEM) images of a Sn implanted SiO_2/Si interface, (a) as implanted, and (b) after annealing. In the as-implanted sample, no Sn dots are observed, while we can see two peaks of Sn concentrations. One broader peak is lying at the center of the SiO_2 layer with a width of 4 nm, as expected. The other sharper peak is lying near the SiO_2/Si interface, suggesting the existence of a stable region near the interface. The origin of this stable region is under investigation. Compressive strain near the SiO_2/Si interface may be related. After annealing, Sn nanoscale dots formed around the stable region in the SiO_2 layer, highly aligned in depth. The average diameter of Sn dots is about 4.1 nm with a standard deviation of 1.0 nm. In our knowledge, this size uniformity is the best among those ever reported for metal nanoscale dots. The plane density of Sn dots are on the order of about 10^{11} dots/cm^2.

Figure 9 shows a high resolution TEM image of Sn dots. A lattice image is observed in some Sn dots, indicating that these dots are neither Sn oxide nor amorphous Sn, but a Sn crystal. According to the lattice spacing of 0.28 nm, we assigned them as the (101) plane of Beta phase Sn. In the phase diagram, Beta phase Sn is a high temperature phase obtained at above 18°C. This is consistent with the annealing temperature of 900°C.

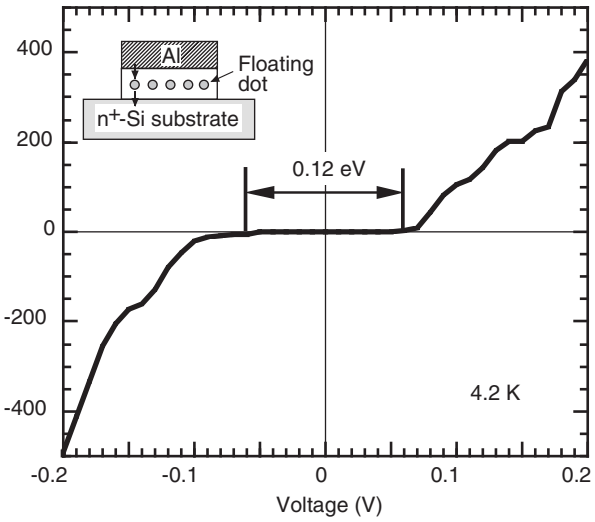

Figure 10
Current-voltage characteristics of diode in which Sn dots are embedded.

4.2 Electrical characteristics

To evaluate the single-electron charging effect, we prepared diode structures and measured the current-voltage (I-V) characteristics. In the diode preparation, a SiO_2 layer, where Sn nanocrystals are embedded, was etched to reduce its thickness to about 10 nm, thereby the tunneling current through the SiO_2 increases and becomes measurable. Then, an Al gate with a diameter of 200 μm were formed on the SiO_2 layer. The back contact was AuGe/Au.

Figure 10 shows the I-V characteristics of the diode measured at 4.2 K. The current flows between the Si substrate and the Al gate through Sn dots and a Coulomb blockade region of about 0.12 V is observed. It should be noticed that steplike I-V characteristics, which is well known as Coulomb staircases, are also observed. The single-electron charging energy at a Sn dot is estimated from the width of the blockade region according to the standard Coulomb blockade theory. In the case of our diode, the capacitance between the Al gate and a Sn dot is expected to be almost equal to that between the Si substrate and a Sn dot due to geometrical consideration. Assuming these capacitances to be C, the width of the blockade region (0.12 V) is equal to e / C and the total capacitance C_Σ of a dot becomes $2C$. Hence the single-electron charging energy $e^2 / 2C_\Sigma$ ($= e^2 / 4C$) is estimated to be 0.03 eV. This value is close to the charging energy of 0.09 eV that is estimated from the self-capacitance of a Sn dot with a diameter of 4 nm. The discrepancy between these two charging energies is probably due to the inaccuracy of the self-capacitance estimation which ignores the finite distances from a Sn dot to the Si substrate, the Al gate, and to other Sn dots.

5. Conclusion

We developed a new Si single-electron memory having a ultra-small floating gate stacked on a channel by self-aligned process. The device exhibits quantized threshold voltage shifts and hysteresis curves in the electrical characteristics at room temperature, indicating that this device can operate as a single-electron memory. A novel method to form small metal dots was also developed. Sn nanocrystals were formed in thin, thermally grown SiO_2 layers by using low energy ion implantation followed by thermal annealing. The I-V characteristics show a clear Coulomb gap and Coulomb staircases.

These results show that the techniques described in this paper is promising for making single-electron memories to be practical.

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