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High Performance 0.04 µm PMOSFET

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This paper describes a high-performance 0.04-µm PMOSFET with a 7-nm-deep ultra-shallow junction. An ultra-low energy implantation of $B_{10}H_{14}^+$ at 2 keV (with effective boron energy of 0.2 keV), which does not cause transient-enhanced diffusion, is employed for extension formation. To prevent thermal diffusion, we developed a two-step activation annealing process (2-step AAP) that forms a shallow extension with low-temperature annealing after deep source and drain formation. A maximum drive current of 0.40 mA/µm (@ I_{off} of 1 nA/µm and V_d = –1.8 V) was achieved, and the smallest PMOSFET (with a L_{eff} of 0.038 µm) has been demonstrated for the first time. We also achieved a low S/D series resistance R_{sd} of 760 Ω-µm, even when high sheet resistance (>20 kΩ/sq) is applied to the extension regions.

1. Introduction

CMOSFETs are now widely used for ULSI devices (e.g., logic, memory, analog devices) and have been responsible for improved performance as well as greater density due to device size scaling. Recently, a high-performance CMOS[1)-3)] and an ultra-small 0.04 µm NMOSFET[4)] were intensively studied to achieve low-power, high-speed operation.

In extending CMOS scaling to a sub-0.1 µm region, however, PMOSFET fabrication becomes more critical due to the difficult low-energy implantation of boron ions for source/drain (S/D) extensions, and suppression of boron diffusion, which is caused by both transient-enhanced diffusion (TED) and thermal diffusion (TD) that occur during activation annealing. To solve the problem of low energy ion implantation, we developed a decaborane implantation technology.[5)] Since decaborane has ten borons, it can be implanted with one-tenth lower implantation energy and a ten times higher boron dosage. For problems with TED, we found that a low-energy implantation of less than 0.5 keV suppresses TED.[5)] For problems with TD, one solution is to reduce the activation annealing temperature. This measure causes a reduction in dopant activity, however, and consequently degrades the gate capacitance, as well as contact and series resistances.

In our research to resolve this tradeoff, we developed a new MOSFET fabrication process called the two-step activation annealing process (2-step AAP),[6)] which forms shallow S/D extensions with low-temperature rapid thermal annealing (RTA) to prevent TD after deep S/D formation with a high-temperature RTA. This process maintains high gate capacitance (C_{gox}) and low contact resistance (R_c). With these new technologies, we were able to produce a high-performance 0.04-µm PMOSFET.

2. Ultra-Shallow Junction by Decaborane Ion Implantation

Recently, we developed a low-energy decaborane ion implantation technology that can implant at one-tenth lower effective acceleration energy

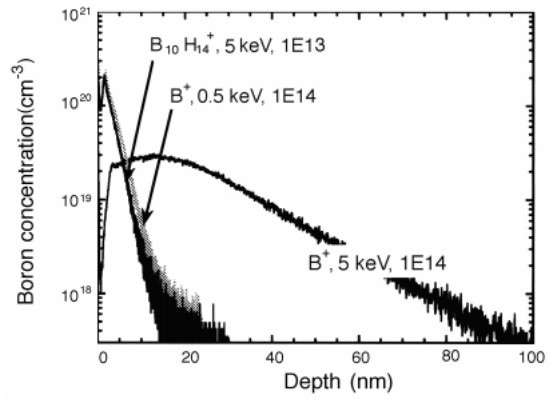

Figure 1
Boron profile of decaborane ion implantation.

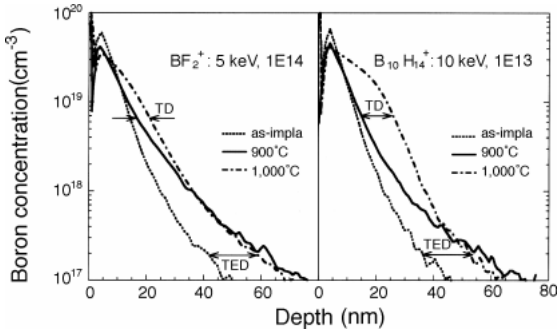

Figure 2
Boron diffusion profiles implanted by $B_{10}H_{14}^+$ at 10 keV, and BF_2^+ at 5 keV after 10 s at 900°C and 1,000°C.

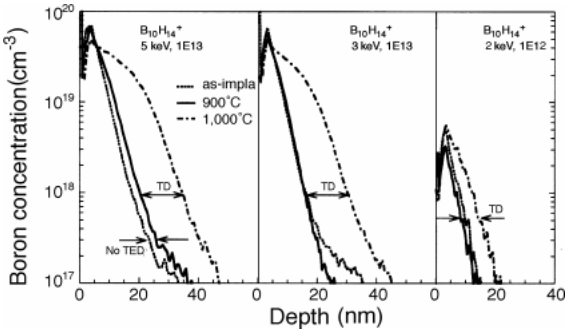

Figure 3
Boron diffusion profiles implanted by $B_{10}H_{14}^+$ at 5 keV, 3 keV, and 2 keV after 10 s at 900°C and 1,000°C.

and a ten times higher effective boron dosage.[5] **Figure 1** shows a SIMS profile of decaborane ion implantation at 5 keV, and of boron implantation at 5 and 0.5 keV. Although the 5 keV boron has a deeper profile, the 5 keV decaborane has a shallow profile very similar to that of boron at 0.5 keV. Regarding the implanted dosage, decaborane is set at 1×10^{13}/cm^2, which is one-tenth lower than that of boron. These results clearly demonstrate the advantages of decaborane ion implantation: decaborane can be implanted with one-tenth lower implantation energy and a ten times higher boron dosage.

Figure 2 shows the diffusion profiles of BF_2 at 5 keV and of decaborane at 10 keV after annealing at 900˚C and 1,000˚C. Both profiles of effective energy and dosage are nearly equal. We can observe TED in both profiles at 900˚C annealing in the low concentration region. At 1,000˚C in the high concentration region, we can see thermal diffusion (TD). These are typical diffusion profiles that cause both TED and TD.

Figure 3 shows the diffusion profiles of decaborane ion implantation with energies reduced to 5, 3, and 2 keV. The dosage for the 2 keV implanted sample was set at one-tenth lower than that of other samples. Based on the 900˚C data on all energy levels, TED can be completely suppressed by reducing the implantation energy to below 5 keV. We believe that this is because low energy ion implantation may generate interstitial Si near the Si surface. As a result, the interstitial Si diffuses out from the Si surface without causing TED. At 1,000˚C, however, thermal diffusion still occurs. Therefore, for a decanano device, activation annealing must be reduced to less than 900˚C. In this research, we used a 7-nm-deep shallow junction of $B_{10}H_{14}^+$, 2 keV, and applied 900˚C for extensions of the 0.04-μm PMOSFET.

Figure 4 summarizes the sheet resistance and junction depth of junctions that were implanted with decaborane and BF_2. The junction depth was defined at a dosage of 1×10^{18}/cm^3. High-energy implanted and 1,000˚C-annealed junctions cause TED and TD. Low-energy and 1,000˚C junctions only cause TD. Low-energy and 900˚C junctions have the shallowest line without causing TED and TD. This clearly indicates that both TED

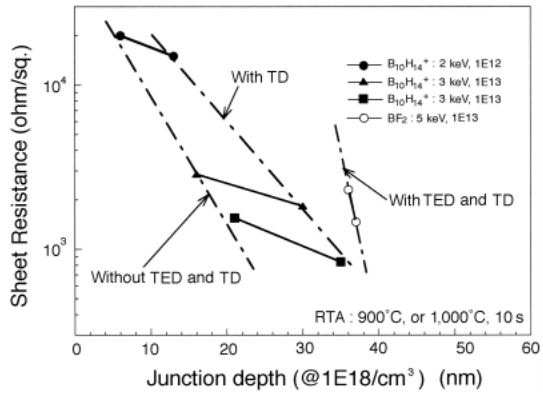

Figure 4
Sheet resistance vs. junction depth.

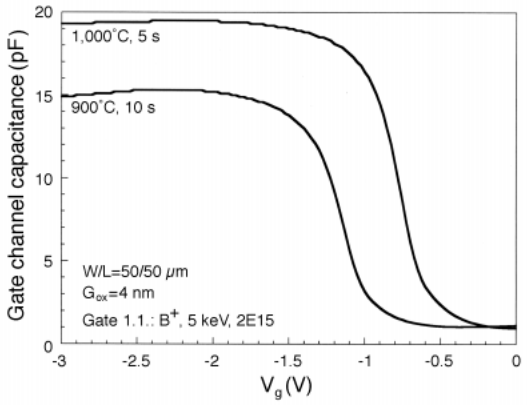

Figure 5
Gate capacitance vs. gate voltage at 900°C and 1,000°C RTA.

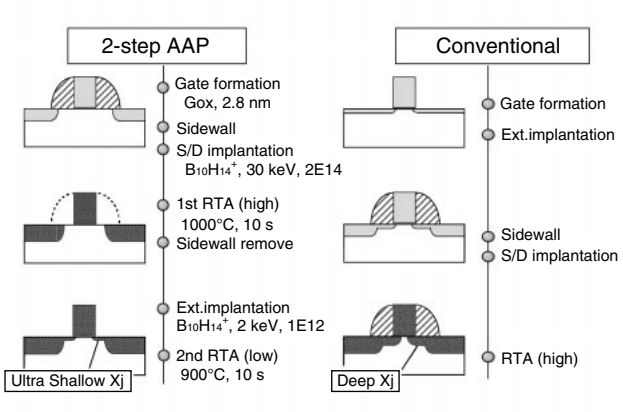

Figure 6
Process steps of 2-step activation annealing and conventional processes.

and TD must be suppressed to achieve an ultra-shallow junction with low sheet resistance. The 7-nm junction used for the 0.04-μm PMOSFET has very high sheet resistance of more than 20 kΩ/sq, but does not degrade S/D resistance (as discussed later).

3. Device Fabrication

For high-performance operation, activation annealing above 1,000°C is essential to prevent poly-Si gate depletion for a high drive current. **Figure 5** shows the gate capacitance after activation annealing at 900°C and 1,000°C. Annealing at 900°C is inadequate to prevent gate depletion. Thus, annealing at 1,000°C is not only required to achieve high gate capacitance, it is also necessary to achieve low contact resistance (R_c). Such high temperatures as 1,000°C cause the thermal diffusion of boron, however. To resolve this dilemma, we developed a two-step activation annealing process (2-step AAP).

Figure 6 shows the process steps of the two-step activation annealing and conventional sidewall processes. The conventional process consists of gate formation, extension implantation, sidewall (SW) formation, deep S/D and gate implantation, and finally, a high-temperature RTA that forms deep extension junctions.

Our 2-step AAP consists of gate formation and SW formation, and deep S/D and gate implantation. The first RTA is performed at high temperature to achieve high dopant activity. After the SW is removed, the S/D extension is implanted and annealed at a lower temperature. This provides ultra-shallow junctions without causing TD and also achieves high gate capacitance and low contact resistance.

For our 0.04-μm PMOSFET, a 2.8 nm gate oxide (measured using an optical method) was used. A dummy SW is formed using CVD SiO_2. A high dose of boron ($B_{10}H_{14}^+$, 30 keV, 2×10^{14} ions/cm^2) is then implanted for the gate and deep S/D junctions, followed by the first RTA at high temperature (1,000°C for 10 s) for high dopant acti-

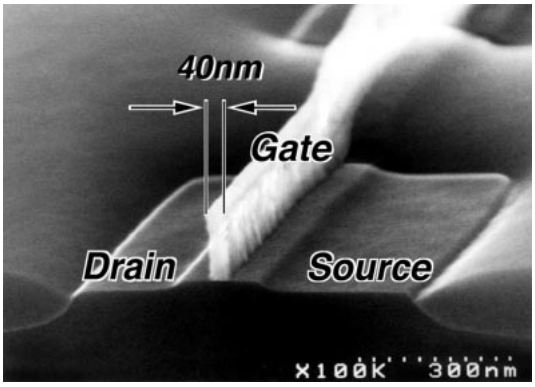

Figure 7
Cross-sectional SEM of device with 0.04 µm gate length after sidewall removal.

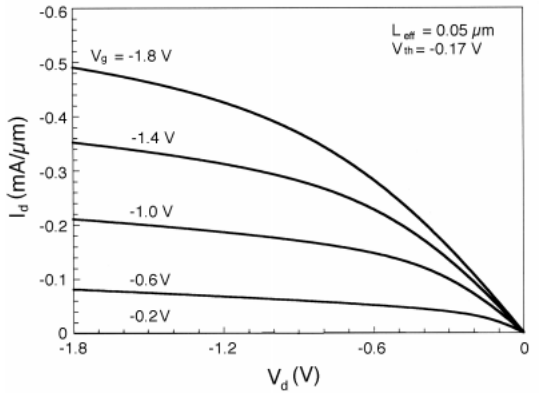

Figure 9
I_d-V_d characteristics of PMOSFET (L_{eff} = 0.05 µm).

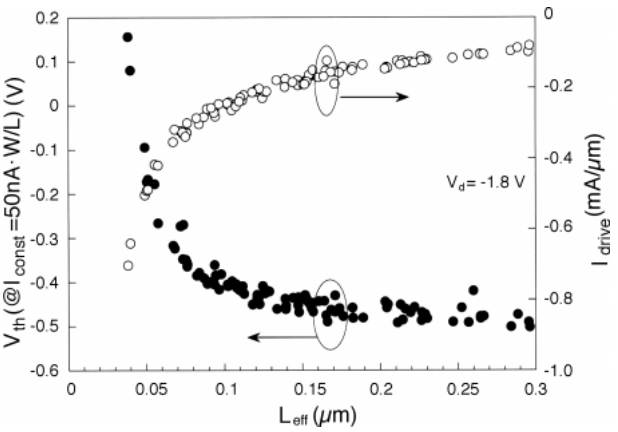

Figure 8
Saturated V_{th} rolloff and drain current.

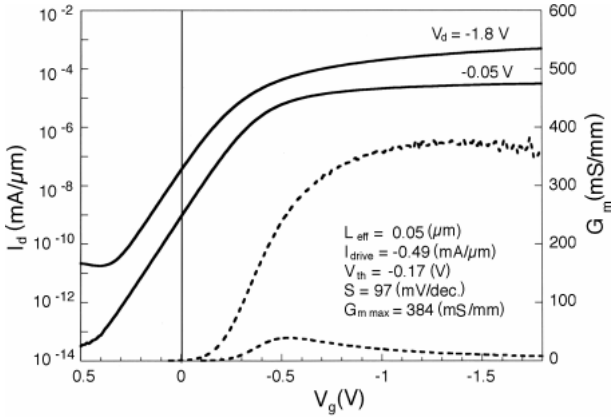

Figure 10
Subthreshold characteristics of PMOSFET (L_{eff} = 0.05 µm).

vation. After the SW is removed by a HF wet process, ultra-low-energy boron is implanted by $B_{10}H_{14}^{+}$, 2 keV, 1×10^{12} ions/cm^2, followed by the second RTA at a lower temperature (900˚C for 10 s) to form 7-nm-deep ultra-shallow junctions without TED and TD. For this device, we only employed a conventional channel structure, with no pocket or halo channel implantation.

Gate formation of deca-nano critical size is also a difficult process. In this research, we used electron beam lithography and the SiO_2 mask trimming process. A 100-nm wide resist was patterned by EB lithography. Using this EB resist, a SiO_2 hard mask formed on the poly-Si was etched by RIE, then shrunk through a wet etching process. Finally the poly-Si was etched by RIE. This process is able to form stable gates with line widths less than 0.04 µm. **Figure 7** is a SEM image of a device having a poly-Si gate length of 0.04 µm after SW removal. The well-shaped 0.04 µm gate is clearly visible.

4. Device Performance

Figure 8 shows the dependence of V_{th} and drive currents on L_{eff} at a supply voltage of –1.8 V. L_{eff} is extracted by using the "new shift and ratio method".[7] V_{th} is defined as I_{const} = 50 nA · W/L_{eff}. A well-suppressed short channel effect was observed at L_{eff} up to 0.05 µm. A continuously increasing drive current was also observed.

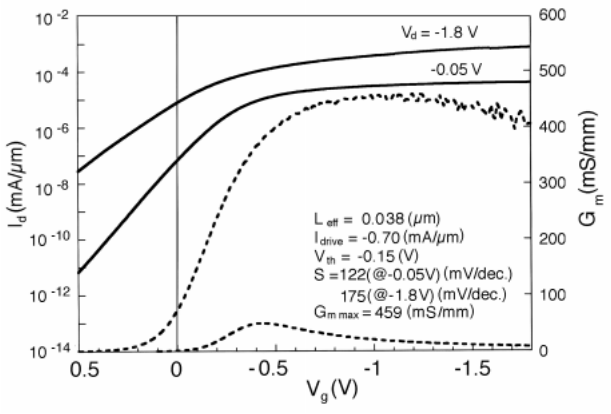

Figure 11
Subthreshold characteristics of PMOSFET (L_{eff} = 0.038 µm).

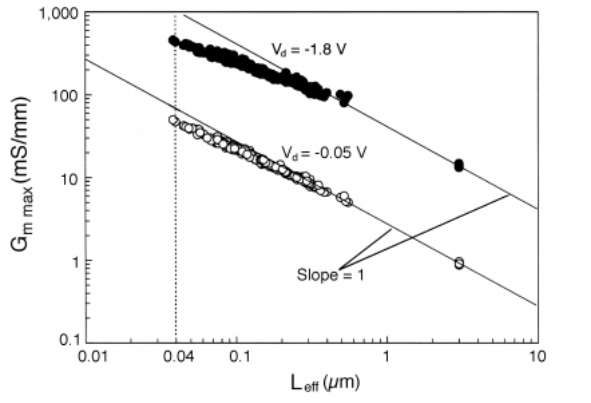

Figure 12
Saturation transconductance vs. L_{eff}.

Figures 9 and 10 show the I_d-V_d and I_d-V_g characteristics of a PMOSFET with L_{eff} of 0.05 µm. An excellent drive current of 0.5 mA/µm with V_{th} of –0.17 V was achieved. Figure 10 also shows the subthreshold slope and G_m characteristics. A well controlled subthreshold slope of 97 mV and very high $G_{m\,max}$ of 384 mS/mm were achieved without causing punch-through current. **Figure 11** shows the data for our smallest PMOSFET among our devices that can operate as a transistor. Its L_{eff} is 0.038 µm, the drive current is 0.70 mA/µm, and $G_{m\,max}$ is more than 450 mS/mm.

Figure 12 plots the log scale of $G_{m\,max}$ and L_{eff} at supply voltages of –1.8 and 0.05 V. When L_{eff} was decreased, $G_{m\,max}$ continuously increased down to L_{eff} less than 0.04 µm. For –0.05 V, most plots show an inverse proportional slope of 1. This data suggests the possibility of producing PMOSFETs with an effective gate length less than 0.04 µm.

Table 1
Process conditions of new and old PMOSFETs.

	New process 0.04 µm PMOS	Old process 0.1 µm PMOS
Process	2 step AAP	Conventional SW
Extension	$B_{10}H_{14}^+$, 2 KeV,10^{12}/cm^2	$B_{10}H_{14}^+$, 5 KeV,10^{13}/cm^2
RTA	900°C,10 s	1,000°C,10 s
Xj	7 nm	37 nm
R_{sheet}	up to 20Ω/sq	1.5 kΩ/sq
Gox	2.8 nm	4.0 nm

We would now like to discuss the short channel effects compared to our previous devices.[5] **Table 1** summarizes the contrasting conditions for the new and old processes. The old process involved a conventional sidewall process. For S/D extension, decaborane was implanted at 5 keV 1×10^{13} ions/cm^2 and annealed at 1,000°C. This provides a 37-nm deep junction when using 1.5 kΩ/sq and a 4 nm gate oxide. The new process uses a 7-nm-deep junction with 20 kΩ/sq and a 2.8 nm gate oxide.

Figures 13 and 14 compare the subthreshold slope and drain induced barrier lowering (DIBL). The new process improved the short channel effect by about 0.05 µm over the old process due to a reduced junction depth and thicker gate oxide.

Figure 15 plots the total resistance (R_{total}) and source/drain series resistance (R_{sd}) of the new and old processes for various gate lengths. The results are quite interesting. The new process achieved a low R_{sd} of 760 Ωµm, which is lower than that of the old process (1,010 Ωµm), even though the S/D extension of the new process uses a very high sheet resistance of more than 20 kΩ/sq. We believe that the reduced length of the extension region (due to the suppressed lateral diffusion and

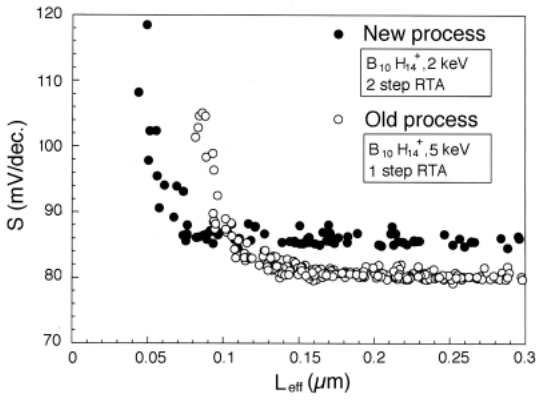

Figure 13
Subthreshold slope vs. L_{eff} compared to old process PMOSFETs.[5)]

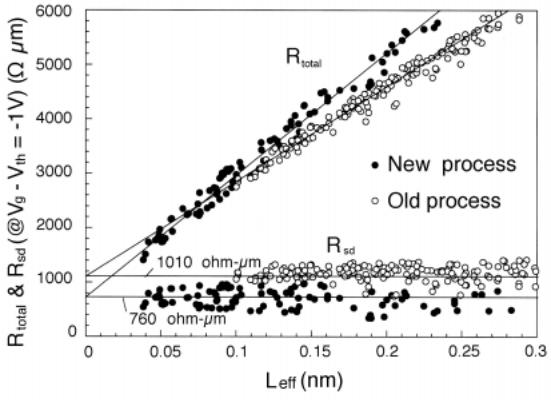

Figure 15
Total resistance and S/D series resistance of new and old processes with various L_{eff}.

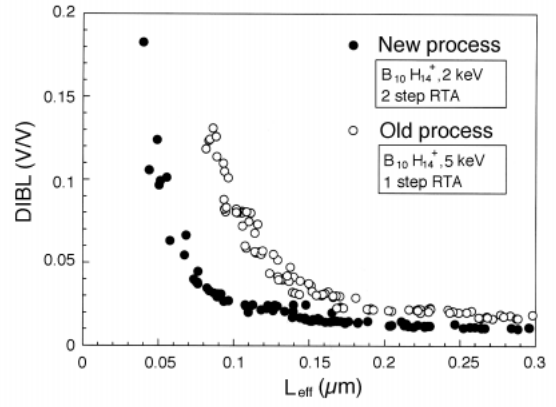

Figure 14
DIBL vs. L_{eff} compared to old process PMOSFETs.[5)]

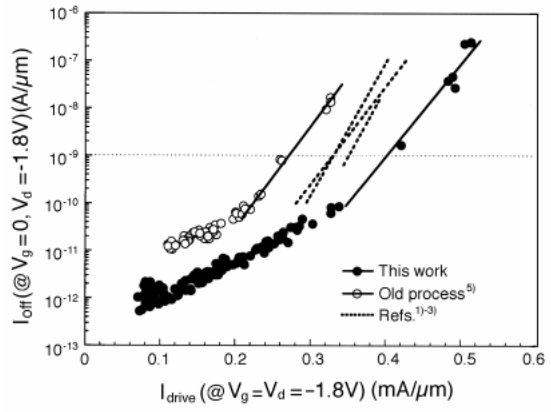

Figure 16
Comparison of I_{drive} -I_{off} of PMOS to results reported in recent publications.[1)-3),5)]

optimum sidewall length) make this possible. This short extension also helps reduce source/drain resistance. Therefore, minimizing the extension length is important factor in achieving a low source/drain resistance.

Figure 16 plots the I_{drive} vs. I_{off} values of the new process compared to those of the old process[5)] and recently reported high-performance PMOSFETs.[1)-3)] This work achieves a maximum I_{drive} of 0.40 and 0.70 mA/μm due to the great success in scaling L_{eff} down to 0.05 μm and 0.038 μm, without being affected by SCE, and while maintaining a low R_{sd}. This result is significant because it guarantees an improvement in drive current by scaling device size down to at least 0.04 μm with suppressed SCE.

5. Conclusion

We have developed and demonstrated a high-performance 0.04 μm PMOSFET technology to achieve excellent SCE and maximum drive current of 0.40 mA/μm (@ I_{off} of 1 nA/μm and V_d = –1.8 V). A 7-nm-deep ultra-shallow junction is fabricated using 2 keV decaborane ion implantation for TED suppression and a two-step activation annealing process that completely prevents boron thermal diffusion while maintaining high dopant activity for a high C_{gox} and low R_c. A low R_{sd} of 760

Ωµm is achieved even when using high sheet resistance of more than 20 kΩ/sq for the shallow S/D extension. This suggests that an extremely shallow junction does not degrade R_{sd} because the length of the extension region is reduced.

Acknowledgments

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