Post-K Computer Development, Updates for SC’18
Fujitsu’s High-end HPC Development

- Fujitsu has been leading HPC technologies for over 40 years

**K computer**
- Ranked Top500 No.1 in 2011
- Competitive in various fields
- Gordon Bell Prize Finalist (2016)
- HPCG No.3 (2018)
- Graph500 No.1 (2018)

**PRIMEHPC FX100**

**Post-K computer**
- Next Japanese flagship supercomputer under development
RIKEN and Fujitsu are currently developing Post-K computer, the most advanced general-purpose supercomputer, in the world.

Post-K computer is optimized to achieve superior performance in real applications as next Japanese flagship system.
Post-K Computer Goals and Approaches

Approach
1. A64FX CPU
2. Compiler and Runtime
3. LLIO (Lightweight Layered IO-Accelerator)
A64FX CPU

- Achieves high performance in HPC and AI applications
  - Arm Scalable vector extension (SVE), high-bandwidth caches and memory
  - (D|S|H)GEMM and INT (16b/8b) GEMM > 90%, STREAM Triad > 80%

<table>
<thead>
<tr>
<th>ISA (Base + Extension)</th>
<th>A64FX (Post-K computer)</th>
<th>SPARC64 VIII fx (K computer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology</td>
<td>7 nm</td>
<td>45 nm</td>
</tr>
<tr>
<td>Peak Performance</td>
<td>&gt; 2.7 TFLOPS</td>
<td>128 GFLOPS</td>
</tr>
<tr>
<td>SIMD</td>
<td>512-bit</td>
<td>128-bit</td>
</tr>
<tr>
<td># of Cores</td>
<td>48+4</td>
<td>8</td>
</tr>
<tr>
<td>Memory Peak B/W</td>
<td>1024 GB/s</td>
<td>64 GB/s</td>
</tr>
</tbody>
</table>

Copyright 2018 FUJITSU LIMITED
Fujitsu’s compiler and runtime libraries exploit the hardware capabilities along three dimensions:

- **Memory access performance**
  - Software prefetch
  - Loop-blocking

- **Computational performance**
  - Software pipelining with Loop fission
  - Auto-vectorization with SVE

- **Thread-parallel performance**
  - CMG & SVE optimized math library
  - OpenMP 5.0 API & fast barrier

<table>
<thead>
<tr>
<th>Compiler &amp; Runtime</th>
<th>Hardware capabilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory access performance</td>
<td>Computational performance</td>
</tr>
<tr>
<td>• Software prefetch</td>
<td>• Software pipelining with Loop fission</td>
</tr>
<tr>
<td>• Loop-blocking</td>
<td>• Auto-vectorization with SVE</td>
</tr>
<tr>
<td>• Hardware prefetch</td>
<td>• Out-of-order</td>
</tr>
<tr>
<td>• Stacked memory; HBM2</td>
<td>• 512-bit SVE</td>
</tr>
</tbody>
</table>
Preliminary Performance Evaluation Results

A64FX’s instruction set and compiler achieve high performance on loop of math function

Step 1. Armv8 coding
Step 2. + SVE + accel.Instruction coding
Step 3. + Inlined by compiler
Step 4. + Applied software pipelining by compiler
LLIO (Lightweight Layered IO-Accelerator)

- Boosts I/O performance w/o modifying Apps
  - Exploits SSD as a shared cache of persistent filesystem (PFS)

- Provides two kinds of temporary filesystems for I/O optimization
  - Shared/Local temporary filesystem
Post-K Computer Current Status

- CPU powered-on, OS running
- System design verification and testing are underway
- Preliminary performance evaluation started

Development Proceeding on Schedule
Post-K Computer Hardware Features

Post-K computer’s high-density mounting achieves over 1 PFlops per rack

- 1 CPU/Node
- CMU (CPU Memory Unit) 2 Nodes/CMU
- Shelf 24 CMUs/Shelf (48 Nodes)
- Rack 8 Shelves/Rack (384 Nodes)
(Cont.) Post-K Computer Hardware Features

- High-density mounting, shortened transmission distance between CPUs
  - High-efficiency water cooling unit on the CPU memory unit (CMU) provides 100% water-cooling
  - The back-to-back layout and cable box shorten the cables length
  - Single action connection of electric connectors and water couplers achieve compact CMU
shaping tomorrow with you