Next-Generation PRIMEHPC
## The K computer and the evolution of PRIMEHPC

<table>
<thead>
<tr>
<th></th>
<th>K computer</th>
<th>PRIMEHPC FX10</th>
<th>Post-FX10</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>SPARC64 VIIIIfx</td>
<td>SPARC64 IXIfx</td>
<td>SPARC64 XIIfx</td>
</tr>
<tr>
<td>Peak perf.</td>
<td>128 GFLOPS</td>
<td>236.5 GFLOPS</td>
<td>1TFLOPS ~</td>
</tr>
<tr>
<td># of cores</td>
<td>8</td>
<td>16</td>
<td>32 + 2</td>
</tr>
<tr>
<td>Memory</td>
<td>DDR3 SDRAM</td>
<td>←</td>
<td>HMC</td>
</tr>
<tr>
<td>Interconnect</td>
<td>Tofu Interconnect</td>
<td>←</td>
<td>Tofu Interconnect 2</td>
</tr>
<tr>
<td>System size</td>
<td>11PFLOPS</td>
<td>Max. 23PFLOPS</td>
<td>Max. 100PFLOPS</td>
</tr>
<tr>
<td>Link BW</td>
<td>5GB/s x bidirectional</td>
<td>←</td>
<td>12.5GB/s x bidirectional</td>
</tr>
</tbody>
</table>

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Smaller, faster, more efficient

- Highly integrated components with high-density packaging.
- Performance of 1-chassis corresponds to approx. 1-cabinet of K computer.

Efficient in space, time, and power

Fujitsu designed SPARC64™ XIfx CPU Memory Board Chassis (12 CPUs) Cabinet Over 200 nodes/cabinet

- 32 + 2 core CPU
- Tofu2 integrated
- Three CPUs
- 3 x 8 HMCs (Hybrid Memory Cube)
- 8 optical modules (25Gbpsx12ch)
- 1 CPU/1 node
- 12 nodes/2U chassis
- Water cooled
Architecture continuity for compatibility

- **Upper compatible CPU:**
  - Binary-compatible with the K computer & PRIMEHPC FX10
  - Good byte/flop balance

- **New features:**
  - New instructions (stride load/store, indirect load/store, permutation, concatenation)
  - Improved micro architecture (out-of-order, branch-prediction, etc.)

- **For distributed parallel executions:**
  - Compatible interconnect architecture
  - Improved interconnect bandwidth
# 32 + 2 core SPARC64 XI fx

- Rich micro architecture improves single thread performance.
- HMC fulfills required bandwidth for multi-core high performance CPU.
- 2 additional, Assistant-cores for avoiding OS jitter and non-blocking MPI functions.

<table>
<thead>
<tr>
<th>Core config.</th>
<th>K</th>
<th>FX10</th>
<th>Post-FX10</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak FP performance</td>
<td>128 GF</td>
<td>236.5 GF</td>
<td>1-TF class</td>
<td>Maintains similar architecture for compatibility with applications</td>
</tr>
<tr>
<td>Execution unit</td>
<td>FMA × 2</td>
<td>FMA × 2</td>
<td>FMA × 2</td>
<td></td>
</tr>
<tr>
<td>SIMD</td>
<td>128 bit</td>
<td>128 bit</td>
<td>256 bit wide</td>
<td>Wider SIMD for better performance with small-sized additional hardware</td>
</tr>
<tr>
<td>Dual SP mode</td>
<td>NA</td>
<td>NA</td>
<td>Double of DP</td>
<td>Accelerates SP-rich apps</td>
</tr>
</tbody>
</table>
| Integer SIMD            | NA        | NA        | Support         | Accelerates INT rich apps
|                         |           |           |                 | Assists SIMDization with list vector                               |
| Single thread           | -         | -         | Increase OOO    | Application performance often limited by
| performance enhancement |           |           | resources, better thread performance and no FP calc.               |
Flexible SIMD operations

- New 256-bit wide SIMD functions enable versatile operations
  - Four double-precision calculations
  - Stride load/store, Indirect (list) load/store, Permutation, Concatenation

![Diagram of SIMD operations](image-url)
Tofu Interconnect 2

- Successor to Tofu Interconnect
  - Highly scalable, 6-dimensional mesh/torus topology
  - Increased link bandwidth by 2.5 times to 12.5 GB/s

- Interconnect integrated into CPU
  - System-on-chip (SoC) removes off-chip I/O
  - Improved packaging density and energy efficiency

- Optical cable connection between chassis
Flexible interconnect topology

- **Tofu**: Six-dimensional mesh/torus direct network
- Logical 3D, 2D or 1D torus network from the user’s point of view

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**Scalable three-dimensional torus**

Three-dimensional torus unit: $2 \times 3 \times 2$

Well-balanced shape available
Entire software stack is enhanced for Post-FX10

Applications

HPC Portal / System Management Portal

Technical Computing Suite

System Management
- System management
- System control
- System monitoring
- System operation support

Job Management
- Job manager
- Job scheduler
- Resource management
- Parallel

High Performance File System
- Lustre based high performance distributed file system
- High scalability, high reliability and availability

Automatic parallelization compiler
- Fortran
- C
- C++

Tools and math libraries
- Programming support tools
- Mathematical libraries

Parallel languages and libraries
- OpenMP
- MPI
- XPFortran

Linux based OS (enhanced for FX series)

PRIMEHPC FX series

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Summary

- Successor to the PRIMEHPC FX10
  - Fujitsu-developed, compatible SPARC64 CPU and Tofu Interconnect
  - High-density packaging
- SPARC64 XI fx
  - Rich micro architecture (32 computing cores + 2 assistant cores)
  - Richer SIMD operations supported
  - High memory bandwidth (with HMC)
- Interconnect
  - Tofu Interconnect 2 is integrated into the CPU
  - Optical connections between chassis

100 petaflops-capable system

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