FUJITSU Supercomputer
PRIMEHPC FX100
Fujitsu has been developing supercomputers over 30 years, and will continue its development to deliver the best application performance.
# PRIMEHPC FX100 design concept

**Designed for massively parallel supercomputer system**
- High performance for a wide range of real applications

**Enhance and inherit K computer features**
- Many-core CPU-based architecture for application productivity
- Enhanced VISIMPACT (hardware barrier synchronization, sector cache, etc.)

**Introduce new technologies to Exascale computing**
- HPC-ACE2: Wide SIMD enhancements
- Assistant cores: Dedicated cores for non-calculation operation
- HMC: Leading-edge memory technology
Over 1 TF high performance processor

- 32 compute cores
- 2 assistant cores: Offloading non-calculation operations → Daemon, IO, non-blocking MPI functions, etc.

HPC-ACE2: ISA enhancements

- Two 256-bit wide SIMD units per core
- 64 bit x 4 / 32 bit x 8 FMA
- Addressing mode (stride load/store, indirect load/store)
- Cross lane operation (compress, permutation)
Hybrid Memory Cube (HMC)

**Excellent byte/flop balance**

- HMC: high performance per watt in small footprint

<table>
<thead>
<tr>
<th>Peak performance per node</th>
<th>K computer</th>
<th>PRIMEHPC FX10</th>
<th>PRIMEHPC FX100</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP perf. (GFLOPS)</td>
<td>128</td>
<td>236.5</td>
<td>Over 1000</td>
</tr>
<tr>
<td>Memory BW (GB/s)</td>
<td>64</td>
<td>85</td>
<td>480</td>
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</tbody>
</table>
## Enhanced Tofu interconnect
- Highly scalable, 6-dimensional mesh/torus topology
- Increased link bandwidth by 2.5 times to 12.5GB/s

## CPU-integrated interconnect controller
- Reduced communication latency
- Improved packaging density and energy efficiency

## Optical cable connection between chassis
- Enable flexible installation
Enhanced VISIMPACT

Technology for hybrid parallelization
- Automatic parallelization technology by Fujitsu’s compiler
- Hardware barrier for fast synchronization

Advantages of hybrid parallelization
- To reduce communication cost in highly parallel programs
- To increase user memory space by reducing communication buffer

Enhanced hardware barriers
- 8 set between 32 cores
CPU memory board

Three identical computation nodes

SPARC64 XIfx

Optical module

HMC
Main unit

2U rack mountable chassis

• High density: Four CPU memory boards per unit (total 12 nodes, over 12 TF)
• Water cooled: High reliability
System rack

- Optical cables
- Coolant hose
- Coolant pipe
System rack: Rear View
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