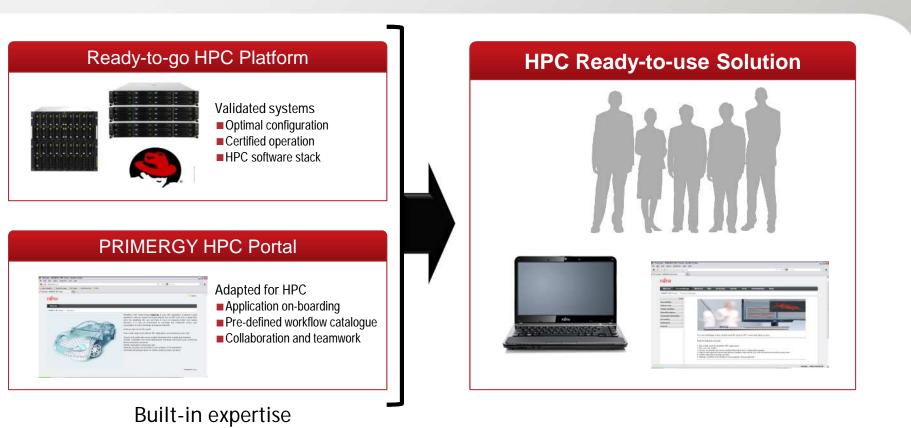


# Ready-to-go with Ready-to-use PRIMERGY x86 – HPC Simplicity

Copyright 2010 FUJITSU LIMITED

# The Concept of HPC Simplicity



Copyright 2010 FUJITSU LIMITED

FUIT



# Ready-to-go systems for HPC

PRIMERGY x86 server configuration and delivery

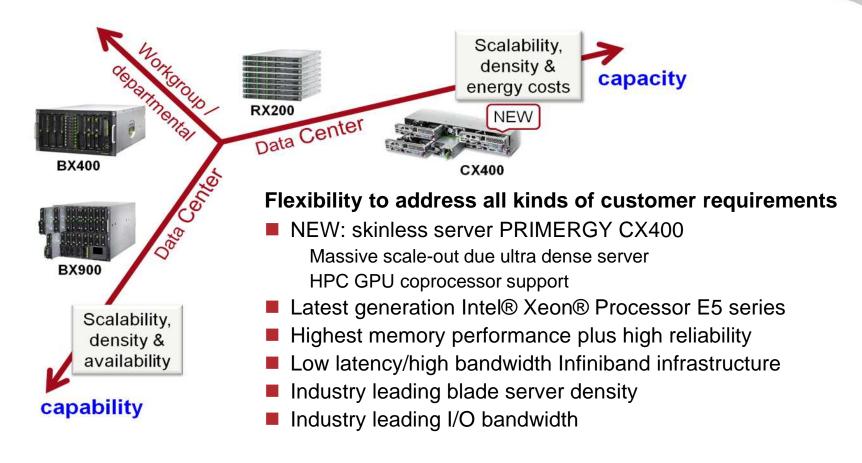
Copyright 2010 FUJITSU LIMITED

#### FUJITSU Building Blocks of PRIMERGY HPC Ecosystem



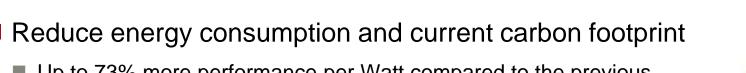
3

# Modular HPC growth potential towards ....



# Most energy efficient server in the world

- Fujitsu PRIMERGY achieves world record in energy efficiency and holds several best in class ratings
  - World record in SPECpower\_ssj2008 by breaking the prestigious milestone of 6,000 overall ssj\_ops/watt
  - http://ts.fujitsu.com/ps2/press/read/news\_details.aspx?id=6092



- Up to 73% more performance per Watt compared to the previous generation means:
  - Up to 33% less energy for the same current performance level to better meet stringent environmental mandates for data centers
  - Up to 66% more workloads on current power budget without stressing current data center cooling





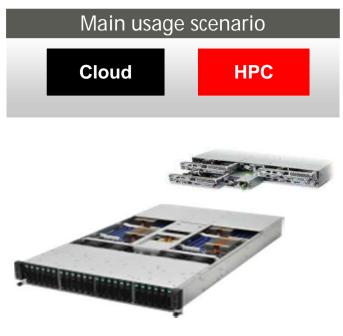
# PRIMERGY CX400 - HPC Design



CX400 combines high performance with high density at lower overall investment

#### High Density / Scalability in 2U Chassis

- HPC requirements optimally fulfilled
  - Up to 4 nodes (1U) or 2 nodes (2U) per 2U chassis
  - 2x Intel® Xeon® E5-2600 processors / node
  - Intel® Xeon® processor E5-2400 node coming soon
  - 16 DIMMs, up to **1600MHz**
  - Redundant, hot-plug PSUs for enhanced availability / lower servicing effort
  - Up to 24x HDD
  - FDR Infiniband interconnect option for highest, most efficient bandwidth and lowest latency
  - **GPU** Option (2U node)
  - Support of Intel MIC Q1/2013 planned



# The Future in High Performance Computing

Intel Xeon Processor 1 core, 2 threads

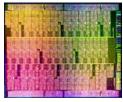


Intel Xeon E5 Processor 8 cores,16 threads





Towards Many Core Architectures



A path towards Exascale enforces a **deployment of parallelism** at each level to the ultimate possible extent

- Node level (distributed memory)
- Multi socket (shared memory on nodes)
- CPU level (number of cores)
- Instruction level (SIMD)

#### Challenges

- Increasing parallelism within the CPU results in demand for higher memory bandwidth and thus greater complexity of the memory hierarchy
- Node parallelism enforce the development and deployment of ultra-high-speed interconnect
- Increasing parallelism towards millions of cores leads to increase in system errors
- Amdahl's Law is more alive than ever and demonstrates that even the smallest portion of serial code dominates (negatively) the overall performance of a code

## Many Core Architectures



### CX400/CX270 and Floating Point accelerators address the core level parallelism



	Intel Sandy Bridge E5-2600	Intel MIC Knights Corner	Nvidia Fermi GPU Tesla 2050
Availability	Today	Q4/2012	Today (Kepler in Q4/2012)
Cores	8 (superscalar)	> 50	Tesla 2050: 448
Programming	Standard languages	Standard languages and OpenCL	CUDA, OpenCL
Architecture*	Multicore	Manycore standalone (possibly) & hybrid	Hybrid

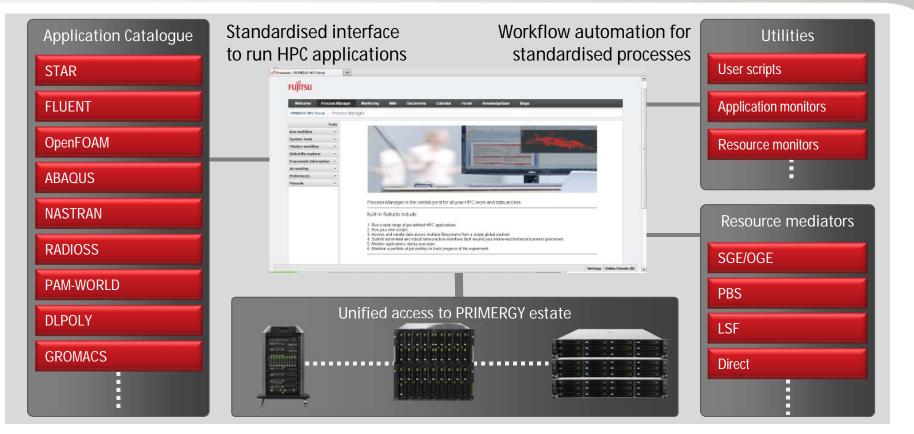
# FUJITSU

# Ready-to-use PRIMERGY HPC solutions

PRIMERGY HPC Portal with expertise in-built

Copyright 2010 FUJITSU LIMITED

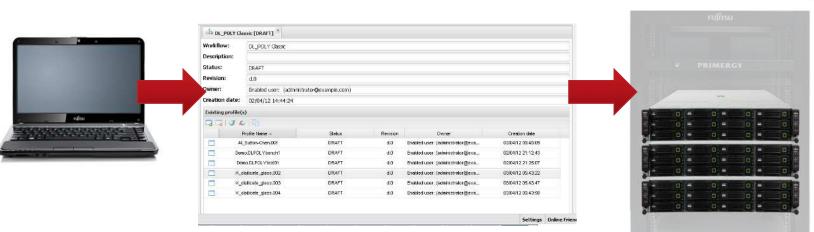
## **PRIMERGY HPC Portal total solution**



Copyright 2012 FUJITSU SYSTEMS EUROPE

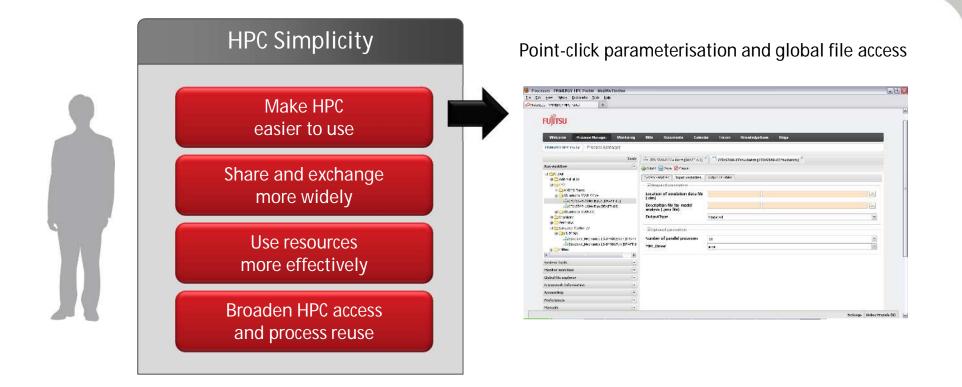
**FUI** 

# **Running an HPC Application**

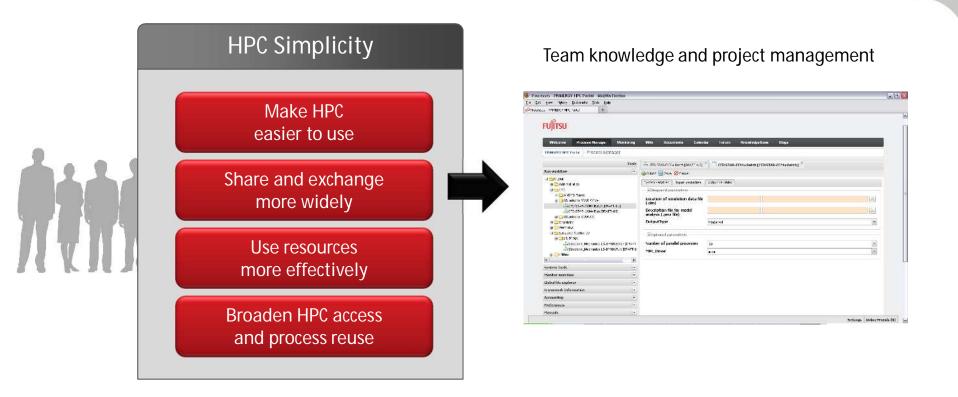


- Experiment inputs managed in job profiles
  - Systematic traceable approach over experiment lifecycle
  - Shareable project team, between service designer and end-users
  - Reduced operations to submit

Usable with minimal learning By end-users with little/no IT knowledge For faster, more accurate setup



FU

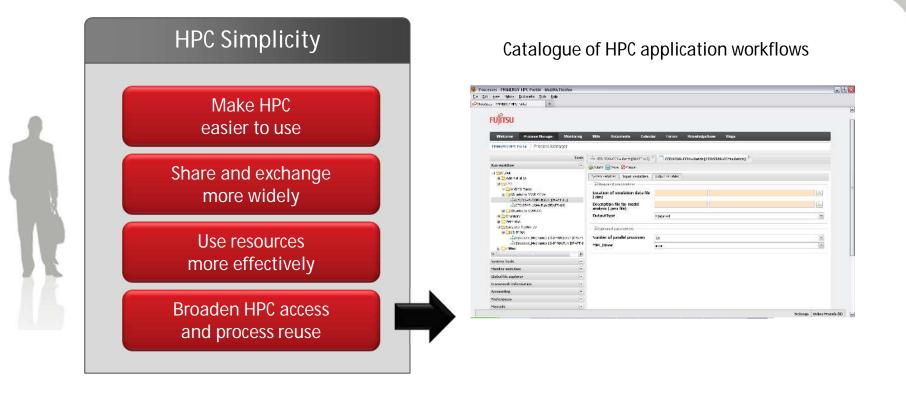


FUI

#### **HPC Simplicity** Project and application usage reporting CESSES PRINERGY HPC PORTAL MICENA - - × La Lat Law lighters factionaries Inde Balo Make HPC THREE HIS WELL FUJITSU easier to use INNERT MADE FOR La Process Michagon Table 👘 (TD 5204-024-08:108-07-02) 👘 🦷 (TD:STAR-DDM-slaten ICD:STAR-COMediaten) Share and exchange Run worldlow Gates Som Otres tal ∰ittabal ⊛CAdmittal al se STORY CANSES Series SCORES STREET \*Beanardamanete more widely Location of simulation data file [.sim] ALCONTRACTOR BALL (NOT 0.2) ACT STAT 204 DA (DAT 0.2) B (2) CLARCE STARCE Description file for model analysis ( gave file) Dutra.#Type III Chanbary B Cover size Undered in State and Vietna 22 all general pressure re-9 (315 P.M. Mercuri Mercures 150-MAERCORA-Use resources Norther of panellel processes in Several Historics LS-D\*HARUN DR-PT 4 MPI\_Drive 1108 - CT - 1864 more effectively System Tank Monitor working formality of Proferences **Broaden HPC access** Settings Unincreasely (0) and process reuse

FU

# FUJITSU



Copyright 2012 FUJITSU SYSTEMS EUROPE

# FUJITSU shaping tomorrow with you