A64FX:
The Fastest Arm-based CPU for HPC

FUJITSU

Fugaku is the Successor to the K Computer

Supercomputer Fugaku
Ranked #1 Green500 2019
Top500, HPCG, Graph500, HPL-AI, 2020

K computer
Ranked Top500 No.1 in 2011

© RIKEN

PRIMEHPC FX1000

PRIMEHPC FX700

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- ■ Fugaku is the successor to K computer that has been in operation for 7 years
- ■ Powered by A64FX, an Arm-based processor designed for HPC
- ■ Commercial models, PRIMEHPC FX1000/FX700, are now available

Fugaku Project

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- Joint Development by RIKEN and Fujitsu

- Flagship supercomputer for Japan

- Arm64-based fast and Green Supercomputer

- Solving the Social issues in the World*

Application Performance

Usability

Energy Efficiency

❖ Fugaku Supercomputer Joins Fight Against Covid-19 (InsideHPC, April 7, 2020)

Fugaku Ultra-Dense Hardware

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Single rack (384 CPUs) = 1 Peta flops

10^{15} floating point operation per second

K computer

100 rack

Fugaku

1 rack

Energy Efficient HPC

- **Supercomputers consume vast amount electric power**
  - K computer 13MW = 15K US households
  - K computer X 100 1.3GW = 1.5M US households
- **Green500, a global ranking for the energy efficiency**
  - Fugaku prototype took No.1 in the Green500 at the SC19,

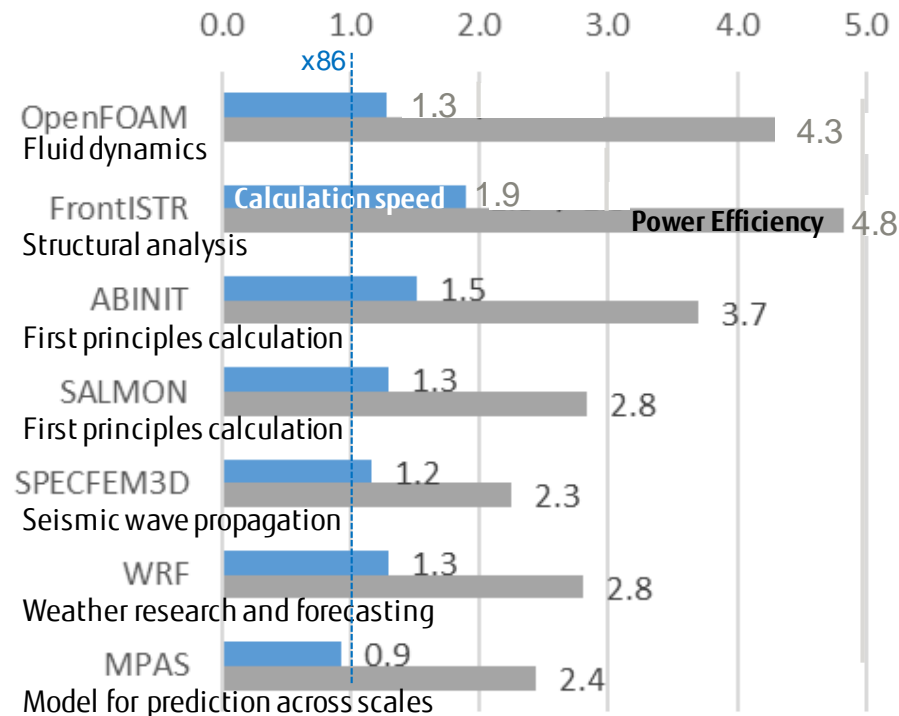| Rank	TOP500 Rank	System	Cores	Rmax (TFlop/s)	Power (kW)	Power Efficiency (GFlops/watts)
1	159	A64FX prototype - Fujitsu A64FX, Fujitsu A64FX 48C 2GHz, Tofu interconnect D , **Fujitsu** Fujitsu Numazu Plant Japan	36,864	1,999.5	118	16.876

  - Fugaku has 40x the performance using only 3x the power of K computer!

High Performance and Power Efficiency

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The power efficiency of major OSS HPC applications

- Measured on A64FX 2.2GHz normalized to IA CPU 2.9 GHz x2

- High efficiency is achieved by energy-conscious design and implementation

	0.0	1.0	2.0	3.0	4.0	5.0

x86

OpenFOAM Fluid dynamics	Calculation speed 1.3	Power Efficiency 4.3
FrontISTR Structural analysis	1.9	4.8
ABINIT First principles calculation	1.5	3.7
SALMON First principles calculation	1.3	2.8
SPECFEM3D Seismic wave propagation	1.2	2.3
WRF Weather research and forecasting	1.3	2.8
MPAS Model for prediction across scales	0.9	2.4

Fugaku ranked at 1ˢᵗ place in all categories

2.8x of 2ⁿᵈ's

4.6x of 2ⁿᵈ's

2.6x of 2ⁿᵈ's
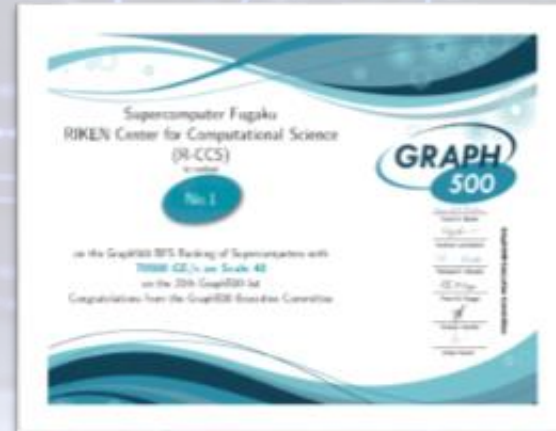
3.0x of 2ⁿᵈ's

Road to Fujitsu's ARM-based Supercomputer

- **Strong collaboration with Arm**
  - Plus Fujitsu's Supercomputer DNA
- **Added features for HPC applications**
  - Optimized toward new supercomputer standard
  - Best performance/power
    - High-performance CPU core for HPC usage
    - High memory bandwidth and B/F ratio
    - High scalability of Tofu interconnect
  - Targeting to not only current HPC but also AI applications
- **Expanding eco-system with HPC technology and applications**
  - Roadmap to general purpose Enterprise
    - Working with Arm/Linux community and OSS

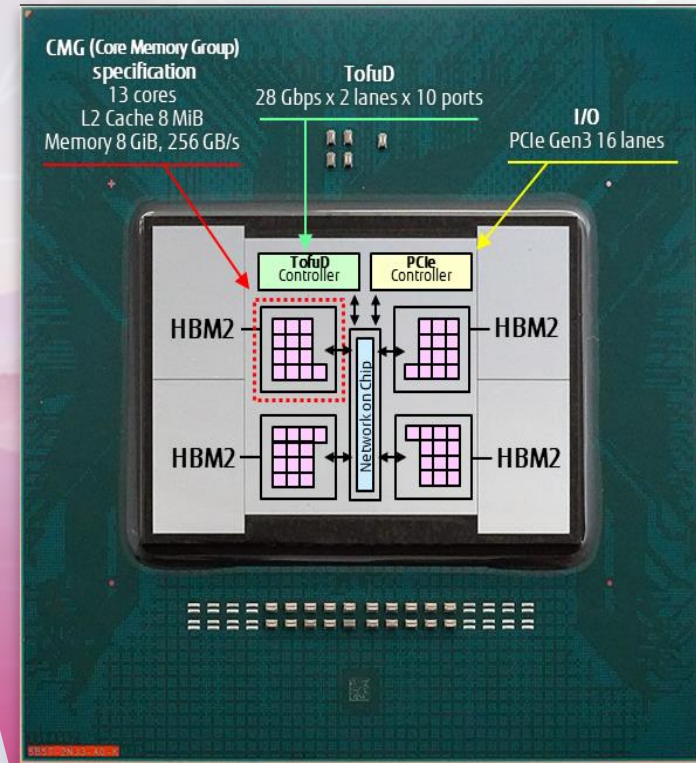Application Performance

Usability

Energy Efficiency

A64FX Overview

- **Fujitsu's Arm Processor**
  - Lead partner with Arm for SVE architecture
  - High speed
  - Low Power Design
- **Goal**
  - CPU with GPU-class performance
  - High performance, high efficiency
    - DP performance >3 TFLOPS, > 90%@DGEMM
    - Memory BW   1024GB/s,   > 80%@STREAM Triad
  - Power efficiency
    - 2-5x performance/watt over IA
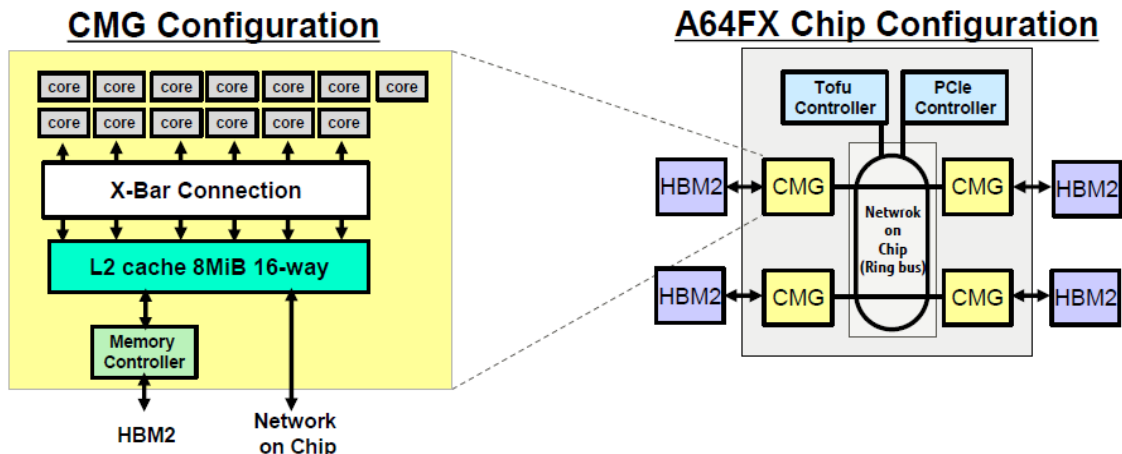   - 16.9GFLOPS/W (HPL)

CMG (Core Memory Group)
specification
13 cores
L2 Cache 8 MiB
Memory 8 GiB, 256 GB/s

TofuD
28 Gbps x 2 lanes x 10 ports

I/O
PCIe Gen3 16 lanes

TofuD Controller   PCIe Controller

HBM2   HBM2

Network on Chip

HBM2   HBM2

Collaboration with Arm

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■ A64FX is the first processor of the ARMv8-A SVE architecture

■ Collaboration with ARM to develop and optimize SVE for a wide range of applications

- 512 bit SIMD
- Added FP16 and INT16/8 dot product for AI applications
- Many other enhancements
  - Gather/Scatter
  - Four operand FMA
  - Predicated operations
  - Math acceleration
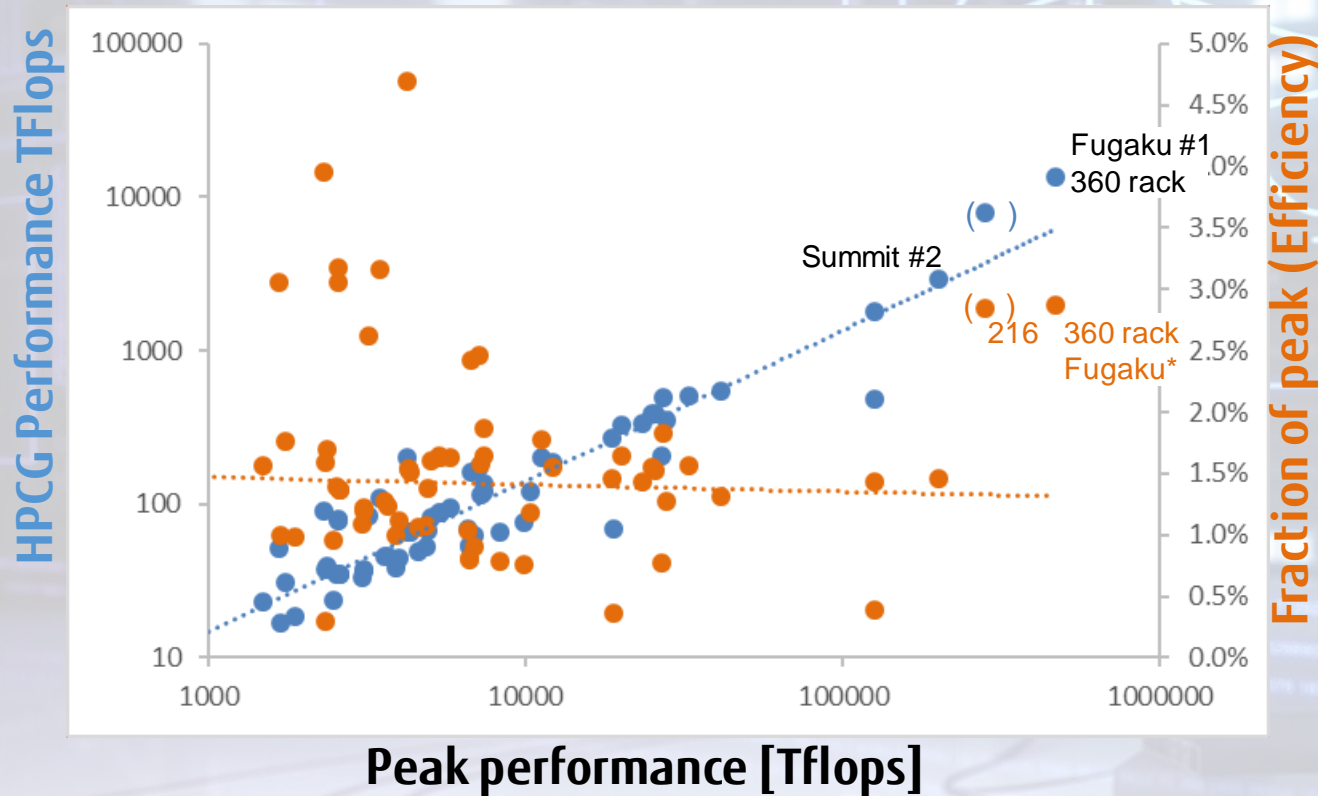 - Compression
  - HW barrier and sector cache

Many Core Architecture

- A64FX consists of four CMGs (Core Memory Group)
  - A CMG consists of 13 cores, an L2 cache and a memory controller
    - One out of 13 cores is an assistant core which handles daemon, I/O, etc.
  - Four CMGs keep cache coherency by ccNUMA with on-chip directory
  - X-bar connection in a CMG maximizes high efficiency for throughput of the L2 cache
  - Process binding in a CMG allows linear scalability up to 48 cores
- On-chip-network with a wide ring bus secures I/O performance

CMG Configuration

core | core | core | core | core | core | core
core | core | core | core | core | core

X-Bar Connection

L2 cache 8MiB 16-way

Memory Controller

HBM2   Network on Chip

A64FX Chip Configuration

Tofu Controller   PCIe Controller

HBM2 — CMG   CMG — HBM2

Netwrok on Chip (Ring bus)

HBM2 — CMG   CMG — HBM2

HPCG results of TOP500 @ ISC20

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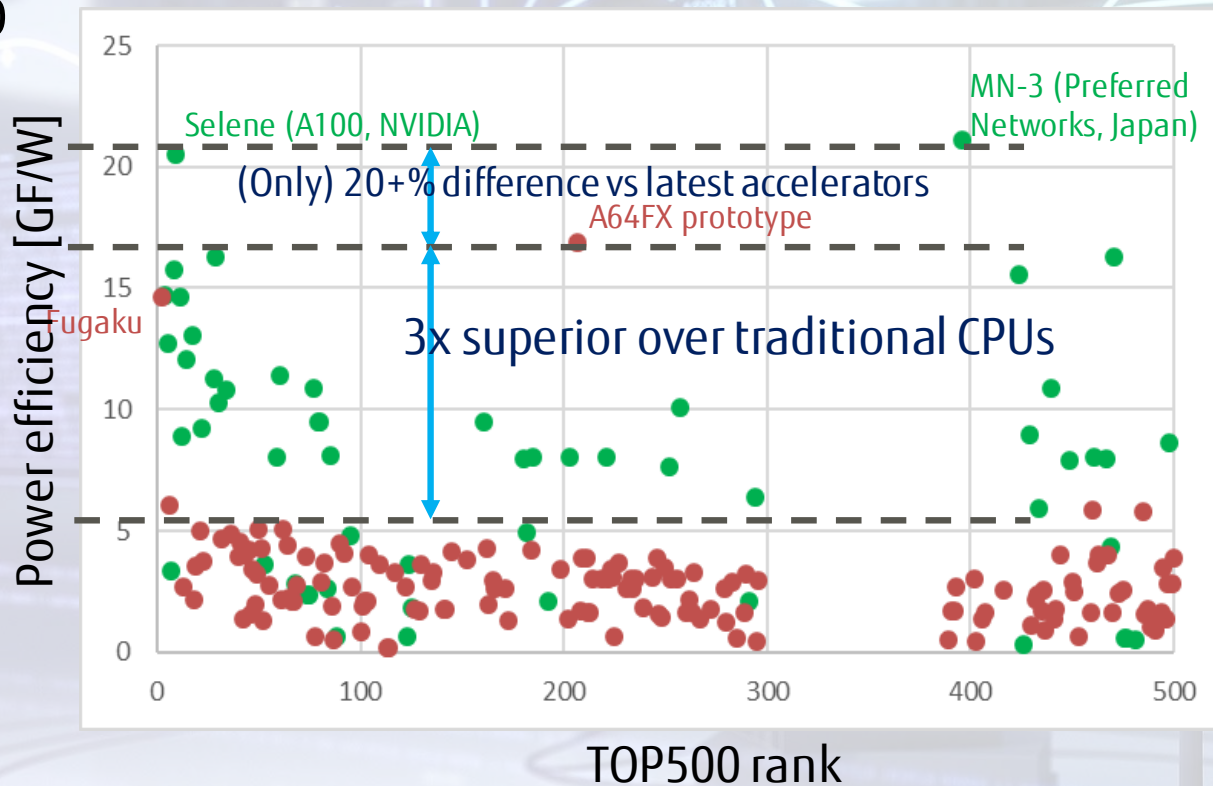■ Fugaku's efficiency is very high at ~3%

Fugaku and A64FX Greenness on TOP500 FUJITSU

- **Power efficiency in GF/W, w/ ACCEL and w/o ACCEL**
  - Top500 - June 22, 2020

A64FX demonstrating power efficiency comparable to latest accelerators, and 3x superiority c.f. traditional CPUs
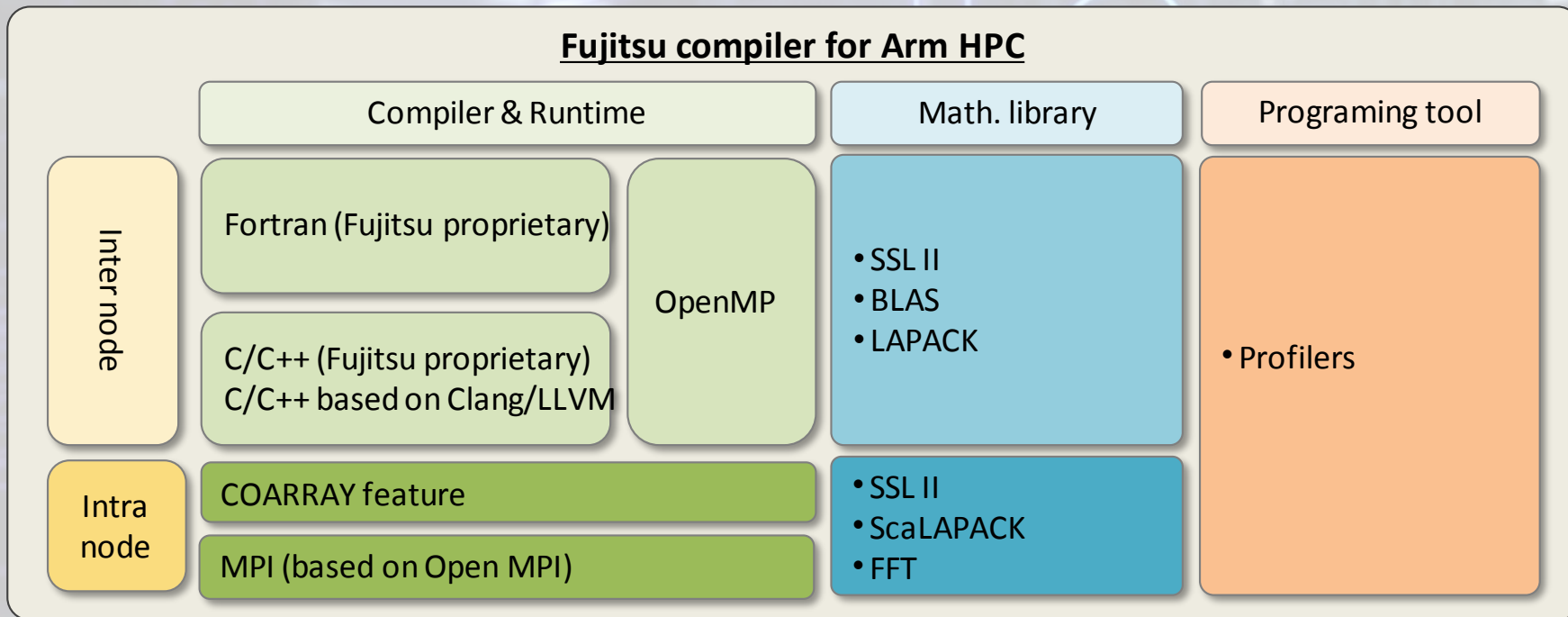
Full Software Stack for the A64FX CPU

- ■ From Kernel, middleware, compiler to HPC application
- ■ OSS stack provides high usability
- ■ Keeping binary compatibility with the other Arm64 v8.2+SVE systems

OpenFOAM, FrontISTR, ABINIT,
SALMON, SPECFEM3D, WRF, MPAS — Applications

Fujitsu Tech. Computing Suite, BCM, Warewulf, PBS, SLURM — Management SW

Fujitsu Compiler Pkg., GCC, Open MPI, Arm Performance Lib. — Programming Env.

Arm Linux RHEL8 — Kernel

A64FX (PRIMEHPC FX1000/FX700) — Hardware

Fujitsu's Programming Environment

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Fujitsu compiler for Arm HPC

Compiler & Runtime	Math. library	Programing tool

Inter node

Fortran (Fujitsu proprietary)

C/C++ (Fujitsu proprietary)
C/C++ based on Clang/LLVM

OpenMP

- SSL II
- BLAS
- LAPACK

- Profilers

Intra node

COARRAY feature

MPI (based on Open MPI)

- SSL II
- ScaLAPACK
- FFT

- Supports major HPC programming environment software and latest international standard
- Supports Arm v8 SVE for optimized application performance

Bottleneck Diagnostics with Fujitsu Profiler

- CPU Performance Analysis information produced by FUJITSU Profiler enables you to
  - observe summarized visualization of activities in the CPU
  - determine bottleneck in the CPU
  - obtain data in the level of loop, procedure, or entire region
- Major part of CPU Performance Analysis information is the cycle accounting graph such as the following
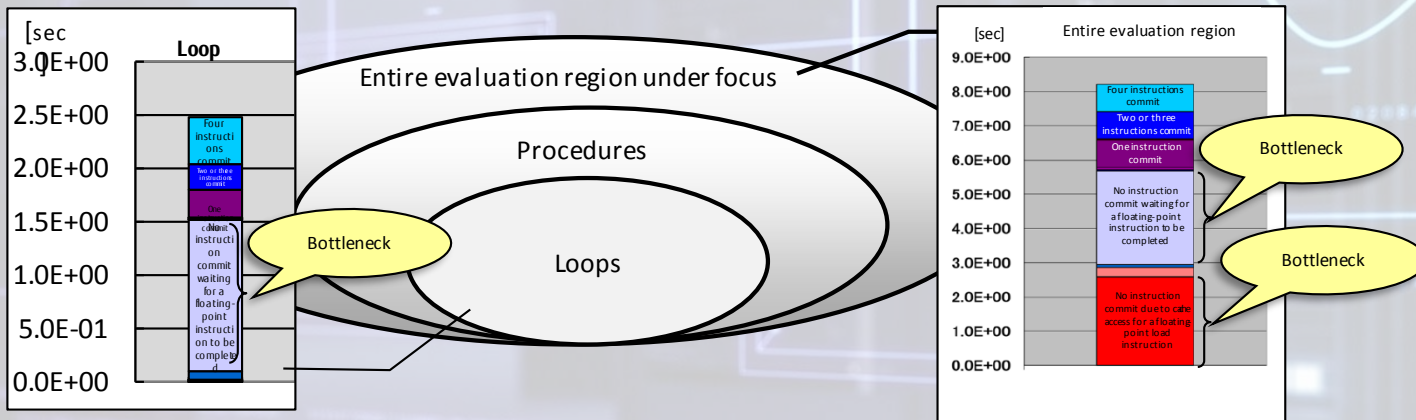
- What is a reason of the bottleneck?
- To what extent can the bottleneck be improved?

CPU Performance Analysis information produced by FUJITSU Profiler is the answer to these questions.

A64FX-based PRIMEHPC Family

PRIMEHPC FX1000

PRIMEHPC FX700

A64FX-based PRIMEHPC Platforms

FX1000

High density custom cabinet,
384 nodes/cabinet, Scale to ~400k nodes
Water cooled,
Tofu interconnect D,
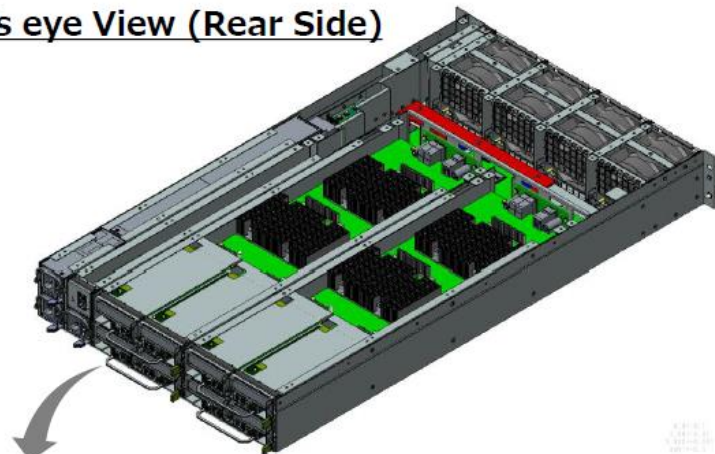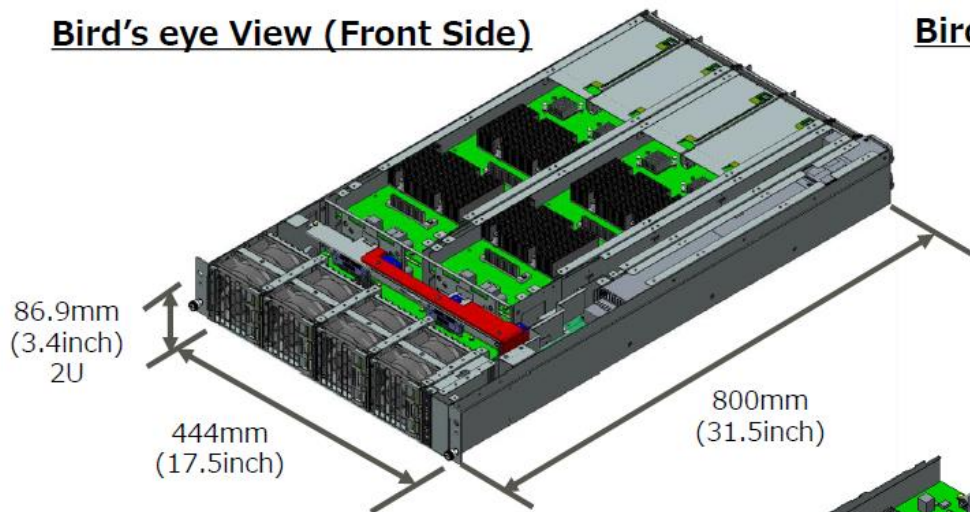Fujitsu software stack

FX700

Standard 19' Rack mount,
8 nodes(=CPU)/2U,
Air cooled,
InfiniBand EDR/HDR100
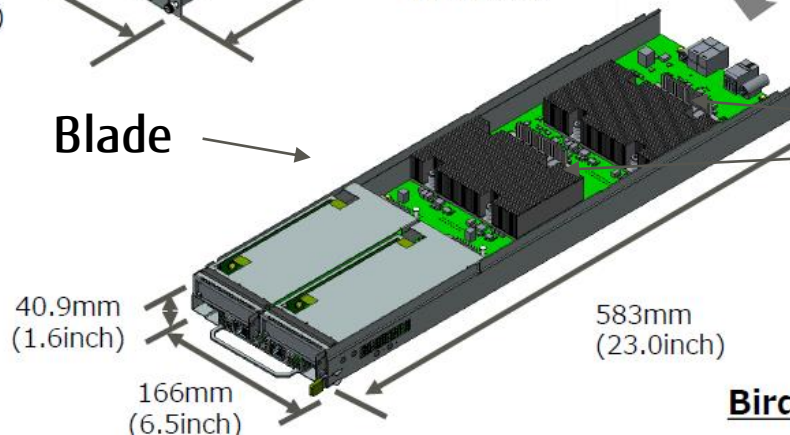Utilize ISV and Open Source

PRIMEHPC FX700 Components

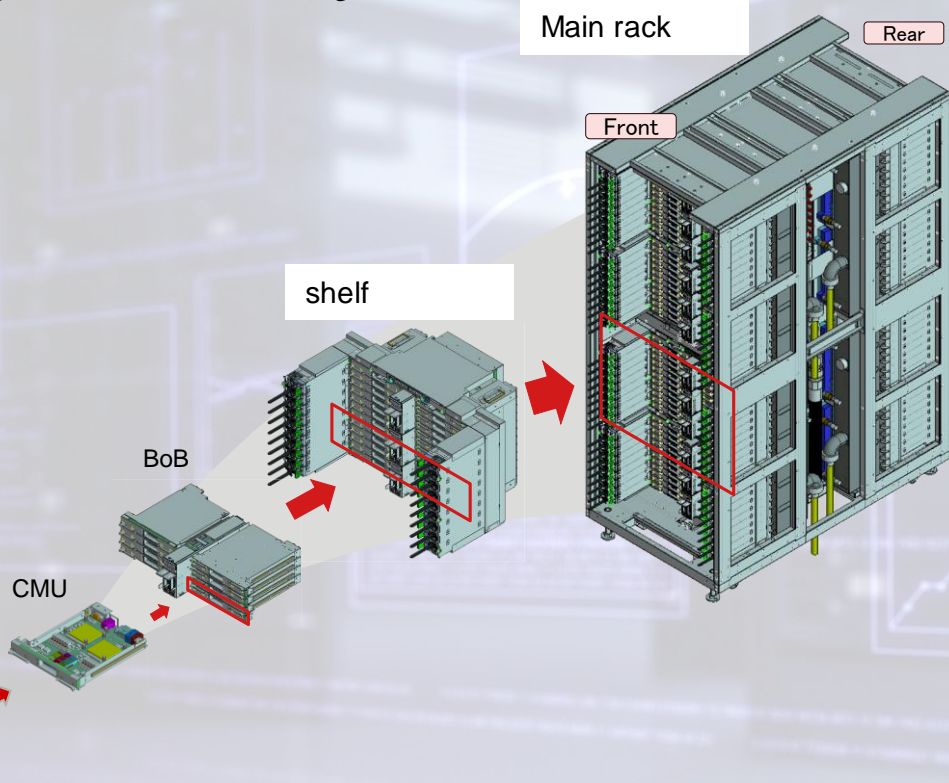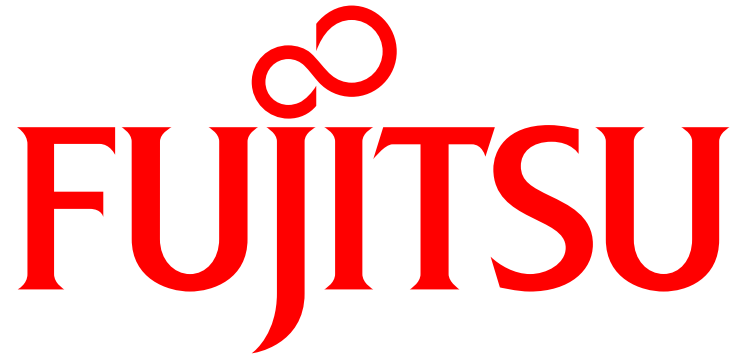**Bird's eye View (Front Side)**

Bird's eye View (Rear Side)

86.9mm
(3.4inch)
2U

444mm
(17.5inch)

800mm
(31.5inch)

Blade

CPU(Node)

40.9mm
(1.6inch)

583mm
(23.0inch)

166mm
(6.5inch)

Bird's eye View of Blade

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System Layout of PRIMEHPC FX1000

Main rack

Rear

Front

shelf

BoB

CMU

CPU

Layer	Node #	description
CPU	1	CPU and Main Memory CPU includes execution cores, assistant cores, L2$, memory controller, interconnect controller (ICC) and PCIe interface
CMU	2	CMU (CPU Memory Unit) consists 2x CPU
BoB	16	BoB (Bunch of Blades) consists 8x CMU
Shelf	48	Shelf consists 3x BoB
Main Rack	384	Main Rack consists 8x shelves

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