FUJITSU Supercomputer PRIMEHPC FX100

PRIMEHPC FX100 provides the ability to address high magnitude problems by delivering over 100 petaflops, a quantum leap in processing performance.

Combining high performance, scalability, and reliability with superior energy efficiency, FUJITSU Supercomputer PRIMEHPC FX100 further improves Fujitsu's supercomputer technology employed in the K computer and PRIMEHPC FX10. The system, from hardware to software, has been fully developed by Fujitsu, thereby delivering high levels of reliability and operability. The system can be flexibly configured to meet customer needs, capable of scaling to over 100 petaflops.

Ultra-high-speed and Ultra-large-scale

The core of the supercomputer, the SPARC64 XIfx processor delivers over 1 teraflops peak performance. Based on the state-of-the-art 20nm semiconductor process technology, 32 compute cores and 2 assistant cores are integrated into a single processor chip. An expansion to the SPARC-V9 instruction set architecture called HPC-ACE2 (High Performance Computing-Arithmetic Computational Extensions 2) features two 256-bit wide SIMD units per core with advanced operation functions, and improves the computational throughput of the processor. HMC (Hybrid Memory Cube) allows a high memory bandwidth of 480GB/s per node and the one-processor-per-node architecture exploits the maximum memory performance. Tofu Interconnect 2 (Tofu2) is integrated into the SPARC64 XIfx processor and enhances node-to-node communication bandwidth to 12.5 GB/s per link with lower latency. Highly scalable Tofu2 enables a system configuration of over 100,000 nodes.

High Density Packaging and Water Cooling

12 nodes are packed into the main unit, a 19-inch 2U form factor chassis. Up to 18 main units can be mounted on a single system rack. Over 90% of the heat is removed by direct water cooling. Lower component temperature achieved by water cooling reduces semiconductor's current leakage, and improves energy efficiency and components' reliability.

Application Performance and Simple Programming Environment

Hybrid parallelization combining MPI and thread parallelization enables efficient memory usage and inter-process communication. However, programming of hybrid parallelized applications requires time and effort. VISIMPACT (Virtual Single Processor by Integrated Multi-core Parallel Architecture) is the technology that simplifies hybrid parallelization. Compilers of FUJITSU Software Technical Computing Suite transform MPI programs to hybrid parallel executions automatically. In addition to this, inter-core hardware barrier and shared L2 cache assist efficient job execution.

Highly Efficient Job Execution

OS or system software interruptions such as daemons cause system noise which results in application performance loss. The two assistant cores of the SPARC64 XIfx processor handle such system interruptions to remove system noise from compute cores' calculation process. They also handle MPI asynchronous communications to shorten process waiting time. With the help of the assistant cores, PRIMEHPC FX100 realizes highly efficient job execution on large scale systems.

High Reliability and Operability

The SPARC64 XIfx processor employs the same high RAS features proven on Fujitsu's mission critical servers. The flexible 6D Mesh/Torus topology of Tofu2 also contributes to overall reliability and availability. FUJITSU Software Technical Computing Suite provides system management, job scheduling, and highly scalable distributed file system functions that realize high operability on large scale systems.

FUJITSU Supercomputer PRIMEHPC FX100 Specifications

CPU	Processor	SPARC64 XIfx
	Architecture	SPARC V9 + HPC-ACE2
	No. of cores	32 compute cores + 2 assistant cores
	Theoretical peak performance	Over 1 teraflops (double precision)
Node	Architecture	1 CPU per node
	Memory capacity	32 GB (HMC)
	Memory bandwidth	240 GB/s (read) + 240 GB/s (write)
	Interconnect	Tofu Interconnect 2
	Interconnect link bandwidth	12.5 GB/s x 2 (bi-directional) per link
Main unit	Form factor	19-inch 2U
	No. of nodes	12
System rack	No. of main units	Up to18 (216 nodes per rack)
Maximum configuration	No. of nodes	Over 100,000
	Theoretical peak performance	Over 100 petaflops (double precision)
	Total memory capacity	Over 3 PB

Contact
FUJITSU LIMITED
Website: www.fujitsu.com