Overview of the SPARC Enterprise Servers















SPARC Enterprise Technologies for the Datacenter

Ideal for Enterprise Application Deployments

- System Overview
- Virtualization technologies
 - > Maximize system utilization
- Advanced RAS
 - > To provide high availability
- Scalability
 - > To provide needed capacity
- Solaris Binary Compatibility
 > Preserve previous investments

New SPARC Enterprise Family



Product Features

	M4000	M5000	M8000	M9000	
Processor	2.15GHz, 5MB L2\$	2.15GHz, 5MB L2\$	2.28GHz, 5MB L2\$ 2.4GHz, 6MB L2\$	2.28GHz, 5MB L2\$ 2.4GHz, 6MB L2\$	
	Max 4 (8 core)	Max 8 (16 Core)	Max 16 (32 core)	Max 64 (128 Core)	
Memory	Max 128GB	Max 256GB	Max 512GB	Max 2TB	
Internal Disks	Max 2 (2.5" SAS)	Max 4 (2.5" SAS)	Max 16 (2.5" SAS)	Max 64 (2.5" SAS)	
PCI Slots	4 PCle 1 PCI-X	Max 8 PCle Max 2 PCI-X	Max 32 PCIe	Max 128 PCle	
Domains	Max 2	Max 4	Max 16	Max 24	
Peak Bandwidth	32 GB/s	64 GB/s	184 GB/s	737 GB/s	
Redundant Service Processor			\checkmark	\checkmark	
Dynamic Reconfiguration	\checkmark	\checkmark	\checkmark	\checkmark	
Hot Swap CPU/Memory			\checkmark	\checkmark	
Full Redundancy			\checkmark	\checkmark	
Upgradable to faster CPUs	\checkmark	✓	\checkmark	\checkmark	
Memory Mirroring	\checkmark	\checkmark	\checkmark	\checkmark	

SPARC64 VI Architecture

CPU Chip



SPARC64 VI Details

Process: 90nm Transistors: ~500M Clock Speed: 2.4GHz Cores/Socket: 2 Threads/Core: 2 Thread Model: VMT L1\$: 128K I\$ 128K D\$ / core L2\$: 6MB internal shared Power: 120W

SPARC64 VI Processor Architecture

- 4 threads per processor
 - > Two SPARC V9 cores
 - > Two threads per core
- Out-of-order execution for improved single-thread performance
- 128 KB L1 caches (Instr & data)
- Up to 6 MB L2 cache
- New System Interface
- Up to 2.4 GHz
- Power: 120W @ (1.1V & 2.4 GHz)



M8000, M9000 Backplane Interconnect



Consolidation and Virtualization

...Improves system utilization

SPARC Enterprise Virtualization Spectrum





Choice!

Change this...







24 Servers

24 Domains

24 Containers

Partitioning Feature for Server Consolidation

- Ability to configure the system board to support one partition, or up to 4 partitions
- Each partition runs a separate copy of Solaris
- Dynamic Reconfiguration (DR) feature enables highly flexible resource reallocation

One Domain Config 4 CPUs in one Domain Four Domain Config One CPU per Domain





Dynamic Domains: Leading to Better Resource Utilization



RAS

... Mainframe-class reliability at open system prices

M4000 to M9000 RAS

Solaris 10 FMA

- Auto reconfiguration on failure
- Bad page retirement
- Integration between SP and OS

Processor

- Instruction level retry
- Parity and ECC protection on chip cache
- Cache memory dynamic degradation

Service Processor

- Hot-swap redundant Service Processor on DC Systems
- Redundant Ethernet connections
- Diagnosis to the FRU level on first fault

Solaris

System

Memory

Processor

System Power and Cooling

- Redundant hot-swap fans and AC/DC power
- Redundant DC/DC power
- Optional Dual Grid power

System IO

- PCI-Express end-to-end CRC
- Hot-swap PCI Express cards
- Redundant, hot-swap boot disks

Memory

- ECC Protection
- Extended ECC
- Memory mirroring

Highly Reliable Processor Development Technology

Synergy of Platform and Semiconductor Technologies

Synergy

Processor Development Technology

- Fujitsu's mainframe development technology continuity
- Fujitsu skills and innovations enable of high performance and high reliability implementation

Semiconductor Technology

- 90nm technology
- 10 layer copper writing
- Low-k^{*} dielectric insulation
- High accumulation and low power consumption





* Low-k layered membrane. Makes such minute wiring possible

World-Record Performance and Mainframe-Heritage High Reliability Technology

RAS Functions at a Mainframe Level

Systems Incorporates All Needed RAS Functions (*) for Mission Critical Applications



Error detection and correction logic implemented across server HW enables swift and exact treatment Unplanned downtime reduced !

* Data integrity assurance, error correction and recovery, error recording for investigation, etc.

Assurance of Data Integrity Between Server Components

ECC Protection in CPU and Main LSI Units (Both Address/Data) All One Bit Errors Are Detected and Corrected



- Data transferred between CPU/Main LSI/Memory(*3) is protected by ECC (Shown by)
- Data transferred between IO controller and PCI-Express slots is protected by CRC (*4)

- *1 Error check function used in parallel data transfer. Error detection & correction of one bit errors. Error detection of multi-bit errors.
- *2 Automatic one bit error detection.
- *3 Only data transferred between memory access controller and memory is checked by ECC. Address part not checked.
- *4 Error check function used in serial data transfer. Cyclic Redundancy Check. Automatically detects and corrects one bit errors and detects two bit errors.

Continuous Operation (vs. IBM System p5)



SPARC Enterprise Features for Continuous Operation

- Predictive error monitoring with self-diagnosis feature
- Partial power shut-down feature
- Automatic isolation of defective components

Continuous Operation (vs. HP Superdome)



SPARC Enterprise Features for Continuous Operation

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Scalability

... Meeting customer's toughest compute problems

Proven Solaris Scalability

- 15 years of SMP optimization
- Studio12 compilers optimized for SPARC64 VI
 Studio compilers due out in late Q2, CY2007
- Scales up to 144 cores today
- Industry-leading ISV support
- Binary compatible with previous Solaris versions

SAP-SD: M8000 Sets World Record

Fastest SPARC Servers !

🕭 Sun **FUITSU** -----**SPARC Enterprise M8000** server with 16 x 2.4 GHz **SPARC64 VI processors** achieved 7,300 users • Beats IBM p-570 by 32% **Beats HP Integrity** Superdome by 30%

^[1] SAP-SD: Disclosure

Two-tier SAP Sales and Distribution (SD) standard SAP ERP 2005 application benchmark: Sun SPARC Enterprise M8000 (16-way, 16 processors, 32 cores, 64 threads) 7,300 users, 16 2.40 GHz SPARC64 VI, 256 GB, Oracle 10g, Solaris 10, Cert. XXXXXX, HP Integrity Superdome-16 (16-way, 16 processors, 32 cores, 64 threads), 5,600 users, 16 1.6 GHz Dual-Core Intel Itanium 2 9050, 256 GB, SQL Server 2005, Windows Server 2003 Datacenter Edition, Cert. 2006090; IBM p5 570 (16-way, 16 processors, 16 cores, 32 threads), 5,520 users, 16 2.2 GHz POWER5+, 128 GB, DB2 UDB 8.2.2, AIX 5.3, Cert. 2006044; IBM p5 595 (64-way, 64 processors, 64 cores, 128 threads), 23,456 users, 64 2.3 GHz POWER5+, 512 GB, DB2 9, AIX 5.3, Cert. 2006045. SAP, R/3, mySAP reg TM of SAP AG in Germany and other countries. More info www.sap.com/benchmark.

^[1] SAP-SD: Disclosure (w/o cert)

Two-tier SAP Sales and Distribution (SD) standard SAP ERP 2005 application benchmark: SPARC Enterprise Server M8000, 16 processors / 32 cores / 64 threads, SPARC64 VI 2.4 GHz, 256 KB L1 cache, 6 MB L2 cache on-chip, 256 GB main memory. Number of benchmark users & comp.: 7,300 SD (Sales & Distribution) Average dialog response time: 1.98 seconds Throughput: Fully Processed Order Line items/hour: 731,330 Dialog steps/hour: 2,193,990 SAPS: 36.570 Average DB request time (dia/upd): 0.018 sec / 0.041 sec CPU utilization of central server: 99% Operating System central server: Solaris 10 **RDBMS:** Oracle 10g SAP ECC Release: 6.0. The SAP certification number was not available at press time and can be found at the following Web page: www.sap.com/benchmark.

- IBM p5 570 (16-way, 16 processors, 16 cores, 32 threads), 5,520 users, 16 2.2 GHz POWER5+, 128 GB, DB2 UDB 8.2.2, AIX 5.3, Cert. 2006044; IBM p5 595 (64-way, 64 processors, 64 cores, 128 threads), 23,456 users, 64 2.3 GHz POWER5+, 512 GB, DB2 9, AIX 5.3, Cert 2006045. SAP, R/3, mySAP reg TM of SAP AG in Germany and other countries. More info www.sap.com/benchmark.
- HP Integrity Superdome-16, (16 processors, 32 cores, 64 threads), 5,600 users, 16 1.6 GHz Dual-Core Intel Itanium 2 9050, 256 GB, SQL Server 2005, Windows Server 2003 Datacenter Edition, Cert.2006090. SAP, R/3, mySAP reg TM of SAP AG in Germany and other countries. More info www.sap.com/benchmark.

Linpack: M9000 Breaks a Teraflop!

- The SPARC Enterprise M9000, with 64 2.4GHz processors
- Delivering a score of 1.016 TFLOPS on the Linpack benchmark (HPC). [2]
- Over 2X faster than IBM p5 595 (32 x 1.9GHz POWER5)
- 29% faster than HP's Itanium 2 based Superdome (64 x 1.6GHz/24MB)

SPEComp: Parallel Computer Leadership

- Sun Fire M8000 running at 2.28 GHz tops all results at 32 threads. [3]
 - > Beat the best IBM result on SPECompMbase2001 by 20%
 - > Beat the IBM p5 560Q RedHat4 solution on SPECompMbase2001 by 53%
- M9000 with 2.4GHz SPARC64 VI processors beat the best IBM result on SPECompL2001
- M9000 with 2.4GHz SPARC64 VI processors beat the best Itanium 2 based result on SPECompL2001

SPECint_rate2006

Up to 93% Scalability

System	Processor	Ghz	Chips	Cores	Base	Peak
M4000	SPARC64 VI	2.15	4	8	66	81.6
M5000	SPARC64 VI	2.15	8	16	124	158
M8000	SPARC64 VI	2.28	16	32	285	335
M8000	SPARC64 VI	2.4	16	32	298	352
M9000	SPARC64 VI	2.28	64	128	1060	1220
M9000	SPARC64 VI	2.4	64	128	1110	1290

Solaris 10

... The most advanced operating system on the planet

Solaris 10 for SPARC Enterprise

Protecting Customer Investments

- Binary compatibility guarantee
 > 10 Years since Solaris 2.6
- Free and open source
 > 800,000 developers
- Secure out of the box
 - > Solaris trusted extensions
- Extreme Observability: DTrace
 - > Problems solved in minutes, not days

Predictive Self-Healing



Stops problems before they happen

Self-diagnosis in milliseconds

Fine-grained recovery

Zero source code changes required

Solaris Fault Manager

Solaris Service Manager

Solaris ZFS

A New Way to Manage Data

End-to End Data Integrity

64-bit Checksums, Copy-on-Write Transactions

Immense Data Capacity

Worlds First 128-bit File System

Easier Administration

Pooled Storage Model – No Volume Manager

> Huge Performance Gains

Especially Architected for Speed



Roadmap

Processor Roadmap





