Attachment

FX1 Key Features & Specifications

(FX1 is sold only in Japan.)

Features

1. Fujitsu's high-performance SPARC64™ VII CPU

- Latest 65 nm processing technology
- Back-gate bias control for lower power consumption
- L2 cache shared between cores
- High-speed barrier mechanism between CPU cores

2. Compact installation of computation nodes

- FX1 configuration
  - Four sets of computation nodes consisting of single CPUs housed in a 5U chassis.
- Interconnects
  - One DDR InfiniBand™ interface per computation node (four ports per chassis unit).
- High-speed barrier synchronization between nodes, reduction-calculation function implemented in hardware (optional)

3. Fast memory throughput

- Custom chipset developed in-house
- Sufficient memory bandwidth to CPU performance

4. New compiler technology for the multi-core era

- Automatic parallelization without special multicore-oriented programming
- Advanced automatic prefetch optimization to maximize memory performance
- Advanced instruction scheduling designed specifically for the SPARC64 VII

5. Excellent usability

- Software acceleration of programs designed for vector supercomputers
  - Even programs originally designed for vector supercomputers, which typically have poor efficiency on scalar machines, are accelerated without modification.
- Easy software migration
  - MPI programs running on PC clusters can be quickly re-implemented utilizing re-translation.

6. Data integrity

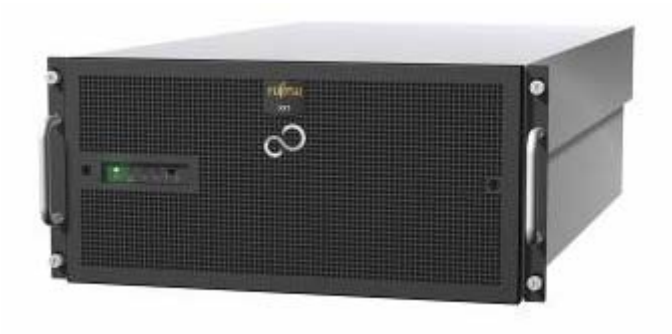
ECC is widely implemented throughout system—in CPU, memory, system bus, etc.—to correct errors. There is no impact on system operations. Main memory is protected with "extended ECC" in addition to ECC. Data will be preserved even in the event of a multi-bit error when a memory chip fails.

Specifications

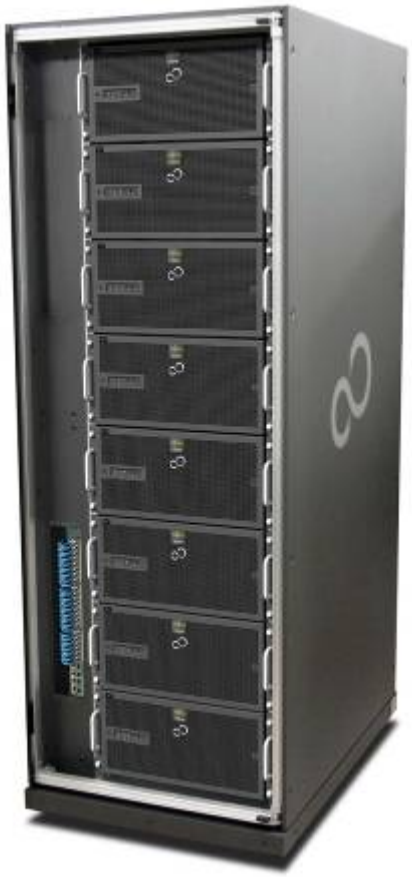
CPU	Processor	SPARC64™ VII
	Clock rate	2.5 GHz
	Cache	L1: 64 KB instruction cache, 64 KB data cache per core L2: 6 MB per CPU, shared
	Cores	4 per CPU
	Performance	40 GFLOPS per CPU
	Simultaneous multi-threading	2 threads per core
	Barrier synchronization	CPU-wide high-speed barrier mechanism between cores
Node	CPUs	1
	Memory capacity	Max 32 GB
	Memory error-checking	ECC, extended ECC
	Memory bandwidth	40 GBps
	Interfaces	73 GB x 1 hard drive; InfiniBand™ HCA (2 GBps) x 1; 1000baseT x 2
Chassis	Nodes	4
	Dimensions (excluding front grab handles)	443 x 800 x 220 mm (rackmount 5U)
	Weight	70 kg
	Power supply	AC 200–240 V AC, 50/60 Hz
	Power consumption	Max 2,213 W; Apparent power 2,236 VA
	Maximum thermal generation	7,988 kJ/h
	Energy-saving efficiency as per Japan's Energy Conservation Law	0.0155 (Section C)

[Images]

- Chassis exterior



- Populated rack



- CPU/memory unit