Fujitsu’s data converter technology has brought forward the enablement of real 100G transport networks. This technological progress continues with Fujitsu’s 55-65 GSa/s 8-bit CMOS DAC.

Targeting highly integrated 100/200G optical transceiver devices the challenge is to enable greater functionality whilst staying within a stringent power budget. This is achieved largely due to the high sample rate of the DAC coupled with the IPs availability in CMOS technology which allows for a compact low power solution.

Fujitsu’s existing CHAIS ADC IP macros in 65nm and 40nm have provided the opportunity to combine features such as soft decision FEC with high speed ADCs to enable feature-rich receiver designs. This reduces the chip count, in turn reducing power consumption and total footprint while increasing reliability and flexibility. These benefits are further enhanced when the DACs are included due to the Transmit features which can be realised using the 4-channel DAC macro with its integrated PLL. This DAC integration mitigates the requirement for a separate modulation-encoding multiplexer thus extending the power consumption, footprint, flexibility and reliability advantages.

**DAC Macro Features**
- Fujitsu 40nm Technology
- Resolution : 8-Bit
- 4 Channels (2 x IQ pairs)
- Sampling Rate : 55 – 65 GS/s
- Power Supply : 1.8V, 0.9V, -0.9V
- Power Consumption : 0.75W/ch
- ENOB: 6.5 (-6dBFS sinewave at ~8GHz)
- Output current: 6mA
- > 13GHz -3dB Output Bandwidth
- 2’s Complement Data Format
- Digital Input: 128 x 8-bit data words (1024 bit) @ FS/128 per DAC
- FS/128 output clock to core
- 2GHz Input Reference Clock
- Internal offset cancellation at start-up
- Designed for flip-chip packages

Full DAC macro block diagram
Applications

- 40G/100/200G Communications Systems
- Test Equipment

Test Chip (Leia)

Test chips for the 55-65 GSa/s 8-bit DAC (codenamed Leia) will be available providing all 4 channels of the 40nm CMOS DAC macro. Each of these channels has RAM at its input which is used to store 256K X 8 bit samples to the DAC channel. This RAM can be loaded with user defined waveform data to send through the DAC channels. Control / programming functions and RAM read/write operations are all performed via an SPI interface. There are several storage modes available which enable control of the RAMs from external triggers.

Development Kits (Leia-DK)

A development kit to accompany the Leia test chip will be available for the evaluation of the DAC IP (codenamed Leia-DK).

Each kit includes:
- Evaluation board with choice of test chip being solder mounted or with socket for easy replacement
- Mains power supply and voltage regulator board
- Interconnect leads/boards
- Windows GUI Software
- Access to DAC outputs via SMPM connectors
- On-board programmable clock distribution circuitry

The kit includes everything needed to minimise the time taken to get started. A USB interface is provided on the evaluation board for easy connection to a PC.

Part Numbers

- LEIA-ES – DAC macro test chips
- LEIA-DK – This evaluation board is supplied with a solder-mounted LEIA-ES test chip.
- LEIA-DK-SOCKET – This evaluation board is supplied with low inductance sockets fitted. This allows easy replacement or swapping of LEIA-ES test chips. The LEIA-ES test chips are sold separately.