GRAPHICS CONTROLLERS
MB88F33X INDIGO2(-X)

APIX PCB-DESIGN GUIDELINE
REV1.5
APPLICATION NOTE
## Revision History

<table>
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<tr>
<th>Rev</th>
<th>Date</th>
<th>Author</th>
<th>Description</th>
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<tr>
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<td>CD</td>
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<td>• Common Mode Chokes recommendation changed</td>
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<td>• Added reference to Application Note regarding APIX Cable Assembly Requirement from INOVA</td>
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<td>• Extended layout rules regarding ground recommendations</td>
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<td>1.5</td>
<td>2014-07-17</td>
<td>AP</td>
<td>• One common ground, separation not longer recommended</td>
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<tr>
<td></td>
<td></td>
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<td>• Oscillator layout example</td>
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This document contains 22 pages.
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1 Introduction

The MB88F33x ‘Indigo2(-x)’ graphics controller uses the Automotive Pixel Link (APIX™) from Inova Semiconductors as an interface to other Fujitsu controllers as well as to discrete transmitters from Inova Semiconductors or other graphic controller/processor products with an integrated APIX interface. Due to the fact that the APIX interface uses a serial link with up to 3 GB/s transfer rate, it is mandatory to obey certain rules for the layout and when selecting components.

This design guide describes design restrictions and recommendations regarding signal wiring and the electrical power system of the APIX interface in MB88F33x ‘Indigo2(-x)’. For more details about the device features and its relevant settings, please refer to the MB88F33x Hardware Manual. In addition, some critical components are described and requirements for the power supply module are discussed. Reference Designs (schematic and layout) can be purchased directly from Inova Semiconductors for extensive testing, measuring and evaluation.

This application note supports designers and answers the most common questions. It is not intended to replace the designer's own responsibility nor can it guarantee optimized operation conditions.
## 2 APIX Pins

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>62</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
<tr>
<td>63</td>
<td>XI</td>
<td>Crystal reference in (or clock ref in)</td>
</tr>
<tr>
<td>64</td>
<td>VDEA_PLL</td>
<td>APIX supply 3.3V (Oscillator, PLL, Input Stage)</td>
</tr>
<tr>
<td>65</td>
<td>XO</td>
<td>Crystal reference out</td>
</tr>
<tr>
<td>66</td>
<td>VDDA_PLL</td>
<td>APIX supply 1.2V (XTAL, PLL digital)</td>
</tr>
<tr>
<td>67</td>
<td>VDDA_VCO</td>
<td>APIX supply 1.2V (VCO)</td>
</tr>
<tr>
<td>68</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
<tr>
<td>69</td>
<td>SDINRP</td>
<td>Serial Data Input Rx (positive)</td>
</tr>
<tr>
<td>70</td>
<td>VCMR</td>
<td>Common Mode decoupling</td>
</tr>
<tr>
<td>71</td>
<td>SDINRM</td>
<td>Serial Data Input Rx (negative)</td>
</tr>
<tr>
<td>72</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
<tr>
<td>73</td>
<td>VDDEA</td>
<td>APIX supply 3.3V (Input Stage)</td>
</tr>
<tr>
<td>74</td>
<td>SDOUTRM</td>
<td>Serial Data Output Rx (negative)</td>
</tr>
<tr>
<td>75</td>
<td>SDOUTRP</td>
<td>Serial Data Output Rx (positive)</td>
</tr>
<tr>
<td>76</td>
<td>VDDEA</td>
<td>APIX supply 3.3V (Input Stage)</td>
</tr>
<tr>
<td>77</td>
<td>VDDA</td>
<td>APIX supply 1.2V (RX, TX, PLL analog)</td>
</tr>
<tr>
<td>78</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
<tr>
<td>79</td>
<td>SDINLTP</td>
<td>Serial Data Input Loop through (positive)</td>
</tr>
<tr>
<td>80</td>
<td>SDINLTM</td>
<td>Serial Data Input Loop through (negative)</td>
</tr>
<tr>
<td>81</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
<tr>
<td>82</td>
<td>VDDA</td>
<td>APIX supply 1.2V (RX, TX, PLL analog)</td>
</tr>
<tr>
<td>83</td>
<td>SDOUTLTM</td>
<td>Serial Data Output Loop through (negative)</td>
</tr>
<tr>
<td>84</td>
<td>SDOUTLTP</td>
<td>Serial Data Output Loop through (positive)</td>
</tr>
<tr>
<td>85</td>
<td>VDDA</td>
<td>APIX supply 1.2V (RX, TX, PLL analog)</td>
</tr>
<tr>
<td>86</td>
<td>VSSA</td>
<td>APIX Ground, connect to common Ground</td>
</tr>
</tbody>
</table>

Table 1: APIX Pin Description
3 Power Supply

3.1 Schematics

The MB88F33x APIX interface requires a clean supply. Therefore the supply should be filtered using APIX-related components as shown in Figure 1. Switched mode power supplies can generate spikes at very low source impedances. These are difficult to filter using capacitors only. A series inductor (ferrite) is therefore recommended, as shown.

VDDA could be fed from the same 1.2V supply as used for the core supply (VDD).

The 1.2V VDD for the core should be sourced from a clean supply. A switched mode power supply should be filtered with a series inductor. Note that a suitable ESD clamp may be required to ensure a low resistance path for ESD.

![Figure 1: Supply circuitry](image)
APIX Supply Noise Protection:
It is recommended to place a decoupling capacitor at the star point between core and APIX supply. This capacitor routes noise from the digital core to ground which prevents its coupling into the APIX supply.

![Figure 2: Supply circuitry VDD, VDDA](#)

### 3.2 Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Description, Part No</th>
<th>Placement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ferrite</td>
<td>e.g. WE742792656, Murata BLM18PG471SN1</td>
<td>Close to supply pins</td>
</tr>
<tr>
<td>High-frequency bypass capacitors (1nF to 100nF)</td>
<td>Low ESR, low ESL ceramic with smallest package (X7R or NP0)</td>
<td>Within 1 cm of each supply pin, better directly at supply pins</td>
</tr>
<tr>
<td>Low-frequency bypass capacitors (1uF to 10uF)</td>
<td>Low ESR, low inductance (tantalum, aluminium electrolyte)</td>
<td>Within 8 cm of each supply pin</td>
</tr>
</tbody>
</table>

Table 2: Power supply components

### 3.3 Layout Rules
- Use power and ground planes instead of wires.
- Use minimal spacing between the power and ground planes to minimize their inductance.
- Use one common ground. Avoid ground currents flowing under the APIX circuitry.
- Use PCB traces of the bypass capacitors as short as possible to minimize the total self inductance. Reduce the loop area enclosed by the vias (see Figure 3).

![Figure 3: Optimal via placement](#)
4 Downstream and Upstream Circuitry

4.1 Schematics

Depending on the application and system set up, there are two recommended ESD protection circuitries. Figure 4 shows an example schematic for the MB88F33x APIX pins and connector with ESD protection at the connector. This variant is the better choice for good ESD protection.

Figure 4: Signal circuitry of the APIX interface – option 1
In the second variant, shown in Figure 5, the ESD protection is between the device and the coupling capacitors. This concept allows a ground offset between RX and TX units. Additional resistors are needed for cable discharge.

![Figure 5: Signal circuitry of the APIX interface – option 2](image)

The previous schematics have to be applied for both RX and TX loop-through interface.

**Common mode chokes:**

Common mode chokes cause additional attenuation and change the transmission line impedance. Therefore they should not be applied for APIX signal lines.

Common mode rejection is provided by cable shielding.

**Termination of unused daisy chain:**

If the daisy chain (loop through) is not used, a 100 Ohm resistor should be placed between SDOUTLTP and SDOUTLTM. The SDINLT* pins should be unconnected. This termination improves the internal RX upstream calibration.
4.2 Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Value, Part No</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupling capacitors</td>
<td>20nF to 100nF X7R with low series inductance</td>
</tr>
<tr>
<td>VCM capacitor</td>
<td>100nF X7R</td>
</tr>
<tr>
<td>Shield capacitor</td>
<td>100nF X7R with low series inductance</td>
</tr>
<tr>
<td>ESD protection</td>
<td>Use single ESD diodes</td>
</tr>
<tr>
<td>APIX connector</td>
<td>Use connector suitable for high frequency signals, e.g. Rosenberger D4S20F-40MA5-Z</td>
</tr>
<tr>
<td>APIX cable</td>
<td>Leoni Dacar 535, Leoni Dacar 535-2 (see also application note regarding Apix Cable Assembly requirements from INOVA: AN_INAP_203.pdf)</td>
</tr>
</tbody>
</table>

Table 3: APIX related components

The coupling capacitors can have values between 20nF and 100nF. The actual value depends on the targeted parameter that needs to be optimized. For blocking DC swing from line coding a bigger value is better, for the lowest pattern frequency attenuation, lower values are suitable.

4.3 Signal Breakout

For the optimal routing of high speed signals the following scheme is recommended. The order of the APIX transmission pins is optimized for the Rosenberger HSD connector. Device and connector are both on the same layer.

Figure 6 shows the connector pinning and wiring of the Rosenberger connector as it is used on Fujitsu application boards. Fujitsu recommends to use the same pin numbering.
4.4 Layout Rules

General layout rules for differential high speed signals should be taken into consideration. In addition, it is recommended to design the layout with the following main parameters.

Transmission lines

- Follow the general rules for transmission lines as described in chapter Signal Integrity.
- The transmission lines of the APIX circuitry should be routed as microstrip lines on the top layer (same layer as Indigo2) or as strip lines in an inner layer.
- Avoid vias, which cause impedance discontinuities. If vias are necessary, enlarge the keep out area around the vias in all layers and add ground vias adjacent to the signal vias.
- If option 2 is used (ESD protection at device), place pull down resistors close to transmission lines.
- Separate differential pairs with guard ground. The distance between guard ground and transmission line should be larger than 3 times the distance between traces of a transmission line pair (good practice is 5 times).

Connector shield grounding

- Shield signal pairs in connector from other signals.
- A low impedance connection between the shield and the PCB ground is required. The shield connection impedance must be low in the frequency range at which the shield should operate. Figure 7 shows layout recommendations for a Rosenberger connector with use of 4 capacitors to reduce the inductance. The connection (direct or capacitive coupled) may depend on the specification of the system designer.

- Remove ground planes below Rosenberger HSD connector in order to reduce parasitic capacitors.
Coupling Capacitors

- Place coupling capacitors in APIX signal lines close to Rosenberger HSD Connector or closed to Indigo2 pins.
- Ground plane directly below pads of coupling capacitors should be removed (Figure 8)

![Figure 8: Ground Plane under coupling capacitor pads](image-url)
5 Oscillator

The circuitries shown below are flexible designs, implemented in Fujitsu’s evaluation boards. Designer should note however, that an optimal design with respect to oscillation stability and precision with minimal jitter depends heavily on the target system and that the responsibility for this lies with the respective PCB designer.

The crystal oscillation buffer has a built in feedback resistor. If APIX oscillator mode is switched to clock input (see hardware manual, bootstrap configuration), the feedback resistor is disabled. There is no need for an external feedback resistor.

5.1 Schematics

Use of crystal:

![Figure 9: Oscillator circuitry with external crystal](image)

Use of external clock generator (clock input):

![Figure 10: Oscillator circuitry with external clock generator](image)

5.2 Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal</td>
<td>30MHz, +/-100ppm</td>
<td>low ESR</td>
</tr>
<tr>
<td>C1, C2</td>
<td>approx 10pF</td>
<td>low ESR, designed for high frequency applications (NP0, C0G)</td>
</tr>
<tr>
<td>Rd</td>
<td>Depends on crystal</td>
<td>Damping resistor</td>
</tr>
</tbody>
</table>

Table 4: Oscillator components
The capacitors $C_1$ and $C_2$ form the load capacitance for the crystal. The optimum load capacitance ($C_L$) for a given crystal is specified by the crystal manufacturer. The equation to calculate the values of $C_1$ and $C_2$ is

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_S$$

where $C_S$ is the stray capacitance of the PCB, typically about 5pF.

The function of the damping resistor $R_d$ is to limit the current available at the electrodes of the crystal unit. $R_d$ must be large enough to avoid overdriving the crystal, yet small enough to provide enough current to start oscillation quickly. The smaller the value of $R_d$, the faster the oscillator will start. High drive current causes some crystals to age faster, depending on the manufacturing process. An excessive drive current may increase electromagnetic noise, reduce the frequency tolerance or damage the crystal in worst case (long term reliability issue).

Optimum component values depend on the specifications of the crystal resonator and the peripheral environment (parasitic capacitance of external printed circuit board, etc.).

### 5.3 Layout

Good layout practices are fundamental to the correct operation and reliability of the oscillator.

- Keep traces for crystal circuitry short to minimize noise and to reduce the stray capacitance $C_S$.
- Keep supply wires with high current and high frequency traces far away from the oscillation circuitry to avoid crosstalk and noise coupling.
- The lines of the oscillation circuit should not cross lines of other circuits.
- Avoid the use of vias. Vias should only be used for connections to the ground plane.
- Place ground plane under oscillator circuitry to reduce noise. The better solution is to place an additional ground pattern around the oscillation circuitry as a shield. The shield must have a low impedance connection to the ground plane for high frequency. (Note: Figure 11 does not show the power supply decoupling)

![Figure 11: Oscillator layout example](image-url)
6 System Supply and System Ground Concept

To avoid ground loops one main supply for all APIX boards should be used. The supplies for all APIX RX boards should be derived from the supply on the TX board. APIX ground on Indigo2 board should be connected to APIX cable shield via capacitor (2x100nF) and resistor (1M).

Different points of chassis can have ground offsets. If it’s required to connect Indigo2 board ground to chassis (e.g. physical connection with skews) then a separate ground shape – a frame ground – is needed. The frame ground is directly connected to the chassis. Frame ground and digital ground are connected via resistor and capacitor only as shown in Figure 12.

![Figure 12: Recommended supply and ground concept](image-url)
Fujitsu does not recommend a supply concept as shown in Figure 13. This concept can cause ground offsets and ground loops which cause noise and reduce the reliability of the APIX link.

![Figure 13: Non recommended supply and ground concept](image)

A DC Offset between TX ground and Indigo2 ground should not influence APIX link because signal lines are AC coupled.

But high current pulses on ground could cause ground bounce which lead to temporarily common mode changes of APIX signal. The differential swing of APIX signal could be dropped in case that the level of common mode change exceeds the specified input level of APIX Receiver.

![Figure 14: Dropped APIX swing without recommended supply and ground concept](image)
7 Signal Integrity

General layout rules for differential high speed signals should be taken into consideration. The basic rules are described in this chapter.

7.1 Differential Transmission Lines

- Use strip lines or microstrip lines. Microstrip lines have the advantage of not using vias which can cause impedance mismatch. Strip lines have the advantage that they are insensitive against EMC emission.

![Figure 15: Differential transmission lines](image)

- The differential impedance of the transmission line is \( Z_0 = 100 \) Ohm +/-10%.
- The single-ended impedance of the transmission line is 50 Ohms to GND.
- Maintain equal gaps on the whole trace.
- Place closed ground plane under transmission lines without interruption.
- Avoid use of through vias for connecting lines between an outer layer and an inner layer. These introduce stubs and cause impedance mismatches. If a layer change cannot be avoided, use blind or buried vias.
- Avoid unbalanced circuit elements. These cause differential to common mode coupling.
- Line length of p and n signal lines should be matched.
- Meander lines (individual for p and n) are forbidden because of impedance mismatch.

7.2 Bends

- Avoid right-angle bends or sharp corners in traces (parasitic capacitance), try to use bends of 45° or less. Curves are better than bends. If right angle bends cannot be avoided, round outside corner of the bend or chamfer the corner.

![Figure 16: Corner patterns](image)

- Keep the same space between differential lines
7.3 Skew Control
- Make sure that a differential pair has equal line lengths.
- Eliminate the skew between the clock channel and the data channels (not relevant for APIX).
- If meander lines are used, keep at least 5W of spaces between the meander line patterns.

7.4 Coupling, crosstalk
- Separate neighboring transmission line pairs by minimum 5x intra-pair distance if shields are not used (reduction of crosstalk coupling).
- Keep transmission lines away from other signals.
- Shield transmission lines to avoid cross-talk. Use a symmetrical architecture for the shields.
Figure 20: Shielded lines
8 Additional APIX Information

Please refer to Inova Semiconductors:
http://www.inova-semiconductors.com/