MB86R11 Application Note

DDR3 Interface

PCB Design Guideline

February, 2011
The 1.0 edition
Preface

This guideline describes PCB design restrictions related to MB86R11 DDR3 interface signal wiring.

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<tr>
<td>2011/02/22</td>
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<td>Newly issued</td>
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1. **Floor plan**

Figure 1-1 shows the reference example of the floor plan of MB86R11 and connected DDR3 SDRAM devices.

![Floor plan diagram](image)

**Figure 1-1** Reference example of the floor plan of MB86R11 and DDR3 SDRAM devices
2. PCB laminating

This chapter shows the recommended laminating conditions of the PCB.

<table>
<thead>
<tr>
<th>Resist thickness</th>
<th>Conductor thickness</th>
<th>Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>40μm</td>
<td>L1 43μm</td>
<td>SIG. (copper foil: 18mm, plating: 25mm)</td>
</tr>
<tr>
<td>100μm</td>
<td>L2 35μm</td>
<td>Power</td>
</tr>
<tr>
<td>150μm</td>
<td>L3 35μm</td>
<td>SIG.</td>
</tr>
<tr>
<td>150μm</td>
<td>L4 35μm</td>
<td>GND</td>
</tr>
<tr>
<td>100μm</td>
<td>L5 35μm</td>
<td>Power</td>
</tr>
<tr>
<td>150μm</td>
<td>L6 35μm</td>
<td>SIG.</td>
</tr>
<tr>
<td>150μm</td>
<td>L7 35μm</td>
<td>GND</td>
</tr>
<tr>
<td>150μm</td>
<td>L8 43μm</td>
<td>SIG. (copper foil: 18mm, plating: 25mm)</td>
</tr>
</tbody>
</table>

Insulation material: relative permittivity=4.3 (only the resist part is 3.9)

Figure 2-1 PCB laminating

**Specified condition of wiring layer**
- L1 and L8 are used as wiring and pull-out wiring layer of CLK.
- L3 and L6 are used as wiring layer of DQS, DQ, and CMD/ADD.
- L2 and L5 are used as power layer.
- L4 and L7 are used as GND layer.
3. DDR3_SDRAM specifications

This chapter shows DDR3_SDRAM that can be used for the DDR3 interface with Emerald. If an alternative device fulfills the same requirements, it can also used. Please note however, that if you use an alternative device, there may be differences concerning I/O quality which may require your attention. However, all I/O characteristics should be checked as could differ. Even if you use the device(s) listed below, you must refer to the specifications provided by the DRAM manufacturer for the confirmation of details (e.g. operating temperature conditions etc.).

Table 3-1  Recommended DDR3_SDRAM

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Product name</th>
<th>IBIS model name</th>
<th>Driver strength</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micron Technology, Inc.</td>
<td>MT41J128M16HA-15E</td>
<td>v69a_at.ibs</td>
<td>34Ω</td>
<td>It has already been verified by the transmission line analysis.</td>
</tr>
<tr>
<td></td>
<td>(2Gb 1333Mbps)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4. Signal design restrictions (DDR3 interface part)

This chapter describes the signal wiring design restrictions for the DDR3 interface part.

4.1. Definition of signal line group

In order to make the requirements for wiring configurations described further on in this document easier to understand, the DDR3 interface signals are classified into the groups listed below.

<table>
<thead>
<tr>
<th>Wiring preferential order</th>
<th>Group name</th>
<th>Pin name of MB86R11</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MCK_Group</td>
<td>MCK, MXCK</td>
</tr>
<tr>
<td>2</td>
<td>MDQS0_Group</td>
<td>MDQS0, MXDQS0</td>
</tr>
<tr>
<td></td>
<td>MDQS1_Group</td>
<td>MDQS1, MXDQS1</td>
</tr>
<tr>
<td></td>
<td>MDQS2_Group</td>
<td>MDQS2, MXDQS2</td>
</tr>
<tr>
<td></td>
<td>MDQS3_Group</td>
<td>MDQS3, MXDQS3</td>
</tr>
<tr>
<td>3</td>
<td>MDQ0_Group</td>
<td>MDQ0 ~ MDQ7, MDM0</td>
</tr>
<tr>
<td></td>
<td>MDQ1_Group</td>
<td>MDQ8 ~ MDQ15, MDM1</td>
</tr>
<tr>
<td></td>
<td>MDQ2_Group</td>
<td>MDQ16 ~ MDQ23, MDM2</td>
</tr>
<tr>
<td></td>
<td>MDQ3_Group</td>
<td>MDQ24 ~ MDQ31, MDM3</td>
</tr>
<tr>
<td>4</td>
<td>MCNTL_Group</td>
<td>MCKE, MXCS, MODT</td>
</tr>
<tr>
<td>5</td>
<td>MCMD_Group</td>
<td>MA0 ~ MA14, MBA0 ~ MBA2, MXCAS, MXRAS, MXWE</td>
</tr>
</tbody>
</table>
4.2. General wiring restrictions

This section describes the general wiring restrictions.

- It is recommended that signal wiring be designed to have the following characteristic impedance.
  - Single impedance: $50\Omega \pm 10\%$
  - Differential impedance: $100\Omega \pm 10\%$

- Signal wiring on power layer and GND layer should be sufficient width to guarantee the flow of return current. (Signal line should be wired on the same power group or GND group. It must not cross over other power and GND groups.)

- Please use parallel wiring for the positive and negative signals of the differential MCK_Group and MDQSx_Group signals. In addition, also take care that the position and number of layer vias is the same.

- The following groups must wire the same layer respectively, and the number of layer transfer vias must become the same, too.
  - MDQS0_Group and MDQ0_Group
  - MDQS1_Group and MDQ1_Group
  - MDQS2_Group and MDQ2_Group
  - MDQS3_Group and MDQ3_Group

- There are no restrictions to the number of layer transfer vias for other signals, but use a minimum possible.

- When using meander wiring layouts for signal delay, crosstalk may occur and the delay value reduced, therefore having wider spacing between wirings is recommended. The recommended wire spacing is about five times the wiring width.

![Wire spacing](image)

Bevelled corners used in order to reduce signal reflections

Figure 4-1 Meander wiring

The recommended conditions and the simulation waveform which are described further on in this document are valid under the above conditions.

If your design greatly differs from the above conditions, then please run a simulation on your wiring.

4.3. Resistance

- Resistors described in this guideline should be generally selected from the E12 series.
  - E12 series: 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82

- The following resistance tolerance values should be used (according to the resistance type):
  - Terminal resistance: under $\pm 5\%$
  - Divider resistance for VREF: under $\pm 1\%$
4.4. **Terminal resistance/damping resistance/wire length**

Table 4-2 shows the recommended resistance value and wire length for each group. The wiring topology diagram relevant to this section is shown in "4.7. Wiring topology".

<table>
<thead>
<tr>
<th>No.</th>
<th>Group name</th>
<th>External terminal resistance value (Rt)</th>
<th>Damping resistance value (Rd)</th>
<th>Wire length from MB86R11 output to SDRAM input</th>
<th>Internal group approved wire length variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MCK_Group</td>
<td>39Ω × 2 0.1µF capacitor × 1 (Refer to &quot;4.7.1.&quot;)</td>
<td>N/A</td>
<td>Refer to &quot;4.7.1.&quot;</td>
<td>Meet the conditions of &quot;4.7.1.&quot;</td>
</tr>
<tr>
<td>2</td>
<td>MDQSx_Group</td>
<td>N/A</td>
<td>N/A</td>
<td>Refer to &quot;4.7.2.&quot;</td>
<td>Meet the conditions of &quot;4.7.2.&quot;</td>
</tr>
<tr>
<td>3</td>
<td>MDQx_Group</td>
<td>N/A</td>
<td>N/A</td>
<td>Refer to &quot;4.7.3.&quot;</td>
<td>Meet the conditions of &quot;4.7.3.&quot;</td>
</tr>
<tr>
<td>4</td>
<td>MCNTL_Group</td>
<td>39Ω</td>
<td>N/A</td>
<td>Refer to &quot;4.7.4.&quot;</td>
<td>Meet the conditions of &quot;4.7.4.&quot;</td>
</tr>
<tr>
<td>5</td>
<td>MCMD_Group</td>
<td>39Ω</td>
<td>N/A</td>
<td>Refer to &quot;4.7.4.&quot;</td>
<td>Meet the conditions of &quot;4.7.4.&quot;</td>
</tr>
</tbody>
</table>
4.5. Wiring gap/crosstalk

Please keep to the wiring configurations shown below in order to avoid malfunctions and deteriorated signal integrity due to crosstalk.

(1) The recommended gap for wiring within MDQx_Group and MCMD_Group groups should be over 300µm.

Example: MDQ0 — MDQ1
           Over 300µm

Example: MA0 — MA1
          Over 300µm

Figure 4-2  Gap for wiring within MDQx_Group and MCMD_Group

(2) The gap for wiring with other groups should be over 300µm.

Example: MDQ0 — MA0
          Over 300µm

Example: MDQ0 — MDQ8
          Over 300µm

Figure 4-3  Gap for wiring of other signal groups

(3) Differential wiring signals of MCK_Group and MDQSx_Group should use a wiring gap of over 500µm to other signals.

If it is difficult to guarantee a gap above 500µm, separate the wire from other signals using a GND area. However, please take the consequent decrease of the wiring impedance into consideration.

Example: MCK — Other signals
          Over 500µm

Example: MDQS — Other signals
          Over 500µm

Figure 4-4  Gap for wiring between signal in MCK_Group/MDQSx_Group and other signals
4.6. **ZQ/ODT setting**

Table 4-3 shows the ZQ setting conditions.

<table>
<thead>
<tr>
<th>Group name</th>
<th>Driver strength of MB86R11 (RON)</th>
<th>ZQ setting of MB86R11</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCK_Group</td>
<td>40Ω</td>
<td></td>
</tr>
<tr>
<td>MDQSx_Group</td>
<td>48Ω</td>
<td></td>
</tr>
<tr>
<td>MDQx_Group</td>
<td>48Ω</td>
<td></td>
</tr>
<tr>
<td>MCNTL_Group</td>
<td>60Ω</td>
<td>ZQ calibration</td>
</tr>
<tr>
<td>MCMD_Group</td>
<td>60Ω</td>
<td></td>
</tr>
</tbody>
</table>

Table 4-4 shows the recommended ODT setting conditions for MDQSx_Group and MDQx_Group signals.

<table>
<thead>
<tr>
<th>Operating condition</th>
<th>MB86R11</th>
<th>DDR3_SDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write to DDR3_SDRAM</td>
<td>Off</td>
<td>60Ω</td>
</tr>
<tr>
<td>Read from DDR3_SDRAM</td>
<td>40Ω</td>
<td>Off</td>
</tr>
</tbody>
</table>
4.7.  Wiring topology

This section illustrates the recommended wiring topology of each group.

4.7.1.  Wiring topology diagram of MCK_Group

- In wiring, the L1/L8 layer is assumption.
- Wire length doesn't contain the length of the via.

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Length of wiring &quot;L1 + L2&quot; [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCK</td>
<td>40.7±1 (Differential and equal-length)</td>
</tr>
<tr>
<td>MXCK</td>
<td>40.9±1 (Differential and equal-length)</td>
</tr>
</tbody>
</table>

Figure 4-5  Wiring topology diagram of MCK_Group
4.7.2. Wiring topology diagram of MDQSx_Group

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Length of wiring &quot;L1&quot; [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDQS0/MXDQS0</td>
<td>29.1±3 (Differential and equal-length)</td>
</tr>
<tr>
<td>MDQS1/MXDQS1</td>
<td>29.7±3 (Differential and equal-length)</td>
</tr>
<tr>
<td>MDQS2/MXDQS2</td>
<td>28.9±3 (Differential and equal-length)</td>
</tr>
<tr>
<td>MDQS3/MXDQS3</td>
<td>28.6±3 (Differential and equal-length)</td>
</tr>
</tbody>
</table>

- In wiring, the L3/L6 layer is assumption.
- Wire length doesn't contain the length of the via.

Figure 4-6  Wiring topology diagram of MDQSx_Group
4.7.3. Wiring topology diagram of MDQx_Group

### Signal name | Length of wiring "L1" [mm] | Signal name | Length of wiring "L1" [mm]
--- | --- | --- | ---
MDM0 | Wire length of MDQS0_Group (Average value): +3.8±2 | MDM2 | Wire length of MDQS2_Group (Average value): +5.3±2
MDQ0 | Wire length of MDQS0_Group (Average value): +5.0±2 | MDQ16 | Wire length of MDQS2_Group (Average value): +3.5±2
MDQ1 | Wire length of MDQS0_Group (Average value): +3.8±2 | MDQ17 | Wire length of MDQS2_Group (Average value): +1.6±2
MDQ2 | Wire length of MDQS0_Group (Average value): +3.5±2 | MDQ18 | Wire length of MDQS2_Group (Average value): +5.0±2
MDQ3 | Wire length of MDQS0_Group (Average value): +2.6±2 | MDQ19 | Wire length of MDQS2_Group (Average value): +3.6±2
MDQ4 | Wire length of MDQS0_Group (Average value): +2.4±2 | MDQ20 | Wire length of MDQS2_Group (Average value): +4.9±2
MDQ5 | Wire length of MDQS0_Group (Average value): +5.4±2 | MDQ21 | Wire length of MDQS2_Group (Average value): +5.3±2
MDQ6 | Wire length of MDQS0_Group (Average value): +4.0±2 | MDQ22 | Wire length of MDQS2_Group (Average value): +4.0±2
MDQ7 | Wire length of MDQS0_Group (Average value): +2.1±2 | MDQ23 | Wire length of MDQS2_Group (Average value): +2.9±2
MDQ8 | Wire length of MDQS1_Group (Average value): +3.8±2 | MDQ24 | Wire length of MDQS3_Group (Average value): +1.3±2
MDQ9 | Wire length of MDQS1_Group (Average value): +3.6±2 | MDQ25 | Wire length of MDQS3_Group (Average value): +0.4±2
MDQ10 | Wire length of MDQS1_Group (Average value): +3.0±2 | MDQ26 | Wire length of MDQS3_Group (Average value): +3.5±2
MDQ11 | Wire length of MDQS1_Group (Average value): +3.8±2 | MDQ27 | Wire length of MDQS3_Group (Average value): +3.1±2
MDQ12 | Wire length of MDQS1_Group (Average value): +3.4±2 | MDQ28 | Wire length of MDQS3_Group (Average value): +5.4±2
MDQ13 | Wire length of MDQS1_Group (Average value): +4.4±2 | MDQ29 | Wire length of MDQS3_Group (Average value): +1.8±2
MDQ14 | Wire length of MDQS1_Group (Average value): +5.7±2 | MDQ30 | Wire length of MDQS3_Group (Average value): +3.8±2
MDQ15 | Wire length of MDQS1_Group (Average value): +2.7±2 | MDQ31 | Wire length of MDQS3_Group (Average value): +5.3±2

Note 1) The DQ signal can be shuffled in byte (Do not include DM).

Figure 4-7  Wiring topology diagram of MDQx_Group
4.7.4. Wiring topology diagram of MCNTL_Group/MCMD_Group

- In wiring, the L3/L6 layer is assumption.
- Wire length doesn't contain the length of the via.

Wire length from MB86R11 to SDRAM at the farthest position (48.7mm~62.7mm)

Figure 4-8  Wiring topology diagram of MCNTL_Group/MCMD_Group
5. Power system design restrictions

This chapter describes the power system design restrictions for the DDR3 interface part of MB86R11.

5.1. Number and capacity of bypass capacitor

Table 5-1 shows the number of bypass capacitors for the high frequency noise removal for which mounting is necessary directly under MB86R11.

<table>
<thead>
<tr>
<th>Pin name of Emerald</th>
<th>Power supply voltage</th>
<th>Number of necessary bypass capacitor</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDRVDE</td>
<td>1.5V</td>
<td>18</td>
<td>For DDR3 interface</td>
</tr>
<tr>
<td>VSS</td>
<td>0V</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

- If capacity is a value close to 0.1µF (0.22µF etc. for instance), the bypass capacitor can be used.
- Place the 0.1µF capacitor as close as possible to the power/GND pins of Emerald (refer to "5.2. Pull-out wiring condition").
- For the 0.1µF capacitor, we recommend the use of ceramic capacitors of under size 1005 (1.0mm x 0.5mm).
  In addition, use low ESL (Equivalent Series Inductance) value components where possible in order to decrease noise.
- Mount a high-capacity capacitor for the low frequency if needed. One 100µF is recommended to be used for the current variation of 1A only as a guide.
- Verify your board design by simulations and measurements if you can not mount capacitors of the above number.
5.2. Pull-out wiring condition

This section shows the example of mounting the bypass capacitor for the high frequency noise removal. Be sure to meet the following pull-out wiring conditions to reduce the inductance value by wiring and to reduce the noise. If it doesn't meet these conditions, widen the wire width as much as possible, and shorten the wire length.

Note 1) There is no problem even if the Chip on Via method without the pull-out wiring is used.

Figure 5-1  Example of mounting a bypass capacitor