Display Timing Calculation

(MB86R01 'Jade')
Display Timing Formulae

\[ f_{dot\_clk} = \text{pixel clock} \]
\[ f_v = \text{vertical frequency} \]
\[ f_{ref} = \text{reference clock (PLL)} \]
\[ SC = \text{Scaler} \]
\[ f_h = \text{horizontal frequency} \]

\[ f_{dot\_clk} = f_v \times VTR \times HTP \]
\[ f_{dot\_clk} = \frac{f_{ref}}{SC} \]
\[ f_v = \frac{f_{dot\_clk}}{VTR \times HTP} \]
\[ f_h = V_t \times VDP \]

Note:

\[ JADE : f_{ref} = 666 \text{Mhz} \]

\[ JADE : f_{dot\_clock} < 67 \text{Mhz} \]

\[ SC = \frac{f_{ref}}{f_v \times VTR \times HTP} = \frac{f_{ref}}{f_{dot\_clk}} \]
Clock Generation in Jade

\[ f_{\text{CCLK}} = \frac{f_{\text{CLK}} \cdot N}{2} \]

\[ f_{\text{PLL}} = f_{\text{CLK}} \cdot N \]
Display Timing Parameters

<table>
<thead>
<tr>
<th>HTP</th>
<th>VTR</th>
<th>HSP</th>
<th>VSP</th>
<th>HSW</th>
<th>VSW</th>
<th>HDP</th>
<th>VDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Horizontal Total Pixels</td>
<td>Vertical Total Raster</td>
<td>Horizontal Synchronize pulse Position</td>
<td>Vertical Synchronize pulse Position</td>
<td>Horizontal Synchronize pulse Width</td>
<td>Vertical Synchronize pulse Width</td>
<td>Horizontal Display Period</td>
<td>Vertical Display Period</td>
</tr>
</tbody>
</table>
1. Select the display parameters from the display panel specification

\[
0 < \text{HDB} \leq \text{HDP} < \text{HSP} < \text{HSP} + \text{HSW} + 1 < \text{HTP}
\]

\[
0 < \text{VDP} < \text{VSP} < \text{VSP} + \text{VSW} + 1 < \text{VTR}
\]

2. Calculate the pixel frequency

\[
f_{\text{dot \_ clk}} = f_v \times VTR \times HTP
\]

3. Calculate the scaler value

\[
SC = \frac{f_{\text{ref}}}{f_v \times VTR \times HTP} = \frac{f_{\text{ref}}}{f_{\text{dot \_ clk}}}
\]

Select integer value:
- Round down
- Round up

Calculate the resulting pixel vertical frequency with the selected scaler value:

\[
f_{\text{dot \_ clk}} = \frac{f_{\text{ref}}}{SC}
\]

\[
f_v = \frac{f_{\text{ref}}}{SC \times VTR \times HTP}
\]

\[f_{\text{dot \_ clock}} < 67 \text{ Mhz}\]

Check that the calculated values fulfill the display specifications.
Optional: adapt the blanking area to reach a more precise result.

Note:
Skew occurs between the syncs and the RGB/DE signals (the RGB and DE signals are delayed):
- Coral family – 13 pixel clock cycles
- Carmine – 15 pixel clock cycles
- The timing at the GDC pads is different to the register settings
- Panels requiring less H-sync back porch are not supported – the H-sync has to be delayed by external logic
4. Set scaler register value
The scaler value depends on the selected offset

Divides display reference clock by the preset ratio to generate dot clock

Offset = 0
- Frequency not divided
- Frequency not divided

Offset = 100n

x00000 Frequency division rate = 1/4
- Frequency division rate = 1/4

x00001 Frequency division rate = 1/6
- Frequency division rate = 1/6

x00010 Frequency division rate = 1/8
- Frequency division rate = 1/8

x00011 Frequency division rate = 1/8
- Frequency division rate = 1/8

x11111 Frequency division rate = 1/64
- Frequency division rate = 1/64

When n is set, with Offset = 0, the frequency division rate is 1/(2n + 1).
When m is set, with Offset = 100n, the frequency division rate is 1/(m + 1).

NOTE: These are setting parameters with the same function (2n + 2 = m + 1).
Because of this, m = 2n + 1 is established. When n is set to the D0 field with Offset = 0, 2n + 1 is reflected with Offset = 100n.
Also, when PLL is selected as the reference clock, frequency division ratios 1/1 to 1/5 are non-functional even if set (!) other frequency division ratios are assigned.

NOTE:
Also, when the PLL is selected as the reference clock, frequency division ratios 1/1 to 1/5 are non-functional even if set (!) other frequency division ratios are assigned.

Therefore – valid setting range: 1/6 ... 1/64
Display Timing Example - 1

Display Panel:
Toshiba Matsushita Display Technology, LTA065B0D0F (6")
Vertical frequency: 60 Hz

Excerpt from the display specification:

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>min.</th>
<th>typ.</th>
<th>Max.</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Period</td>
<td>tv</td>
<td>500</td>
<td>525</td>
<td>550</td>
<td>th</td>
</tr>
<tr>
<td></td>
<td></td>
<td>---</td>
<td>16.67</td>
<td>17.85</td>
<td>ms</td>
</tr>
<tr>
<td>Vertical blanking Term</td>
<td>tvblk</td>
<td>20</td>
<td>45</td>
<td>70</td>
<td>th</td>
</tr>
<tr>
<td>V-sync Pulse Width</td>
<td>tvw</td>
<td>2</td>
<td>---</td>
<td>---</td>
<td>th</td>
</tr>
<tr>
<td>Vertical Front Porch</td>
<td>tvfp</td>
<td>2</td>
<td>---</td>
<td>---</td>
<td>th</td>
</tr>
<tr>
<td>Vertical Data Sync Period</td>
<td>tvds</td>
<td>6</td>
<td>---</td>
<td>---</td>
<td>th</td>
</tr>
<tr>
<td>Vertical Display Term</td>
<td>tvde</td>
<td>480</td>
<td>480</td>
<td>480</td>
<td>th</td>
</tr>
<tr>
<td>Horizontal Period</td>
<td>th</td>
<td>740</td>
<td>800</td>
<td>860</td>
<td>tc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>31.5</td>
<td>31.75</td>
<td>---</td>
<td>us</td>
</tr>
<tr>
<td>H-sync Pulse Width</td>
<td>thw</td>
<td>8</td>
<td>160</td>
<td>---</td>
<td>tc</td>
</tr>
<tr>
<td>Horizontal Front Porch</td>
<td>thfp</td>
<td>8</td>
<td>---</td>
<td>---</td>
<td>tc</td>
</tr>
<tr>
<td>Horizontal Data Sync Period</td>
<td>thds</td>
<td>8</td>
<td>---</td>
<td>---</td>
<td>tc</td>
</tr>
<tr>
<td>Horizontal Display Term</td>
<td>thde</td>
<td>640</td>
<td>640</td>
<td>640</td>
<td>tc</td>
</tr>
<tr>
<td>Clock Period</td>
<td>tc</td>
<td>35.0</td>
<td>39.7</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>Clock “L” Time</td>
<td>tcl</td>
<td>10.0</td>
<td>---</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>Clock “H” Time</td>
<td>tch</td>
<td>10.0</td>
<td>---</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>tds</td>
<td>5.0</td>
<td>---</td>
<td>---</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>tdh</td>
<td>10.0</td>
<td>---</td>
<td>---</td>
<td>ns</td>
</tr>
</tbody>
</table>
Display Timing Example - 2

V-sync

H-sync

RGB Data

DE

H-sync

NCLK

RGB Data

DE
1. Select the display parameter

\[ f_{\text{dot clk max}} = \frac{V_{\text{max}} \times H_{\text{max}} \times T_{\text{vdp}}}{T_{\text{clock}}} = \frac{35 \text{ns} \times 35 \text{ns} \times 480}{28.75 \text{MHz}} = 28.75 \text{MHz} \]

\[ f_{\text{v min}} = \frac{1}{T_{\text{vmax}}} = \frac{1}{17.85 \text{ms}} = 56 \text{Hz} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTP</td>
<td>800</td>
</tr>
<tr>
<td>VTR</td>
<td>525</td>
</tr>
<tr>
<td>HSP</td>
<td>648</td>
</tr>
<tr>
<td>VSP</td>
<td>482</td>
</tr>
<tr>
<td>HSW</td>
<td>160</td>
</tr>
<tr>
<td>VSW</td>
<td>2</td>
</tr>
<tr>
<td>HDP</td>
<td>640</td>
</tr>
<tr>
<td>VDP</td>
<td>480</td>
</tr>
</tbody>
</table>
Display Timing Example - 4

2. Calculate the pixel frequency

\[ f_{\text{dot}} = f_v \times VTR \times HTP = 60Hz \times 525 \times 800 = 25.2\text{MHz} \]

3. Calculate the scaler

\[ SC = \frac{f_{\text{ref}}}{f_v \times VTR \times HTP} = \frac{666\text{MHz}}{25.2\text{MHz}} = 26.4 \]

Round down: \( SC = 26 \)

\[ f_{\text{dot}} = \frac{f_{\text{ref}}}{SC} = \frac{666\text{MHz}}{26} = 26.62\text{MHz} \Rightarrow \text{OK} \]

\[ f_v = \frac{f_{\text{ref}}}{SC \times VTR \times HTP} = \frac{666\text{MHz}}{26 \times 525 \times 800} = 60.99\text{Hz} \Rightarrow \text{OK} \]
Round up: SC = 27

\[ f_{\text{dot clk}} = \frac{f_{\text{ref}}}{SC} = \frac{666\text{MHz}}{27} = 24.67\text{MHz} \Rightarrow \text{OK} \]

\[ f_v = \frac{f_{\text{ref}}}{SC \times VTR \times HTP} = \frac{666\text{MHz}}{27 \times 525 \times 800} = 58.73\text{Hz} \Rightarrow \text{OK} \]

Try to reach a precise result by modifying the blanking area:

<table>
<thead>
<tr>
<th>HTP</th>
<th>860</th>
<th>VTR</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSP</td>
<td>648</td>
<td>VSP</td>
<td>482</td>
</tr>
<tr>
<td>HSW</td>
<td>160</td>
<td>VSW</td>
<td>2</td>
</tr>
<tr>
<td>HDP</td>
<td>640</td>
<td>VDP</td>
<td>480</td>
</tr>
</tbody>
</table>

4. Set scaler register value

Offset 0x100 -> m = SC-1 = 25 = 0x19
Write register DCM1: 0x1900