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## Revision History

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1. DDR2 controller

1.1. Self refresh setting sample at STOP mode

In MB86R01, DDR2DRAM contents are able to be retained by self refresh command to DDR2SDRAM during STOP mode. Example of self refresh setting is shown below.

As a precondition, access to SDRAM must be stopped (stop of GDC operations)

1. ODTCONT off (ODT of SDRAM)
   Write "0000" to DROS register (Offset + 0x60)

2. Resetting auto refresh interval
   Write '0041' to DRCR register (Offset + 0x0E)
   Write '0141' to DRCR register (Offset + 0x0E)
   Wait is in the range of 166MHz[ns] x 30cycles = 180[ns] to refresh interval (setting value of bit7-0 of DRCR)

3. Issue self refresh entry CMD to SDRAM
   Write '0008' to DRIC1 register (Offset + 0x02)
   Write '0000' to DRIC2 register (Offset + 0x04)
   Write '8001' to DRIC register (Offset + 0x00)

4. IRESET/IUSRRST and IDLLRST on
   Write '00000000' to CDCRC register (Offset + 0xEC) of the CCNT module

5. PLL Bypass mode on
   Write "CX" to CRPR register (Offset + 0x00) of the CRG module
   Do not change PLLMO[3:0] field of CRPR register

6. STOP enable on
   Write "80" to CRSR register (Offset + 0x0C) of the CRG module

7. External interrupt High Level setting
   Write "00000055" to EILVL register (Offset + 0x08) of the EXIRC module

8. External interrupt enable on (case of INT_A[0] ON)
   Write "00000001" to EIENB register (Offset +0x00) of the EXIRC module

9. STOP mode on (Wait for External interrupt)
   MCR p15, 0, R1, c7, c0, 4

As a precondition, IRC module's external interrupt must be set as acceptable

External interrupt High Level?

Y

A

Continue to the next sheet

N
(10) Eliminate external interrupt factor at Interrupt Handler

(11) PLL Bypass mode on
   Write "4X" to CRPR register
   (Offset + 0x00) of the CRG module
   Do not change PLLMODE[3:0] field of CRPR register

(12) PLL Lock up Time Wait

(13) IRESET/IUSRRST release.
   Write "00000002" to CDCRC register
   (Offset + 0xEC) of the CCNT module

(14) 166MHz[ns]) x 20cycles = 120[ns] or more Wait

(15) IDLLRST release
   Write "00000003" to CDCRC register
   (Offset + 0xEC) of the CCNT module

(16) DLL LOCK up time (79[µs]) or more Wait

(17) MCKE on (issue Self Refresh Exit CMD to SDRAM)
   Write "003F" to DRIC1 register (Offset + 0x02)
   Write "0000" to DRIC2 register (Offset + 0x04)
   Write "C000" to DRIC register (Offset + 0x00)

(18) Issue NOP CMD x 3 times to SDRAM
   Write "C001" to DRIC register (Offset + 0x00)
   Write "C001" to DRIC register (Offset + 0x00)
   Write "C001" to DRIC register (Offset + 0x00)

(19) Shift to ODTCONT on (SDRAM side) and DDR2C
     normal operation mode
   Write "0001" to DROS register (Offset + 0x60)
   Write "4000" to DRIC register (Offset + 0x00)

(20) 166MHz ([ns]) x 200 cycles = 1200[ns] or more Wait

Release access stop to SDRAM
(GDC is operable)