FUJITSU ASIC Technology

Fujitsu is the only ASIC supplier in the world that can provide customers with leading-edge 90nm node CMOS process technology with Cu interconnects and low-k dielectrics, from 90nm downwards. Fujitsu offers a full turn-key service including design support, testing, bumping, packaging and product engineering.

Mask design rules for technology assessment are already available. Fujitsu will start accepting GDS data for LSIs using 65nm node CMOS technology.

Why Fujitsu?
- The most advanced process technology supplier
- High performance transistors
- Established Cu / Low-k interconnect technology
- Proven reliability
- From front-end design to back-end manufacturing
- Design services and consultations by experts
- Coherent advanced packaging technology

Technology
- LCOS-quality mirror metal
- Smooth, flat and highly reflective
- Narrow gap filling technology
- High-voltage transistor lineups
- New low-k material for 65nm technology
- A highly reliable nano-clustering silica with low dielectric constant (k<2.3) and high elastic modulus (E=10 GPa) for copper damascene process
Fujitsu is investing US$1 billion in its 300mm, 65/90nm Fab. 2 alongside its Fab. 1 in the Mie prefecture, Japan.

### Power dissipation comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>130nm</th>
<th>90nm</th>
<th>65nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series</td>
<td>CS91</td>
<td>CS101</td>
<td>CS201</td>
</tr>
<tr>
<td>Total power (mW)</td>
<td>1000</td>
<td>590</td>
<td>360</td>
</tr>
<tr>
<td>Chip size (mm)</td>
<td>10.0 x 10.0</td>
<td>7.0 x 7.0</td>
<td>5.3 x 5.3</td>
</tr>
<tr>
<td>Ratio</td>
<td>1.00</td>
<td>0.49</td>
<td>0.8</td>
</tr>
<tr>
<td>Max frequency (MHz)</td>
<td>→</td>
<td>120</td>
<td>←</td>
</tr>
<tr>
<td>Logic gate (gate)</td>
<td>→</td>
<td>~3.5M</td>
<td>←</td>
</tr>
<tr>
<td>Memory (bit)</td>
<td>→</td>
<td>7.5M</td>
<td>←</td>
</tr>
</tbody>
</table>

*1 Process = typ, Tj = 25°C, V = 1.20V simulated for core only.

*2 1 gate = 1 dual input nand