Improving electromagnetic compatibility using spread spectrum clock generators

Spread spectrum clocks distribute the energy emitted over a wide frequency band, thus reducing individual peaks in the spectrum and helping meet EMC directives without great expense or re-design, writes Dirk Fischer.

To market an electronic device in Europe, it must comply with the corresponding directives on electromagnetic compatibility. The device must be designed to be sufficiently resistant to interference so that it can function reliably even when it is near other electrical or electronic equipment. Nor must it cause any electromagnetic interference which might disturb the operation of nearby devices such as radio receivers. The technical limits and requirements are laid down in various national and EU standards which apply according to the product – for example, EN55013 for electronic consumer products or EN55014 for household appliances.

An important criterion for meeting these requirements is for the energy emitted to be as low as possible. Circuit-board conductors, sockets or components may act as antennae and emit interfering radiation.

But what can be done to reduce radiation interference or prevent it altogether?

**Causes of interference**

Let us first examine the cause of the interference. The starting point is always a signal that changes over time, i.e., a voltage or a current. The change may be repeated periodically or be a one-off transient process. In both cases, electrical or magnetic fields are generated and these are observed as interference.

Examples of periodic signals are clocks from components such as micro controllers, FPGAs or Asics, modulating signals in communication modules or control signals for motor controllers. Transient changes typically occur during switching operations. Interference is therefore initiated by signals that are needed to operate the module and which cannot normally be completely switched off or removed.

To understand the measures described below, it is useful to clarify the relationship between the time characteristic and the frequency range of a signal. Fast signal changes, i.e., steep signal edges, in both periodic and transient signal forms, contain proportions of many different, sometimes very high, frequencies.

For example, if we consider the clock signal from a synchronous logic circuit, in an idealised form as a square-wave signal, with Fourier analysis, this can be broken down into a series of sinusoidal oscillations and thus transferred to the frequency range. The frequency spectrum of a clock signal therefore consists of many discrete peaks: the fundamental wave with the highest amplitude and numerous harmonic waves, the amplitude of which reduces as the frequency increases.

The frequency spectrum of one-off switching processes can be considered in a similar way (see formula above).

With this knowledge, it becomes clear that the interfering signals emitted can be very effectively reduced by limiting the edge steepness of the clock and control signals, i.e. the strength of the signal driver circuits. The harmonic components then disappear and less energy is emitted. Low-pass filters, RC elements and chokes are also used to absorb higher frequencies as well.

To further reduce the emissions, the device can be screened with sheet metal plates or other conductive surfaces, including foils. A separate ground plane on the circuit board is also an effective way of improving EMC because it screens electrical fields and reduces the energy from magnetic fields by inducing eddy currents.

With spread spectrum clock generators it is easy to significantly reduce the level of interference caused by synchronous clocks.
Development work on EMC and the effective use of the measures described require a lot of experience and it is not always possible to meet the requirements with the first revision of a device. In the worst case scenario, several repeats are needed until the EMC standard is complied with and the product can be released for sale.

As described above, the clock signals from logic circuits are a potential source of interference. The synchronous switching of thousands of transistors causes load changes resulting in periodic, high currents.

With spread spectrum clock generators it is easy to achieve a significant reduction in the level of interference caused by synchronous clocks. In this process, the period of the clock signal is deliberately given a slight jitter and the clock frequency is modulated. Switching circuits are then no longer operated with a discrete frequency but with a very large number of very close frequencies that are constantly changing.

In the frequency spectrum, this process can be observed by the fact that the individual peaks disappear and are replaced by flatter, wider stubs which are then below the limit of the current EMC directives. The energy emitted is distributed over a wider frequency range. The level of the fundamental frequency can therefore be reduced by more than 18dB and the harmonics also benefit from the measure.

System and products
Discrete modules or integrated solutions are used to generate the spread spectrum clocks. With the external configurations, the spread spectrum clock generator (SSCG) module is embedded between quartz crystal and logic IC.

It makes no difference whether the clock is multiplied again in the logic IC by a PLL or whether it is used 1:1. The usual modulation frequency of the SSCG module is around 20kHz. This is slow enough to pass through the PLL without it locking out, ie, the PLL works reliably and the required jitter is still included at the output even in the higher frequency clock.

The modulation depth is typically between ±0.25% and ±1.75% and in most components it can be adjusted with configuration pins or selected as an option when ordering. A 64MHz clock varies by 1%, between 63.36 and 64.64MHz, for example.

On average, the modulated clock is exactly the same as the unmodulated input clock. Common timer applications or UART communication with

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With USB interfaces, the modulation depth should not be more than ±0.25%. A few applications – CAN communication, for example – are not suitable for the modulated clock; however. In these cases, the critical parts of the circuit can be operated with an unmodulated clock and the other part with a modulated clock. Some SSCGs offer suitable reference clock outputs for this purpose.

One approach is to generate the modulation signal digitally. The digital modulation signal is converted by a digital/analog converter with current output. This controls a current-controlled oscillator, which finally generates the output signal.

Further, the modulation signal can be modulated, which eliminates peaks in the modulation frequency that would otherwise be detectable in the frequency spectrum. Compared to the simple modulation signal, this allows a further reduction of around 3dB.

Regarding modulation type, there are two options to choose from. If the target system is to be operated with the maximum frequency, down spread is a suitable option. In this mode, only frequencies in the downward direction are modulated, approximately 64MHz -1.5%. In this case, the clock frequency varies between 63.04 and 64MHz, and the maximum frequency of 64MHz is not exceeded. The centre frequency is then easily below 64MHz.

If the target system has power reserves and could be operated, for example, up to 72MHz, you can choose the centre spread mode. Modulation is then in both directions, 64MHz ±0.75%. The centre frequency is exactly 64MHz, but the maximum frequency that occurs is 64.32MHz.

Clocked digital logic circuits, especially those with fast external buses or strong driver stages, emit electromagnetic waves and are potential sources of interference. This interference has to be kept low in order to satisfy EMC directives and obtain corresponding authorisations for a product.

Conventional methods of improving EMC require planes, additional components, such as chokes, capacitors and screens, as well as additional PCB layers. Moreover, the development costs can be considerable. All of these measures cost time and money.

Spread spectrum clocks can save on components, reduce development time and therefore lower costs.

Figure 3: The improved modulation signal created, the so-called complex modulation cycle