**System Packet Interface Level-4P2**

OIF Compliant SPI-4P2 IO macro and core logic IP for SPI-4PS and NPSI

**Features**

- Point-to-point connection between single PHY and single Link Layer device
- Complies with OIF SPI-4-02.0 System Packet Interface Level 4 (SPI-4) Phase 2 standard
- Supports aggregate bandwidth for OC192, 10Gb/s Ethernet and PoS applications
- Packet Over SONET (POS) PHY Level 4 with FIFOs
- Supports MUX/DEMUX and bridging functions
- 16-bit wide Transmit/Receive Data Path
- Transmit/Receive FIFO Status Interface via LVTTL or LVDS I/O

<table>
<thead>
<tr>
<th></th>
<th>0.11µm</th>
<th>0.18µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data transfer rate per channel</td>
<td>622-1300 Mbps</td>
<td>622-80Mbps</td>
</tr>
<tr>
<td>Aggregate bandwidth rate each direction</td>
<td>10 / 20.8Gbps</td>
<td>10 / 12.5Gbps</td>
</tr>
<tr>
<td>Interface</td>
<td>LVDS</td>
<td>LVDS</td>
</tr>
<tr>
<td>On chip integrated termination resistors</td>
<td>100-ohm</td>
<td>100-ohm</td>
</tr>
<tr>
<td>Mux/Demux</td>
<td>4:1 1:4</td>
<td>4:1 1:4</td>
</tr>
<tr>
<td>Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receive</td>
<td>0.488W</td>
<td>1.04W</td>
</tr>
<tr>
<td>Transmit</td>
<td>0.46W</td>
<td>0.931W</td>
</tr>
<tr>
<td>Process - triple well isolation</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2V and 2.5V</td>
<td>1.8V and 3.3V</td>
</tr>
</tbody>
</table>
# System Packet Interface Level-4

## Benefits
- Industry standard OIF compliance
- Available as core library cell for ASIC designs
- Easy integration of the back-end logic due to internal path being demultiplexed to 64 bits

## Description
The SPI-4 interface core enables the interconnection of physical layer devices to link layer devices in 10Gb/s POS, ATM, and Ethernet applications.

The SPI-4 interface uses LVDS I/O buffers paired with dedicated double data rate (DDR) registers in the data path and LVTTL I/O buffers in the FIFO Status path. The internal data rate is reduced by expanding the 16-bit words in DDR format on the SPI-4 interface to a 64-bit (4 word) single-edge clocked format running at half the SPI-4 interface clock rate.

The macro is fabricated in both Fujitsu’s standard 0.11µm and 0.18µm CMOS technology.

This macro can be used in a variety of applications:
- Line cards in gigabit router and terabit routers
- Optical cross connect switches
- DWDM and SONET/SDH transmission systems

## Deliverables
The Fujitsu value-added SPI-4 Interface Macro enables our customers to design a variety of complex system-on-a-chip ASIC designs for high end networking applications.

A Fujitsu application engineer works with the customer to identify the customer's specific IP requirements. Fujitsu will provide the customer with the following information to support the SPI-4 interface macro:

- Verilog Model
  - Front-end simulation
- Design Compiler Model
  - Timing analysis
  - Place and Route
- Library Exchange Format (LEF)
  - Floorplanning

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