FUJITSU MICROELECTRONICS
DATA SHEET

DS06-20209-5E

Semicustom

CMOS

Standard cell

CS86 Series

■ DESCRIPTION

The CS86 series of 0.18 µm standard cells is a line of CMOS ASICs based on higher integration implemented by introducing wiring pitch reduction technology and on I/O pad placement technology to the conventional CS81 series.

The CS86 series has three types of cell sets (CS86MN, CS86MZ, and CS86ML), covering a variety of applications, from portable devices requiring low power consumption to image processors requiring large-scale circuitry and high speed.The three types of cell sets can be contained on one chip, allowing those system LSIs to be implemented which require low power consumption as well as high-speed operation for certain types of processing.

■ FEATURES

- Technology : 0.18 µm silicon-gate CMOS, 5 to 6 layer wiring
  Standard transistor cells can coexist with either ultra high-speed process cells or low leakage process cells on a chip.
- Supply voltage : 1.8 V ± 0.15 V (standard) to 1.1 V ± 0.1 V
- Junction temperature range : –40 °C to +125 °C
- Cell sets
  - CS86MN : Offers standard transistor characteristics. Designed as a library for products requiring higher throughputs.
  - CS86MZ : Offers transistor characteristics for ultra high-speed operation. Designed as a library for products that require higher processing speeds than those provided by CS86MN.
  - CS86ML : Offers transistor characteristics with less leak current. Designed as a library for mobile devices and other products requiring lower power consumption.
- Cell Specifications :

Cell set name	CS86MZ	CS86MN	CS86ML	Unit
Delay time*1	70	88	136	ps
Power consumption*2	42.7	40.1	38.3	nW/MHz
Leakage power*3	3.922	0.023	0.0067	nW

*1 : 2 input NAND cell (low-power type) , F/O = 2, normal load, Power Supply voltage 1.8 V, Temperature = +25 °C

*2 : 2 input NAND cell (low-power type) , F/O = 1, 4 Grid, Power Supply voltage 1.8 V, Temperature = +25 °C

*3 : 2 input NAND cell (low-power type) , F/O = 0, no load, Power Supply voltage 1.8 V, Temperature = +25 °C

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- Output buffer cells with noise reduction circuits
- Input buffer cells and bidirectional buffer cells with on-chip input pull-up/pull-down resistors
- Buffer cells for crystal oscillation circuits
- Special interfaces : SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others.
- IP macros : CPU (ARM9, FR-V, and others) , DSP, PCI, IEEE1394, USB, IrDA, PLL, DAC, ADC, and others.
- Capable of incorporating compiled cells (RAM/ROM/Register file/Delay line)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using Physical Synthesis tool
- Low power consumption using Low Power Synthesis tool
- Short-term development using a timing driven layout tool
- Hierarchical design environment for supporting large-scale circuits
- Support for Signal-Integrity
- Support for Memory (RAM, ROM) SCAN
- Support for Memory (RAM) BIST
- Support for Boundary SCAN
- Support for path delay test
- Package lineup : QFP, LQFP, HQFP, FBGA

■ MACRO LIBRARY

1. Logic cells

- Adder
- AND-OR Inverter
- Clock Buffer
- Latch
- NAND
- AND
- NOR
- OR-AND
- Scan Flip Flop
- ENOR
- Boundary Scan Register
- Bus Driver
- AND-OR
- Decoder
- NON-Scan Flip Flop
- Inverter
- Buffer
- OR-AND Inverter
- OR
- Delay Buffer
- Selector
- EOR
- Dummy Clock Buffer
- Others

2. IP macro

CPU	FR-V, ARM9, and others.
DSP	Communications DSP, DSP for Digital AV, and others.
Peripheral macro	Interval timer, interrupt controller, DMA controller, RTC, calender, UART, and others.
Interface macro	PCI, IEEE1394, USB, IrDA, and others.
Multimedia processing macros	JPEG, MPEG 4.0, and others.
Mixed signal macros	ADC, DAC, OPAMP, and others.
Compiled macros	RAM (1 port, 2 ports) , ROM, Delay Line, Register file, and others.
PLL	Analog PLL
I/O macro	Compatible with various interface levels between 1.1 V and 5 V; SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others.

Note : ARM is the trademark of ARM Limited in the EU and other countries.

■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated by specifying configuration parameters such as the number of bits and words. The CS86 series has the following types of compiled cells (Note that the word and bit ranges of each macro varies) .

1. Clock synchronous single-port RAM (1 address : 1 RW)

• High density type/High density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

• Super high density type/Super high density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	64 to 144 K	32 to 2 K	2 to 72	bit

• Large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	24 to 1152 K	4K to 16 K	6 to 72	bit

• Super high density large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	2 to 1152 K	512 to 16 K	4 to 72	bit

• High speed type

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 144 K	64 to 2 K	4 to 72	bit

2. Clock synchronous dual-port RAM (2 addresses : 1 RW, 1 R)

• High density type/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

3. Clock synchronous register file (3 addresses : 1 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

4. Clock synchronous register file (4 addresses : 2 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

5. Clock synchronous ROM (1 address : 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 1024 K	128 to 8 K	2 to 128	bit
64	1 to 1024 K	512 to 32 K	2 to 32	bit

6. Clock synchronous delay line memory (2 addresses : 1 W, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 32 K	32 to 1 K	8 to 32	bit
16	384 to 32 K	64 to 2 K	6 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage*1	V_{DD}	−0.5	+ 2.5 *2	V
			+ 4.0 *3	
Input voltage*1	V_I	−0.5	V_{DD} + 0.5 (≤ 2.5 V) *2	V
			V_{DD} + 0.5 (≤ 4.0 V) *3	
Output voltage*1	V_O	−0.5	V_{DD} + 0.5 (≤ 2.5 V) *2	V
			V_{DD} + 0.5 (≤ 4.0 V) *3	
Storage temperature	Tst	−55	+125	°C
Junction temperature	T_j	−40	+125	°C
Output current*4	I_O	±10 (3.3 V CMOS, 2.5 V CMOS)		mA
		± 7.5 (1.8 V CMOS)		
Input signal transfer rate	R_I	—	Clock input*5 : 200 Normal input : 100	Mbps*6
Output signal transfer rate	R_O	—	100	Mbps*6
Output load capacitance	C_O	—	3000/R_O	pF
Supply pin current	I_D	—	* 7	mA

*1 : V_{SS} = 0 V.

*2 : Internal gate area when single-power supply and dual-power supply are used.

*3 : I/O area when 3.3 V I/F or 2.5 V I/F is used with dual-power supply.

*4 : DC current that continuously flows for 10 ms or more, or average DC current.

*5 : It is required to use I/O cells for clock input.

*6 : bps = bit per second.

*7 : Refer to "• Supply pin current per V_{DD}/GND pin (mA)"

• Supply pin current per V_{DD}/GND pin (mA)

(a) Maximum Current Per Power Supply I/O *1

T_j = +125 °C*2

Frame	Source type	Maximum current (with standard power supply) (mA)	Number of layers
YH, XH, YI, XI	V_{DDE}	68	4
	V_{DDE}	59	5
	V_{DDE}	59	6
	V_{DDI}, V_{DD}, V_{SS}	68	4
	V_{DDI}, V_{DD}, V_{SS}	93	5
	V_{DDI}, V_{DD}, V_{SS}	118	6

(b) Current Supply Per Supply I/O to the core

$T_j = +125°C$*2

Frame	Source type	Maximum current (with standard power supply) (mA)	Number of layers
YH, XH, YI, XI	V_{DDI}, V_{DD}, V_{SS}	34	4
	V_{DDI}, V_{DD}, V_{SS}	34	5
	V_{DDI}, V_{DD}, V_{SS}	59	6

*1 : The maximum current per power supply I/O includes the power supplied to the I/O area and the power supplied to the core.

*2 : The current that can be supplied per power supply I/O to the core depends on the junction temperature. When Tj is not +125 °C, multiple the values of maximum current by the following values to calculate the maximum current for each Tj.
The current that can be supplied per power supply I/O to the core depends on the junction temperature. When Tj is not +125 °C, multiple the values of maximum current by the following values to calculate the maximum current for each Tj.
Tj = +111 °C to +125 °C : 1.0
Tj = +91 °C to +110 °C : 1.4
Tj = to +90 °C : 2.8

Note : Calculation of Power Supply Pins
Example :
(wiring layer=6, Tj=+125 °C)
- Maximum current per V_{DD}, GND pin
  V_{DDE} = 59 mA/pin (Refer to " (a) Maximum Current Per Power Supply I/O*1")
  $V_{DDI} = V_{SS}$ = 59 mA/pin (Refer to " (b) Current Supply Per Supply I/O to the core")
- Required number of power supplies (internal / external /V_{SS}) : Ni/Ne/Ns
  Maximum DC internal power-supply current : Iimax,
  Maximum DC external power-supply current : Iemax
  Ni = Iimax/59 mA, Ne = Iemax/59 mA, Ns = Iimax/59 mA + Iemax/59 mA

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

- **Single power supply** (V_{DD} = 1.8 V ± 0.15 V)

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{DD}	1.65	1.8	1.95	V
"H" level input voltage	V_{IH}	V_{DD} × 0.65	—	V_{DD} + 0.3	V
"L" level input voltage	V_{IL}	–0.3	—	V_{DD} × 0.35	V
Junction temperature	T_j	–40	—	+125	°C

- **Dual power supply** (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.65	1.8	1.95	
			1.4	1.5	1.6	
"H" level input voltage	1.8 V CMOS	V_{IH}	V_{DDI} × 0.65	—	V_{DDI} + 0.3	V
	3.3 V CMOS		2.0	—	V_{DDE} + 0.3	
"L" level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	V_{DDI} × 0.35	V
	3.3 V CMOS		–0.3	—	+0.8	
Junction temperature		T_j	–40	—	+125	°C

- **Dual power supply** (V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	1.65	1.8	1.95	
			1.4	1.5	1.6	
"H" level input voltage	1.8 V CMOS	V_{IH}	V_{DDI} × 0.65	—	V_{DDI} + 0.3	V
	2.5 V CMOS		1.7	—	V_{DDE} + 0.3	
"L" level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	V_{DDI} × 0.35	V
	2.5 V CMOS		–0.3	—	+0.7	
Junction temperature		T_j	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC characteristics

• Single power supply : V_{DD} = 1.8 V standard

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH}	I_{OH} = –100 µA	V_{DD} – 0.2	—	V_{DD}	V
"L" level output voltage	V_{OL}	I_{OL} = 100 µA	0	—	0.2	V
"H" level output V-I characteristics	—	1.8 V V_{DD} = 1.8 V ± 0.15 V	*			—
"L" level output V-I characteristics	—	1.8 V V_{DD} = 1.8 V ± 0.15 V	*			—
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	Pull up V_{IL} = 0, Pull down V_{IH} = V_{DD}	8	18	40	kΩ

* : Refer to " (1) 1.8 V" in ■V-I CHARACTERISTICS.

• Dual power supply : V_{DDE} = 3.3 V, V_{DDI} = 1.8 V/1.5 V/1.1 V

(V_{DDE} = 3.3 V±0.3 V/V_{DDI} = 1.8 V ± 0.15 V, V_{DDI} = 1.5 V ± 0.1 V, V_{DDI} = 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH4}	3.3 V Output I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	
"L" level output voltage	V_{OL4}	3.3 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	
"H" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V ± 0.3 V	*1			—
		1.8 V V_{DDI} = 1.8 V ± 0.15 V	*2			
"L" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V ± 0.3 V	*1			—
		1.8 V V_{DDI} = 1.8 V ± 0.15 V	*2			
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	3.3 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	10	33	80	kΩ
		1.8 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	8	18	40	

*1 : Refer to " (2) 3.3 V" in ■V-I CHARACTERISTICS.

*2 : Refer to " (1) 1.8 V" in ■V-I CHARACTERISTICS.

• Dual power supply : V_{DDE} = 2.5 V, V_{DDI} = 1.8 V/1.5 V/1.1 V
(V_{DDE} = 2.5 V±0.2 V, V_{DDI} = 1.8 V ± 0.15 V/V_{DDI} = 1.5 V ± 0.1 V/V_{DDI} = 1.1 V ± 0.1 V,
V_{SS} = 0 V, T_j = –40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"H" level output voltage	V_{OH3}	2.5 V Output I_{OH} = –100 µA	V_{DDE} – 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V Output I_{OH} = –100 µA	V_{DDI} – 0.2	—	V_{DDI}	
"L" level output voltage	V_{OL3}	2.5 V Output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V Output I_{OL} = 100 µA	0	—	0.2	
"H" level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V ± 0.2 V	—			—
		1.8 V V_{DDI} = 1.8 V ± 0.15 V	*			
"L" level output V-I characteristics	—	2.5 V V_{DDE} = 2.5 V ± 0.2 V	—			—
		1.8 V V_{DDI} = 1.8 V ± 0.15 V	*			
Input leakage current	I_L	—	—	—	±5	µA
Pull up/Pull down resistance	R_P	2.5 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDE}	—	25	—	kΩ
		1.8 V Pull up V_{IL} = 0, Pull down V_{IH} = V_{DDI}	8	18	40	

* : Refer to " (1) 1.8 V" in ■V-I CHARACTERISTICS.

2. AC characteristics

(V_{SS} = 0 V, T_j = – 40 °C to +125 °C (Standard))

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Delay time	t_{pd}*1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

*1 : Delay time = propagation delay time, enable time, disable time.

*2 : "typ" is calculated based on the cell specifications.

*3 : Measurement conditions

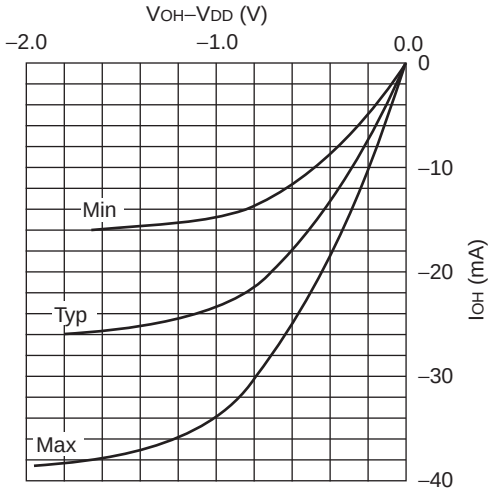
Measurement condition	tmin	ttyp	tmax
V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.62	1.00	1.88
V_{DD} = 1.5 V ± 0.10 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	0.76	1.25	2.42
V_{DD} = 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = –40 °C to +125 °C	1.08	2.14	6.22

Note : AC characteristics are determined based on junction temperature, voltage conditions, and process variation.

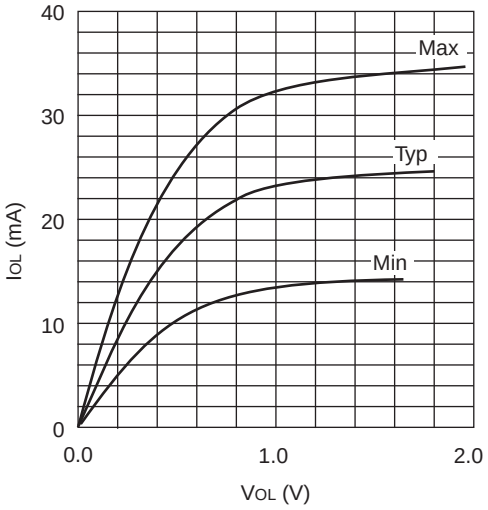
■ V - I CHARACTERISTICS

(1) 1.8 V

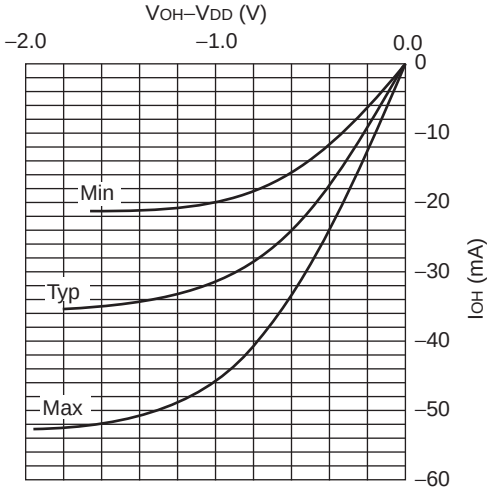
Conditions Min : Process = Slow, T_j = +125 °C, V_{DD} = 1.65 V
Typ : Process = Typical, T_j = +25 °C, V_{DD} = 1.80 V
Max : Process = Fast, T_j = –40 °C, V_{DD} = 1.95 V



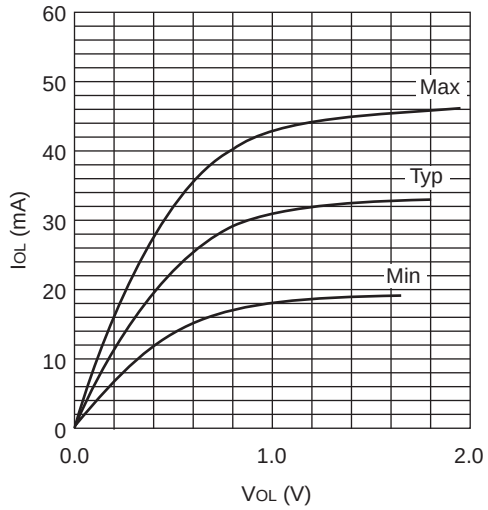
1.8 V CMOS “H” level output
(L, M type)



1.8 V CMOS “L” level output
(L, M type)



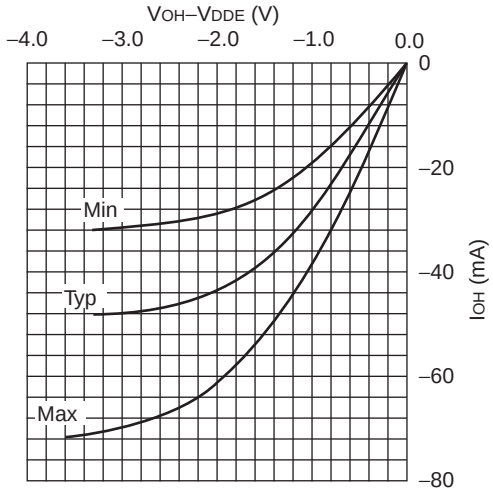
1.8 V CMOS “H” level output
(H, V type)



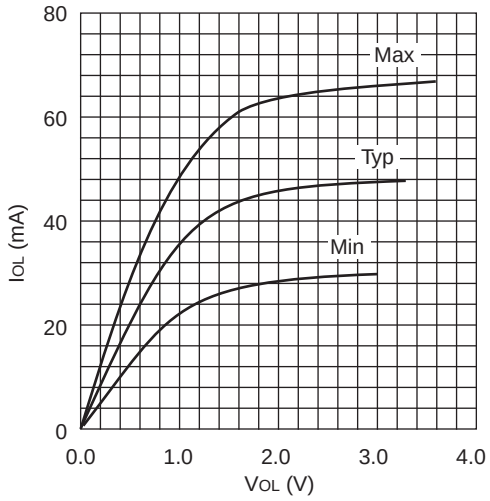
1.8 V CMOS “L” level output
(H, V type)

(2) 3.3 V

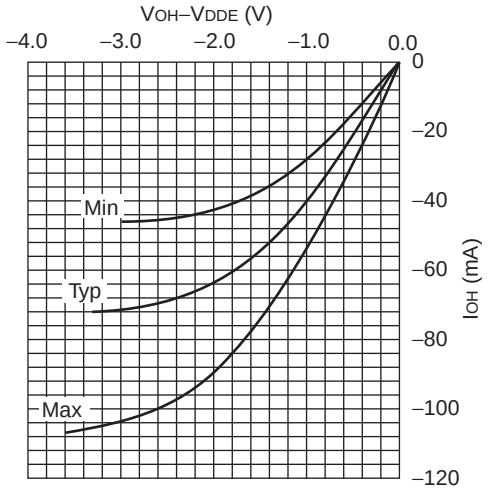
Conditions Min : Process = Slow, T_j = +125 °C, V_{DDE} = 3.0 V
Typ : Process = Typical, T_j = +25 °C, V_{DDE} = 3.3 V
Max : Process = Fast, T_j = –40 °C, V_{DDE} = 3.6 V



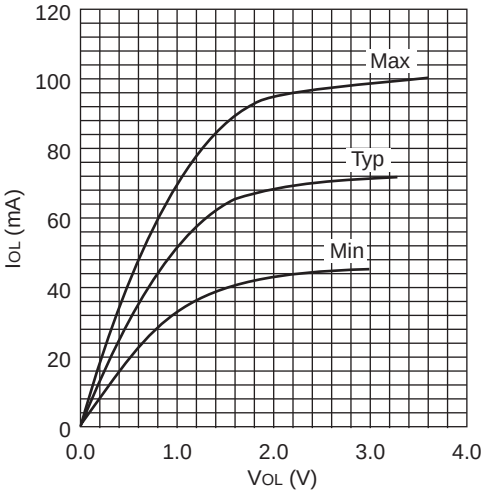
3.3 V CMOS “H” level output
(L, M type)



3.3 V CMOS “L” level output
(L, M type)



3.3 V CMOS “H” level output
(H, V type)



3.3 V CMOS “L” level output
(H, V type)

■ INPUT/OUTPUT PIN CAPACITANCE

(T_j = +25 °C, V_{DD} = VI = 0 V, f = 1 MHz)

Parameter		Symbol	Requirements	Unit
Input pin	—	CIN	Max 16	pF
Output pin	L, M, H, V type	COUT	Max 16	pF
I/O pin	L, M, H, V type	CI/O	Max 16	pF

Note : Capacitance varies according to the package and the location of the pin.

■ DESIGN METHOD

Fujitsu Microelectronics's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

• Physical Prototyping

Compared with the conventional style, Physical Prototyping provides more accurate estimation in the early stage of physical design.

Therefore an early confirmation of chip sizes, interconnection, timing and etc. can be reached, allowing satisfied pieces of ASIC design to be converged within the scheduled development period.

• Low Power

The Low Power Synthesis tool is supported, which enables the use of gated clock buffers with latch.

The use of gated clock buffers of hard macro type provides low power consumption by the clock line. It also provides reliable operation, reduction in script complexity, and shorter turnaround time (TAT) for processing.

• Timing Closure

By using Physical Synthesis Tool, design layout is optimized.

This prevents post-layout timing problems from developing, which are prominent in particular in the field of deep submicron designs.

Fujitsu Microelectronics's hold timing error correction system is provided, by which multiple timing restrictions are considered at the same time for advanced SoC with complex system mode. This shortens the development time from the end of creating a net list to the beginning of manufacturing engineering samples.

• Hierarchical Design

A top-down hierarchical design approach is taken consistently from logic design to physical design to support larger-scale circuit integration based on deep submicron designing. This enables multiple blocks to be designed logically and physically at the same time and timing convergence to be attained in a short period, providing a design environment capable of easily supporting large-scale integration of circuits.

• Support for Signal Integrity

To avoid remake power mash on late stage of layout, estimate the power mesh ratio based on Power consumption and IR-Drop.

Also, a verification system is prepared to check the x-talk noise and delay penalty caused by coupling capacitance between signal wires and the voltage drop caused by simultaneous local switching.

■ PACKAGES

Package	Pin count	Material
QFP	208, 240	Plastic
LQFP	144, 176, 208, 256	Plastic
HQFP	208, 240, 256, 304	Plastic
FBGA	112, 144, 176, 192, 224, 240, 272, 288, 304, 368	Plastic

Note : The packages that can be used depend on the circuit configuration. For details, contact Fujitsu Microelectronics.

FUJITSU MICROELECTRONICS LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-8508, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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