FR FAMILY
32-BIT MICROCONTROLLER
MB91460

A/D CONVERTER

APPLICATION NOTE
Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008-04-23</td>
<td>V1.0, First draft, HPi</td>
</tr>
</tbody>
</table>

This document contains 27 pages.
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1 Introduction

This application note describes the functionality of the Analog/Digital Converter (ADC) and gives some examples.

1.1 Key Features

- Minimum conversion time per Channel: 3 µs
- RC type successive approximation conversion with sample & hold circuit
- 8-bit or 10-bit conversion resolution
- Sequential channel conversion, once (Single Mode), continuous (Continuous Mode) and converts one channel, stops and waits for the next activation (Stop Mode)
- Interrupt generation after conversion selectable
- Interrupt can trigger DMA to transfer conversion result to memory
- Triggered by software, external Pin (ATG) or Timer
2 The Analogue/Digital Converter

THE BASIC FUNCTIONALITY OF THE ANALOGUE/DIGITAL CONVERTER

2.1 Block Diagram

Figure 2-1 shows the internal block diagram of the ADC.

![Figure 2-1: ADC Block Diagram](image)
2.2 Registers

2.2.1 Control Status Register (ADCS1)

This register controls the A/D converter and indicates its status.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>BUSY*</td>
<td>Busy Flag/Stop*</td>
<td>0</td>
<td>0</td>
<td>Read: No A/D Conversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Write: Force Conversion Stop</td>
<td></td>
<td>1</td>
<td>Write: No effect</td>
</tr>
<tr>
<td>14</td>
<td>INT</td>
<td>Interrupt Flag</td>
<td>0</td>
<td>0</td>
<td>Read: A/D Conversion ongoing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Write: Clear Flag</td>
<td></td>
<td>1</td>
<td>Write: No effect</td>
</tr>
<tr>
<td>13</td>
<td>INTE</td>
<td>Interrupt enable</td>
<td>0</td>
<td>0</td>
<td>Interrupt disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Write: No effect</td>
<td></td>
<td>1</td>
<td>Interrupt, if A/D Data</td>
</tr>
<tr>
<td>12</td>
<td>PAUS</td>
<td>A/D Converter Pause</td>
<td>0</td>
<td>0</td>
<td>Read: No A/D Conversion Pause</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Write: Clear Bit</td>
<td></td>
<td>1</td>
<td>Write: No effect</td>
</tr>
<tr>
<td>11, 10</td>
<td>STS1,0</td>
<td>Start Source Select</td>
<td>0, 0</td>
<td>0</td>
<td>ADC Activation by Software</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>ADC Activation by Software and ADTG Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADC Activation by Software and Timer, ADTG Pin, and Timer</td>
</tr>
<tr>
<td>9</td>
<td>START</td>
<td>Start Conversion</td>
<td>0</td>
<td>0</td>
<td>Always read; Write: no effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Start and Restart A/D Conversion</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td>Undefined</td>
<td>X</td>
<td>0</td>
<td>Reserved Bit, always write &quot;0&quot; to it</td>
</tr>
</tbody>
</table>

Table 2-1: ADCS1

2.2.2 Control Status Register (ADCS0)

This register controls the A/D converter and indicates its status.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>7, 6</td>
<td>MDL, 0</td>
<td>Operation Mode Select</td>
<td>0, 0</td>
<td>0</td>
<td>Single Mode 1; Reactivation during Conversion allowed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0, 1</td>
<td>Single Mode 2; Reactivation during Conversion not allowed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1, 0</td>
<td>Continuous Mode; Reactivation during Conversion not allowed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1, 1</td>
<td>Stop Mode; Reactivation during Conversion not allowed</td>
</tr>
<tr>
<td>5</td>
<td>S10</td>
<td>10-Bit Mode</td>
<td>0</td>
<td>0</td>
<td>10-Bit Conversion Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>8-Bit Conversion Mode</td>
</tr>
<tr>
<td>4 ... 0</td>
<td>ACH4-ACH0</td>
<td>A/D converter mode set</td>
<td>00000</td>
<td>Read</td>
<td>Current converted channel is shown during A/D converting (BUSY=&quot;1&quot;). If conversion is halt by forcibly stopping, they show the stopped channel.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write</td>
<td>No effect to these bits.</td>
</tr>
</tbody>
</table>

Table 2-2: ADCS0

* These bits return “1” during Read-Modify-Write instruction.
2.2.3 Date Register (ADCR1, ADCR0)
These register stores digital value generated as a result of conversion. This register contains the last converted value and is rewritten every time the conversion ends.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>These bits always return &quot;0&quot;</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>D9</td>
<td>Data Bits</td>
<td>-</td>
<td>These bits contain A/D data after successful conversion</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 2-3: ADCR1 & 2**

2.2.4 Sampling timer and setting register (ADCT1, ADCT0)
These registers sets the sampling and conversion time

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CT5</td>
<td>Comparison</td>
<td>0,0,0,1,0,0</td>
<td>Setting &quot;000001&quot; means one division (=CLKP). It’s not allowed to set these bits &quot;000000&quot; Note: It’s not allowed to set the comparison time over 500 us</td>
</tr>
<tr>
<td>...</td>
<td>CT0</td>
<td>Time Setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>ST9</td>
<td>Sampling</td>
<td>0,0,0,0,1,0,1</td>
<td>Sampling time = ST value * CLKP cycle Note: It’s not allowed to set the sampling time below 1.2 us when AVCC is below 4.5 V.</td>
</tr>
<tr>
<td>...</td>
<td>ST0</td>
<td>time</td>
<td>0,1,1,0,0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 2-4: ADCT1 & 2**

2.2.4.1 Sampling/Conversion Time
The sampling time must be equal to or greater than 0.4 μs. The Comparison time must be at least 0.6 μs. Therefore an overall A/D conversion time could be 1 μs, but this depends on the used peripheral clock.

Assume a peripheral clock of 16 MHz (62.5 ns cycle time). The sample cycle number then has at least to be 8 (0.5 μs) and the conversion cycle number can be 10 (0.625 μs). Therefore the overall A/D conversion time is 1.125 μs.

All these settings are valid for \( 4.5 \, \text{V} \leq \text{AVcc} \leq 5.5 \, \text{V} \). Please see the hardware manual for external impedance considerations.

Please consider that the source clock frequency of the Reload Timer (CLKP) depends on the settings of the Clock Division setting register (DIVR0).

\[
\text{DIVR0_P [3:0]} \quad \text{Base Clock} \quad \text{Peripheral Clock Divider (div-1 to div-16)} \quad \text{CLKP} \quad \text{to ADC}
\]

**Figure 2-2: ADC Clock**
2.2.5 A/D Channel Setting Register (ADSCH, ADECH)

These registers specify the channels for the A/D converter to convert. Do not update these registers while the A/D converting is operating.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>…</td>
<td>Undefined</td>
<td>X</td>
<td>0</td>
<td>Reserved Bit, always write “0” to it</td>
</tr>
<tr>
<td>13</td>
<td>…</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>ANS4</td>
<td>Starting</td>
<td>0</td>
<td>00000</td>
<td>Start conversion from Channel 0</td>
</tr>
<tr>
<td>8</td>
<td>…</td>
<td>Channel</td>
<td></td>
<td>…</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>ANS0</td>
<td>Setting</td>
<td></td>
<td>11111</td>
<td>Start conversion from Channel 31</td>
</tr>
<tr>
<td>5</td>
<td>…</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ANE4</td>
<td>Ending</td>
<td>0</td>
<td>00000</td>
<td>End conversion at Channel 0</td>
</tr>
<tr>
<td>0</td>
<td>…</td>
<td>Channel</td>
<td></td>
<td>…</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ANE0</td>
<td>Setting</td>
<td></td>
<td>11111</td>
<td>End conversion at Channel 31</td>
</tr>
</tbody>
</table>

Table 2-5: ADSCH & ADECH

2.2.5.1 Start/Stop Channels

- Use start channel = end channel for conversion of only one channel.
- If start channel is greater than end channel, conversion starts from start channel to the highest available channel, then from channel 0 to the end channel.
2.2.6 Analog Input Enable Register ($\text{ADER}_0 - \text{ADER}_n$)

While a pin is used as analog input, corresponding bit in $\text{ADER}$ register have to be set to 1. If a channel between the configured scanning limits is not configured as ADC input (the corresponding bit in this register is “0”), this channel is skipped during the scanning process.

The following table shows $\text{ADER}_H$.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ADE31</td>
<td>ADC Input Selection</td>
<td>0</td>
<td>0</td>
<td>Digital I/O Port enabled</td>
</tr>
<tr>
<td>...</td>
<td>ADE16</td>
<td></td>
<td></td>
<td>1</td>
<td>Analog Input enabled</td>
</tr>
</tbody>
</table>

Table 2-6: $\text{ADER}_H$

The following table shows $\text{ADER}_L$.

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Initial Value</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ADE15</td>
<td>ADC Input Selection</td>
<td>0</td>
<td>0</td>
<td>Digital I/O Port enabled</td>
</tr>
<tr>
<td>...</td>
<td>ADE0</td>
<td></td>
<td></td>
<td>1</td>
<td>Analog Input enabled</td>
</tr>
</tbody>
</table>

Table 2-7: $\text{ADER}_L$
3 Power supply of A/D converter

ELECTRICAL POWER CONSIDERATIONS

3.1 Power consumption

The power consumption (I_R, I_A) of the ADC increases in case a conversion is in progress (ADCSH_BUSY = 1). While the ADC is halted (ADCSH_BUSY = 0), only leakage current (I_RH, I_AH) flows. The following diagrams reflect this behaviour:

![Diagram of power consumption and operating status of ADC]

Note:
Please refer to the datasheet in order to get the absolute values of I_R, I_RH, I_A, and I_AH.

3.2 Noise consideration

Fujitsu microcontroller has implemented an embedded 10-bit Successive Approximated Register (SAR) ADC. Due to the high resolution, the digital bit stream from the ADC output is sensitive to the environment noise. For example, 1LSB corresponds to only 4.9mV for U_REF=5V. Hence, the noise introduced from the external circuits must be considered and should be reduced to the minimum as possible.
The reference voltage $U_{\text{REF}}$, which is equal to $AVRH-AVRL$, is connected to the weighted capacitor array and the resistor array of the ADC. The noise coupled to AVR will not be rejected by ADC. This noise will be added to the $U_{\text{REF}}$ directly, introducing an error with a ratio of $U_{\text{Noise}}/U_{\text{REF}}$. For example, to keep the error caused by this kind of noise below 0.1\text{LSB}, the noise level of $U_{\text{REF}}$ must be kept within 0.49mV.

As a result, the pin AVRH and AVRL pins must be connected with low impedance. In practice often a simple low-pass RC-filter is used for noise reduction. In this case the reference voltage supply current (see datasheet) has to be taken into account when calculating the resistor of the filter, in order to minimize the voltage drop while converting. Normally two capacitors in parallel are recommended, one filtering low frequency noise, the other one filtering high frequency noise ($((10\text{nF}-1\mu F)||(10\text{pF}-100\text{pF}))$). In most cases, this configuration suppresses the noise efficiently. If very high frequency noise appears in the environment, an additional noise filter such as a dedicated $\pi$ mode RC filter might be useful.

The analogue power path $AV_{\text{CC}}$ supplies the internal voltage comparator and the analogue switches of the ADC, while the $V_{\text{CC}}$ path supplies all the digital parts in the microcontroller. Internal parasitic capacitors may couple noise from $AV_{\text{CC}}$ to the internal voltage comparator of the ADC. For this reason, also $AV_{\text{CC}}$ should not be connected directly to $V_{\text{CC}}$ but filter should be used, too. For more efficient noise filtering the same configuration as for AVRH is recommended.

![Figure 3-2: A suggested connection for the power supplies](image-url)
4 Analogue input and related external circuits

4.1 External circuits for analogue input

To protect the analogue pins to suffer from an over-voltage, the so-called “clamping resistor” is usually added to the input pins. The minimum value of the resistor can be chosen as

$$R_{\text{clamp}} = \frac{U_{\text{overvoltage}}}{I_{\text{clamp}}}$$

Where, $I_{\text{clamp}}$ is the specified maximum clamp current in the data sheet.

For some applications, a large clamp resistor is sometimes unacceptable. As a compromise, an external clamping diode with low leakage current could be added between the input pin and AVCC pin.

In some cases, the sensor has been biased with a voltage supply higher than the maximum allowed voltage for the microcontroller. For example, in the automotive applications, the sensors could be biased directly with the car battery, which exhibits a voltage of 12V/24V. A resistor divider consisting of $R_1/R_2$ is commonly used to tail the sensor voltage signal “seen” on the pin down to the value which is equal or smaller than AVCC/VCC (see Figure 4-1).

The ratio between $R_1$ and $R_2$ should satisfy the following constrain:

$$\frac{R_1}{R_2} \geq \frac{U_{\text{signal}}}{AVCC} - 1$$

Other factor which influences the size dimension of $R_1$, $R_2$ and $R_{\text{clamp}}$, is related to current consumption budget and the input signal noise suppressing. The second factor will be discussed here with more detail. The signal from the sensors could be also noisy. The noise, which has a time constant smaller than the sampling time $T_{\text{sampling}}$, is transparent to the ADC, resulting distorted output. In this case, an additional dedicated bypass capacitor together with the clamping resistor or resistor divider, works as a low pass filter. A larger capacitor will lower the AC impedance and will be more effective at shunt away the noise signal. Generally, the time constant of this low pass filter ($R_{\text{clamp}} + R_1 || R_2) x C_{\text{noise}}$ should be chosen considerably larger than the sampling time (5 to 10 times larger with a rule of thumb).

However, at the same time this time constant should be also considerably smaller than the one of the sensor signal, depending on the applications. In this way, the analogue pin is able to follow the dynamic changes, which the ADC is being used to track. These, along with the
dimension of $R_1/R_2$ or $R_{clamp}$ must be considered when choosing the capacitor dimension to avoid rolling off any high frequency signal components of interest.

### 4.2 Input Leakage current consideration

The analogue input pins show a small leakage current, whose maximum value is about 3µA and ranged from 3µA down to 1µA depending on the temperature. The leakage current, which flows through the external resistor, introduces an undesired voltage drop. This error voltage is a function of the external resistor and the leakage current itself. The following example shows a dimension of the resistor with this factor taken into consideration. For the case of using a resistor divider to reduce the error due to leakage current, the size of $R_1 \parallel R_2 + R_{clamp}$ should not be chosen too large and should be according to the following equation:

$$R_1 \parallel R_2 + R_{clamp} \leq \frac{U_{LSB}}{I_{leakage}}$$

Note:

$$U_{LSB} = \frac{U_{REF}}{1024}$$

To keep the error smaller than one LSB for a leakage of 3µA, the size of $R_1 \parallel R_2 + R_{clamp}$ should be smaller than 1.6kΩ. As the leakage current drops down to 1µA, the value of $R_1 \parallel R_2 + R_{clamp}$ can be chosen as large as 5kΩ. This is considering $U_{REF}$ of 5V.

It is found in the test that the leakage current consists of two parts: one is due to the leakage current of the input ESD structure. Another leakage current appears only as the multiplexer is switched on during the sampling time, whose contribution is usually considerably larger than the one created from ESD structure. The second leakage current can be regarded as a noise during the sampling time by the bypass capacitor, which is commonly used to filter the noise from the sensor input. If this capacitor is large enough, it can absorb most of the second leakage current during the sampling time, eliminating its contribution to the error voltage.

![Figure 4-2: Leakage current flowing to the analogue input pin](image-url)
To show the effect of the bypass capacitor on reducing the leakage current error, we take a sampling time of 5 µs and a leakage current of 3 µA as an example. If we want to keep the voltage drop due to the second leakage current smaller than 0.5 LSB, the minimum size of the bypass capacitor should be chosen as:

\[
C = \frac{3 \mu A \times 5 \mu s}{4.9mV / 2} \approx 6nF
\]
5 Sampling time consideration

**SAMPLING TIME CONSIDERATION**

Fujitsu applies an embedded 10-bit successive approximation register ADC with an internal integrated sampling and hold stage. The signal will charge the sampling capacitor at first and then the voltage signal on the sampling capacitor will be evaluated by the 10-bit ADC successively. The time to charge the sampling capacitor to its final value equal to the signal level is a function of the sampling capacitor $C_{\text{sampling}}$, the external resistor and the internal switch on-resistor.

To reduce the error caused by the limited sampling time to an acceptable level, the sampling time should be chosen much larger than the time constant to charge the sampling capacitor. For example, if we choose a sampling time with a factor 7 of the RC constant, namely, $7 \times (R_{\text{extern}} + R_{\text{switch}}) \times C_{\text{sampling}}$. Then the error amounts to $e^{-7} \times U_{\text{REF}}$, corresponding to $0.94 \times U_{\text{LSB}}$ only.

For MB91467D Series, the on-resistor of the transmission gate amounts to 2.6kΩ and the sampling capacitor $C_{\text{sampling}}$ equals to 11pF at $AV_{\text{CC}} = 5V$. For an external resistor of 2.25kΩ, the sampling time should be chosen larger than $7 \times (2.25k\Omega + 2.6k\Omega) \times 11pF = 0.37 \mu s$ by using above thumb rule.

![Figure 5-1: Block diagram for ADC in MB91F460D Series](image)
For the Fujitsu microcontroller the sampling time can be set by defining the register bit ST2 to ST0 of the ADC data register (ADCT). Please refer to the hardware manual.
6 Latch-up related to AV\textsubscript{CC}/V\textsubscript{CC} and large input signal

RECOMMENDATIONS TO PREVENT LATCH-UP

Latch-up conditions can permanently damage the device and must be avoided. It is up to the application to assign any precautions in order to avoid any latch-up condition.

6.1 AV\textsubscript{CC} > V\textsubscript{CC}

Latch-up can happen if AV\textsubscript{CC} becomes larger than V\textsubscript{CC}. This might be related to the application cases that V\textsubscript{CC} is switched on later than AV\textsubscript{CC} or V\textsubscript{CC} is switched off earlier than AV\textsubscript{CC}. The ESD diode D3 becomes forward biased, introducing a possible latch-up.

6.2 AV\textsubscript{CC} < V\textsubscript{CC}

This case happens if the analogue pin is used as a digital output pin, the output level is "H", and at the same time, AV\textsubscript{CC} is switched off. In this case, the PMOS in the output is on and
the parasitic diode D2 of the transmission gate within the analogue multiplex becomes forward biased. A quiescent current flows through PMOS and D2. In case that a latch-up does not happen, a reliable logic “1” should not be expected at the output, due to the load diode D2.

6.3 $U_{\text{AIN}} > AV_{\text{CC}}$ or $V_{\text{CC}}$

If $U_{\text{AIN}}$ becomes larger than $V_{\text{CC}}$ or $AV_{\text{CC}}$, then the ESD diode D1 or D2 will be forward biased. A latch-up can happen. Even if a latch-up does not always happen in this case, the input signal, which exceeds $V_{\text{CC}}$ or $AV_{\text{CC}}$, cannot be converted by the ADC properly.

6.4 Conclusion

It is strongly suggested that $AV_{\text{CC}}$ and $V_{\text{CC}}$ should be DC short circuit together to avoid any possible latch-up.

With the presence of $AV_{\text{CC}}$ and $V_{\text{CC}}$ voltage, an analogue input signal, which is smaller than $AV_{\text{CC}}$ and $V_{\text{CC}}$ can be always put on the analogue pins, independent on the MCU modes.

Latch-up conditions can permanently damage the device if the related specified currents are exceeded. So Latch-up conditions must be avoided under all circumstances. It is up to the application to assign any precautions in order to avoid any latch-up condition.
7 Input Impedance

**ADC BEHAVIOR ON HIGH INPUT IMPEDANCES**

### 7.1 Recharging and discharging the Sampling capacitor

Because the ADC uses a sampling capacitor the input impedance must be set to a value below 15 kΩ to recharge or discharge this capacitor within the sampling time.

**Example:**

Assume an application uses two ADC inputs. At one pin there is a voltage of about Vcc and at the other pin Vss. The first conversion charges the internal capacitor to Vcc within the sample time (A). After this the conversion starts (B). At the second conversion the MUX switches to the other input and the capacitor is discharged to Vss (C). The second conversion starts (D). If the input impedance ($Z_0$) is too high, a rest of charge will remain and a wrong conversion will result.

![Figure 7-1: Current flow in the example](attachment:image1.png)

The left illustration shows the voltage glitch on AN0 if $Z_0$ is low.

The glitch occurs, when the sampling switch is closed.

![Figure 7-2: Voltage glitch at low input impedance](attachment:image2.png)
In this illustration the input impedance $Z_0$ is too high. The sampling capacitor is not discharged within the sampling time and thus a wrong voltage is converted (red circle).

![Diagram](Image)

**Figure 7-3: Voltage glitch at high input impedance**

**Note:**

At high impedance input circuit, there will always be a glitch of about 0.5 Volts max even if the previous conversion was at 0 Volt. This results from the ADC internal architecture itself.

For the same reason discussed in this chapter an EMI capacitors for any analogue input pins should not exceed 1 nF.
8 ADC Example

EXAMPLES FOR THE ADC

8.1 ADC with interrupts

Main.c

```c
/* THIS SAMPLE CODE IS PROVIDED AS IS AND IS SUBJECT TO ALTERATIONS. FUJITSU */
/* MICROELECTRONICS ACCEPTS NO RESPONSIBILITY OR LIABILITY FOR ANY ERRORS OR */
/* ELIGIBILITY FOR ANY PURPOSES.                                             */
/* (C) Fujitsu Microelectronics Europe GmbH                                    */
/*---------------------------------------------------------------------------*/
void InitADC (void)
{
    PFR29_D1 = 1;       /* resource function mode: analog input AN1 */
    ADERL = 0x0002;  /* channel 1 to analog input             */
    ADCS0 = 0xA0;  /* ADC set to 8 bit continuous mode      */
    ADCT1 = 0xFF;  /* Comparison time = 39.62uS @ 16MHz CLKP*/
    ADCT0 = 0xFF;  /* Sampling time = 63.94uS @ 16MHz CLKP */
    ADSCH = 0x01;  /* convert only AN1 */
    ADECH = 0x01;
    ADCS1 = 0xA2;  /* interrupt enabled, software trigger, 
                     start conversion */
}
void main (void)
{
    DDR00 = 0xFF ; /* Data direction Port 0 = Output */
    InitIrqLevels();
    __set_Il(7);  /* allow all levels */
    __EI();  /* globally enable interrupts */
    PFR16 = 0x00;
    DDR16 = 0xFF;
    PDR16 = 0x00;
    InitADC();  /* init AD - converter */
    while(1)  /* waiting for interrupt (no operation) */
        __asm("\tnop");
}
__interrupt void ISR_ADC (void)
{
    PDR16 = ADR0;  /* shows voltage on Port 0 ( LEDs ) */
    ADCS1 = 0xA2;  /* clear interrupt flag */
}
```

The above example demonstrates to configure ADC in the continuous mode with 8 bit conversion resolution with interrupts enabled. The maximum possible sampling and comparison time is used here. After every ADC interrupt the converted data is output to the LEDs connected to Port 16.
void InitIrqLevels (void)
{
    ...
    ICR59 = 30; /* Priority Level 30 for ADC */
    ...
}

/* ISR prototype */
__interrupt void ISR_ADC (void);
    ...

#pragma intvect ISR_ADC 134 /* ADC */
    ...
9 Additional Information

Information about FUJITSU Microcontrollers can be found on the following Internet page:

http://mcu.emea.fujitsu.com/

The software examples related to this application note is:

91460_adc8-v10
91460_adc_rlt-v10
91460_adc8_dma-v14
91460_ppg_rlt_adc_dma-v10
91460_adc8_uart_async-v13
91460_adc10_dma_irq-v12

It can be found on the following Internet page:

http://mcu.emea.fujitsu.com/mcu_product/mcu_all_software.htm
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