FR FAMILY
32-BIT MICROCONTROLLER
MB91460

PULSE FREQUENCY MODULATOR

APPLICATION NOTE
Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008-06-05</td>
<td>V1.0, First draft, HPi</td>
</tr>
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This document contains 14 pages.
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1 Introduction

The PFM is used to generate pulses of a short duration in a long period. This is an alternative to using PWM signals in some applications.

The 16-bit pulse frequency modulator consists of two 16-bit down-counters, two 16-bit reload registers, prescalers for generating the internal count clocks and control/status registers.

1.1 Key Features

- Two independent programmable 16-bit down-counters generating low and high pulses
- The input clock (count clock) can be selected from prescaled internal clocks (the peripheral clock (CLKP) divided by 2/8/32/64/128) separately for each counter.
- The mark level and output waveform can be inverted.
2 Pulse Frequency Modulator

THE BASIC FUNCTIONALITY OF PULSE FREQUENCY MODULATOR IS EXPLAINED

2.1 Block Diagrams

Figure 2-1 shows the internal block diagram of a Pulse Frequency Modulator.
### 2.2 Registers

#### 2.2.1 Control status register \((P0TMCSR, \ P1TMCSR)\)

Controls the operation mode, shows the status of the reload counter and interrupts for the 16-bit reload. Only change the value of bits other than \(UF\) and \(TRG\) when \(CNTE = "0"\).

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Name</th>
<th>Explanation</th>
<th>Value</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>-</td>
<td>Reserved</td>
<td>-</td>
<td>(Always\ set\ to\ \ '0')</td>
</tr>
<tr>
<td>14</td>
<td>INV</td>
<td>The output signal inversion bit</td>
<td>0</td>
<td>counter 0 high level, counter 1 low level</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>counter 0 low level, counter 1 high level</td>
</tr>
<tr>
<td>13</td>
<td>-</td>
<td>Reserved</td>
<td>-</td>
<td>(Always\ set\ to\ \ '0')</td>
</tr>
<tr>
<td>12-10</td>
<td>CSL2,</td>
<td>The count clock select bits</td>
<td>000</td>
<td>CLKP / (2^1)</td>
</tr>
<tr>
<td></td>
<td>CSL1,</td>
<td></td>
<td>001</td>
<td>CLKP / (2^3)</td>
</tr>
<tr>
<td></td>
<td>CSL0</td>
<td></td>
<td>010</td>
<td>CLKP / (2^5)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011</td>
<td>saved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>Clock disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101</td>
<td>CLKP / (2^6)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110</td>
<td>CLKP / (2^7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111</td>
<td>Clock disabled</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>Reserved</td>
<td>-</td>
<td>(Always\ set\ to\ \ '0')</td>
</tr>
<tr>
<td>8</td>
<td>MD1</td>
<td>Mode Bit</td>
<td>0</td>
<td>Setting prohibited</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Necessary for PFM operation</td>
</tr>
<tr>
<td>7-5</td>
<td>-</td>
<td>Reserved</td>
<td>-</td>
<td>(Always\ set\ to\ \ '010')</td>
</tr>
<tr>
<td>4</td>
<td>RELD</td>
<td>This bit enables reload operations.</td>
<td>0</td>
<td>The count operation stops when an underflow occurs due to underflow</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The counter operates in reload mode</td>
</tr>
<tr>
<td>3</td>
<td>INTE</td>
<td>Interrupt request enable bit</td>
<td>0</td>
<td>Interrupt request is generated when the UF bit changes to &quot;1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>no interrupt requests are generated</td>
</tr>
<tr>
<td>2</td>
<td>UF</td>
<td>Underflow flag</td>
<td>0</td>
<td>Read: No counter underflow Write: Clears the Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Read: Counter underflow occurred Write: No effect</td>
</tr>
<tr>
<td>1</td>
<td>CNTE</td>
<td>Counter count enable bit</td>
<td>0</td>
<td>stops count operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>sets the counter to wait for a trigger</td>
</tr>
<tr>
<td>0</td>
<td>TRG</td>
<td>Software trigger bit</td>
<td>0</td>
<td>Write: No effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Write: Software trigger applied</td>
</tr>
</tbody>
</table>

**Table 2-1: P0TMCSR and P1TMCSR**
2.2.2 16-bit Counter Register \((P0TMR, P1TMR)\)
Reading this register reads the count value of the 16-bit down counter. Its initial value is indeterminate. Always read this register using 16-bit data transfer instructions Output Compare Unit

2.2.3 16-bit Reload Register \((P0TMRLR, P1TMRLR)\)
The 16-bit reload register stores the initial count value. Its initial value is indeterminate. Always write to this register using 16-bit data transfer instructions.

2.2.4 Port function register \((PFRxx, EPFRxx)\)
To enable PFM output one should enable its corresponding port function register. Please refer data sheet of corresponding device for more information

2.3 PFM Counter Operation

2.3.1 Reload Counter Operation
This section describes the operations of the 16-bit reload counter

The Peripheral Clock (CLKP) divided by 2, 8, 32, 64 or 128 can be selected as the clock source when operating the counter from an internal clock. Writing "1" to both the \(CNTE\) and \(TRG\) bits in the control status register enables and starts counting simultaneously.

One clock cycle (CLKP divided by 2/8/32/64 or 128) is required from the counter start trigger

An underflow occurs when the counter value changes from 0000H to FFFFH. Therefore, an underflow occurs after "reload register setting + 1" counts. If the RELD bit in the control register is "1" when the underflow occurs, the contents of the reload register are loaded into the counter and counting continues. When RELD is "0", counting stops with the counter at FFFFH. The UF bit in the control register is set when the underflow occurs. If the INTE bit is "1" at this time, an interrupt request is generated.

![Figure 2-2 Counter activation and operation timing](image)
2.3.2 PFM Operation and Setting

This section describes the following operations of the 16-bit pulse frequency modulator (combining the functionality of both reload counters).

The underflow output of reload counter channel 0 is connected internally to the trigger input reload counter channel. The underflow output of reload counter channel 1 is connected internally to the trigger input of reload counter channel 0.

Both counters must be set up with RELD = “0”. Counter 0 should then be started by software trigger TRG = “1”. By starting counter 0 a high level is generated at the output. At the underflow condition of counter 0, counter 1 is automatically reloaded and started by the internal trigger (falling edge, set MOD1 = “1” for both counters) and a low level is generated at the output. At the underflow condition of counter 1, counter 0 is automatically reloaded and started by the internal trigger and a high level is generated at the output.

Interrupts can be set up on underflow condition of counter 0, counter 1 or both. The interrupts of counter 0 and counter 1 are combined together (logical OR).

The default output is low level if both CNTE = “0”, and both INV = “0”.
2.4 Calculation

If we need to generate a following waveform with $T_{High} = 20\text{ms}$ and $T_{Low} = 100\text{ms}$

We can calculate $T_{High}$ as,

$$T_{High} = (P0TMRLR + 1) \times \left( \frac{1}{\text{CLKP} / P0TMCSR: \text{CTS}} \right)$$

Let us assume CLKP is 16MHz and $P0TMCSR: \text{CTS}$ is B'010

Then,

$$T_{High} = (P0TMRLR + 1) \times \left( \frac{1}{16\text{MHz}/32} \right)$$

I.e. $P0TMRLR = \frac{20\text{ms}}{2\mu\text{s}} + 1 = 10001$

Similarly,

$$T_{Low} = (P1TMRLR + 1) \times \left( \frac{1}{\text{CLKP} / P1TMCSR: \text{CTS}} \right)$$

Let us assume $P1TMCSR: \text{CTS}$ is B'101

Then,

$$T_{Low} = (P0TMRLR + 1) \times \left( \frac{1}{16\text{MHz}/64} \right)$$

I.e. $P0TMRLR = \frac{100\text{ms}}{4\mu\text{s}} + 1 = 25001$
3 Software Example

EXAMPLE FOR PULSE FREQUENCY MODULATOR

3.1 Basic Functionality of the PFM

The following example shows how to set up the Pulse Frequency Modulator.

```c
void InitPFM(void)
{
    PFR16_D6 = 1;
    EPFR16_D6 = 1;
    P0TMRLR = 0x2711; //Reload Register
    P0TMCSR_INV = 0; //default level
    P0TMCSR_CSL = 2; //CLKP / 2^5
    P0TMCSR_MOD1 = 1; //PFM operation
    P0TMCSR_RELD = 0; //Count operation stops when an underflow occurs
    P0TMCSR_INTE = 1; //Interrupt enabled
    P0TMCSR_UF = 0; //Clear underflow flag
    P0TMCSR_CNTE = 1; //sets the counter to wait for a trigger

    P1TMRLR = 0x61A9; //Reload Register
    P1TMCSR_INV = 0; //default level
    P1TMCSR_CSL = 5; //CLKP / 2^6
    P1TMCSR_MOD1 = 1; //PFM operation
    P1TMCSR_RELD = 0; //Count operation stops when an underflow occurs
    P1TMCSR_INTE = 1; //Interrupt enabled
    P1TMCSR_UF = 0; //Clear underflow flag
    P1TMCSR_CNTE = 1; //sets the counter to wait for a trigger

    P0TMCSR_TRG = 1; //TRG applies a software trigger
}

__interrupt void PFMIRQHandler (void)
{
    if(P0TMCSR_UF == 0)
    {
        P0TMCSR_UF = 0;
    }
    else if(P1TMCSR_UF == 0)
    {
        P1TMCSR_UF = 0;
    }
    else
    {
        P1TMCSR_UF = 0;
        P0TMCSR_UF = 0;
    }
}
```
4 Additional Information

Information about FUJITSU Microcontrollers can be found on the following Internet page:
http://mcu.emea.fujitsu.com/

The software examples related to this application note is:
91460_PFM
It can be found on the following Internet page:
http://mcu.emea.fujitsu.com/mcu_product/mcu_all_software.htm
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