FR FAMILY
32-BIT MICROCONTROLLER
MB91F467S

MB91F467S EMULATION

APPLICATION NOTE
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008-02-06</td>
<td>1.0 MSt, first release</td>
</tr>
<tr>
<td>2008-03-05</td>
<td>1.1 MSt, Chapter 3.2.5 APIX® IP Register address (MODULEID) Bit0..7 description corrected</td>
</tr>
<tr>
<td>2008-03-28</td>
<td>1.2 OMG. Chapter 2.2: add. informations added</td>
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</tr>
</tbody>
</table>

This document contains 16 pages.
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1 Introduction

This application note describes the emulation system for MB91460S (MB91F467S) series. The current emulation system is based on EVA device MB91V460A, which does not include an APIX® interface. For that reason the APIX® interface is emulated by an FPGA. The FPGA is connected to the bus interface of MB91V460A.

Note:
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The following chapters describe any discrepancies between FPGA emulation system and MB91F467S standalone Flash microcontroller.
2 Hardware Setup

The chapter describes the setup of the Emulation system.

2.1 Required parts

To emulate the MB91F467S series, the following parts are required:

1. MB2198-01 Emulator Main Unit
2. MB2198-10: DSU4 cable
3. EMA-MB91V460A-002B/-80: Adapter board, including MB91V460A
4. EMA-MB91V460A-300: APIX® FPGA extension board
5. EMA-MB91F467S-LS-176M07: Socket adapter board (level shifter)
6. EMA-MB91F467S-NLS-176M07: Socket adapter board (No level shifter)
7. NQ-PACK176SD-ND: Socket for package FPT-176P-M07
   (Tokyo Eletech Corp. www.tetc.co.jp/e_tet.htm)

On the target system, a NQ-PACK176SD-ND socket is required enabling connection to the EMA-MB91F467S-LS-176M07 board.

2.2 Installation

The figure below shows the default system setup for APIX® receiver and transmitter connection during emulation.

![Figure 2-1: APIX® emulation system setup](image-url)
For detailed installation instruction see the user guides of the emulation tools.

- UG-910055-xx-EMA-MB91V460A-002.doc
- UG-910065-xx-EMA-MB91V460A-003.doc
- UG-910069-xx-EMA-MB91V460A-300.pdf

It is recommended to read the user guide for the EMA-MB91V460A-300 APIX® FPGA board to ensure correct settings for operation.

In addition there are several application notes for MB2198-01 emulator available, describing features and software installation (e.g. USB drivers).
3 Differences between MB91F467S and Emulation System

The chapter describes the differences between the emulation system and MB91F467S series.

3.1 Overview about differences

<table>
<thead>
<tr>
<th>Feature</th>
<th>Emulation system (MB91V460A + FPGA)</th>
<th>MB91F467S series</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum CPU Operating Frequency</td>
<td>MB91V460A: 80 MHz</td>
<td>100MHz</td>
</tr>
<tr>
<td>Must setting for ext. Bus Frequency</td>
<td>20MHz</td>
<td>user defined</td>
</tr>
<tr>
<td>Bus Interface pins</td>
<td>Bus interface function required</td>
<td>Bus Interface or GPIO function selectable</td>
</tr>
<tr>
<td>Ext. Bus Chip select for FPGA board</td>
<td>One chip select is required for EMA-MB91V460A-300 board</td>
<td>Not required</td>
</tr>
<tr>
<td></td>
<td>User defined: CS [0…7]</td>
<td></td>
</tr>
<tr>
<td>APIX® Register start address</td>
<td>0x0030.7200</td>
<td>0x00.7200</td>
</tr>
<tr>
<td>APIX® IP version Register address</td>
<td>0x0030.7320</td>
<td>0x00.7320</td>
</tr>
<tr>
<td>APIX® Interrupts</td>
<td>APIX® interrupts connected to external Interrupt 13 and 15</td>
<td>APIX® interrupts set in APIX® register</td>
</tr>
<tr>
<td></td>
<td>TRANSACTION BUFFER → INT13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EVENT BUFFER → INT15</td>
<td></td>
</tr>
<tr>
<td>Interrupt vector table (Intvect)</td>
<td>External Interrupt</td>
<td>Internal APIX® Interrupts</td>
</tr>
<tr>
<td>DMA</td>
<td>Setup via external bus DMA transfer request</td>
<td>Setup via internal register</td>
</tr>
<tr>
<td>Number of Transaction buffers</td>
<td>8 buffers</td>
<td>16 buffers</td>
</tr>
<tr>
<td>Available ASHELL</td>
<td>ASHELL 0</td>
<td>ASHELL 0 &amp; 1</td>
</tr>
<tr>
<td>APIX® Link speed</td>
<td>500Mbit/s</td>
<td>125Mbit/s</td>
</tr>
<tr>
<td>AIC pin selection</td>
<td>Selectable via jumper on emulation board</td>
<td>Selectable via PFR/EPFR register</td>
</tr>
</tbody>
</table>
Table 3-1: Overview of the differences between MB91F467S and emulation system

3.2 Details of differences

3.2.1 Maximum CPU operating frequency

The maximum operating frequency of the emulation device MB91V460A is 80MHz. Do not set higher PLL frequencies! The MB91F467S series has a maximum operating frequency of 100MHz.

Using the Emulator ensure that the PLL frequency do not exceed 80MHz. The PLL options can be set in the file start91460.asm (See Chapter 4.7.1 Clock Selection in start91460.asm file).

For further details refer to MB91460A series Hardware Manual and MB91F467S series Datasheet.

3.2.2 Must setting for ext. bus frequency

The frequency for external bus of the MB91V460A in emulation must be set to 20MHz!

Other settings may cause malfunction of FPGA and APIX® communication.

3.2.3 Bus Interface usage

Using Emulation system all available Bus interface pins are also used for APIX FPGA board. This ports shall not be set to GPIO functionality otherwise connection to APIX FPGA gets lost.

Using MB91F467S the pins can be assigned to Bus interface functionality or GPIO functionality.

3.2.3.1 FPGA Reset

Address line A23 is used in some FPGA bit streams. In case of using this bit stream do not use A23 in your Application. Otherwise APIX FPGA might be reset

Latest FPGA bit stream is using Port13_7 as Reset line. A23 can be used as Bus Interface pin.

<table>
<thead>
<tr>
<th>Reset pin</th>
<th>FPGA moduleid register value</th>
</tr>
</thead>
<tbody>
<tr>
<td>P05_7 (A23)</td>
<td>0x80270101, 0x80040201, 0x80070201, 0x80250201, 0x80110301, 0x80260301</td>
</tr>
<tr>
<td>P13_7</td>
<td>0x80180801</td>
</tr>
</tbody>
</table>

Table 3-2: FPGA Reset pin usage

The FPGA bit stream version can be read out via the moduleid register.

See chapter 3.2.6 for register address.
3.2.4 Ext. Bus Chip select for FPGA board

The APIX® FPGA extension board (EMA-MB91V460A-300) is connected to the external bus interface of the MB91V460A emulation chip. Thus it is required to enable one chip select line to access the FPGA via the external bus! The chip select can be freely selected by the user. The FPGA board has to be configured via DIP-SW on EMA-MB91V460A-300 board.

NOTE:
- The chip select which is enabled for FPGA usage,
  - can not be used for any RAM/ROM on target hardware anymore!
  - has to be configured on adapter board (EMA-MB91F467S-LS-176M07) as masked chip select additionally. Please read the user guide for the adapter board for details on how to configure masked chip select!

3.2.5 APIX® Register start address

The start address of the APIX® Register is different in Emulation tool and MB91F467S.

In MB91F467S the start address is 0x00007200

Using the Emulation system the register start address is in external Bus interface address range. The Offset address value is: 0x0030.7200

There exist two header files for the remote handler (remote_flash.h and remote_emu.h) which overcome the address offset. Select in remote.h file which system is used.

When using the Emulation system the used Chip select must be setup in start91460.asm to ensure access to the Remote Handler / APIX® Register.

3.2.6 APIX® IP Register address (MODULEID)

Within the Register set of the APIX interface there is one 32-bit register including the IP version.

For the MB91F467S this Register is at address: 0x00.7320
For the FPGA system it is at address: 0x30.7320

The MODULEID Register description is as following:

<table>
<thead>
<tr>
<th>Bit 31</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>NONFPGA version</td>
</tr>
<tr>
<td>1</td>
<td>FPGA version</td>
</tr>
</tbody>
</table>

Bit 30 – 24: reserved : read value is ‘0’
Bit 23 – 16: Date code: Day
Bit 15 – 08: Date code: Month
Bit 07 – 00: Revision
3.2.7 APIX® Interrupts

On MB91F467S two internal interrupts are available for the APIX® interface. On Emulation system these interrupts are available at external interrupts.

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>APIX® Event/ Fatal Error</th>
<th>APIX® Transaction Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB91F467S</td>
<td>No. 76 / ICR30</td>
<td>No. 80 / ICR32</td>
</tr>
<tr>
<td>Emulation system</td>
<td>No. 31 / ICR07</td>
<td>No. 29 / ICR06</td>
</tr>
</tbody>
</table>

Table 3-3: Interrupt assignment

3.2.8 DMA usage

At MB91F467S internal DMA transfer from APIX register can be used. Using the emulation system, the DMA transfer must setup using DMA via external Bus.

3.2.9 Number of Transaction buffer

The number of available transaction buffer is different in Emulation system and MB91460S. For the Emulation system (FPGA) 8 buffers (0-7) are available. They are assigned to Link 0. For the MB91460S series 16 Transaction buffers are available.

3.2.10 Available APIX® Link

In Emulation system ASHELL 0 is available. In MB91460S series ASHELL 0 and 1 are available. ASHELL 0 can be assigned to internal Physical layer (APIX® link) or Automotive Interconnection Link output. ASHELL 1 is assigned to Automotive Interconnection Link only.

3.2.11 APIX® Link speed

Emulation system APIX® Link speed is 500Mbit/s as external INAP APIX® Transceiver are used. The MB91F467S APIX® Link speed is 125MBit/s.

3.2.11.1 Payload data

MB91F467S: max. 2.79 MByte/s
Condition: Use Case: Downlink over Pixelchannel
CLKB = 100MHz, CKLP = 50 MHz,
Data transfer from internal Flash to transaction buffer using DMA
Emulation system: max. 150 kByte/s
Condition: Use Case: Communication over Automotive Interconnect to external AShell (1Bit Datawidth)
CLKB = 60MHz, CLKP=10MHz, CLKB = 20MHz
Data transfer from internal Flash to transaction buffer using DMA

3.2.12 AIC pin selection

In case of AIC link (Automotive InterConnection) usage the dedicated pins needs to be configured.

For Emulation system the selection if using GPIO or AIC function is done via jumper on emulation board. See corresponding documentation.

Note: Emulation system supports only ASHELL 0!
Using MB91F467S selection is possible via PFR and EPFR register setting.
4 MB91F467S template Project

The chapter describes the template project of MB91F467S series.

Fujitsu Microelectronics Europe GmbH is offering a template project for MB91F467S series. It includes some basic settings for e.g. APIX®, Linker, C-Compiler which must be checked and modified in detail, corresponding to the user application.

4.1 Template file structure

The template project comes with following files:

- Start91460.asm
- Vectors.c / .h
- Mb91467s.h / .asm
- Remote.h / .asm
- Remote_flash.h
- Remote_mcu.h
- Main.c
- Fpga.c / .h

4.1.1 Start91460.asm

The Start91460.asm file is sued to initialise the MCU. Settings like stack size, Clock speed and Bus interface can be set in this file.

When using the Emulation system ensure that the Chip select for the APIX® FPGA board (DIP switch on EMA-MB91V460A-300) is set to “ON” and all configuration register are set accordingly.

4.1.2 Vectors.c / .h

This file contains the Interrupt vector table. In addition the Interrupt level can be set via the ICRxx register.

Be aware of the different interrupt vectors of MB91F467S and Emulation system for the Remote handler / APIX®.

4.1.3 Mb91467s.h / .asm

This file defines the I/O register of MB91F467S series. The Remote Handler / APIX® register are defined in a separate file.

4.1.4 Remote.h / .asm

The Emulation system and MB91F467S have different addresses for Remote Handler / APIX® register. Select in this file which target system (STANDALONE or EMULATION) is used. Depending on this selection a header file is included with offset address for that target system.
4.1.5 Remote_flash.h
This file contains the register definition and addresses of Remote Handler / APIX® register for Mb91F467S. (start address: 0x00007200)

4.1.6 Remote_emu.h
This file contains the register definition and addresses of Remote Handler / APIX® register for Emulation system. (start address 0x00307200)

4.1.7 Fpga.c / .h
The Emulation system has to set some respective reset settings during startup. This files hold the required rest and initialization routines for the fpga.

The following function call has to be inserted into the project main and has to be called after initialization of the external bus interface:

Fpga_Init();
5 Appendix

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5.3 Related Documentation

5.3.1 Application Notes:
- INSTALLATION GUIDE MB2198-01
  mcu-an-391026-e-vxx-mb2198_install.pdf
- GETTING STARTED:
  mcu-an-391027-e-vxx-mb2198_getting_started.pdf
- EMULATING AND DEBUGGING WITH SOFTUNE AND MB2198-01:
  mcu-an-391028-e-xx-mb2198_emulation.pdf
- GETTING STARTED:
  mcu-an-300005-e-vxx-mb91v460_getting_started.pdf
- Start91460
  mcu-an-300021-e-vxx-start91460.pdf

5.3.2 Documentation:
- MB91460A series Hardware Manual
- MB91F467S series Datasheet
- EMA-MB91V460A-00x User Guide
- EMA-MB91V460A-300 (APIX® extension board) User Guide
- EMA-MB91F467S-LS-176M07 (socket adapter board) User Guide

-- END --