Fujitsu System Applications Support
Overview – System Applications Support

- SOC Application Development Lab
- Multimedia – VoIP
- Wireless – Bluetooth
- Processors, DSP and Peripherals – ARM Reference Platform
Fujitsu provides:

- System-level evaluation and emulation systems
- A platform for system development
- A real system environment for H/W and S/W verification
- Vehicles for demonstration of functionality
VoIP Core Brief

- **Applications**
  - Residential gateway, IP phone, cable modem, CT, wireless

- **Key Features**
  - Designed for implementing speech vocoders to support VoIP applications for CPE
  - Supports four simultaneous and independent voice channels
    - G.168 echo cancellation
    - Vocoders: G.711, G.726, G.728, G.729A, G.729E
    - DTMF decode and DTMF encode
    - Jitter buffering
  - ARC-3 DSP core with co-processor provides efficient & flexible soft solution
  - Bus master interface with built-in DMA for accessing host and system memory
  - Shared system memory eliminates need for a dedicated memory
  - Audio CODEC interface (SPORT) with AC’97 compliant audio CODEC interface
  - Test chip available in 0.25µm technology
  - Complete reference design supports residential gateway application
VoIP Software Architecture

GATEWAY APPLICATION

VoIP API

MGCP

RTP

JITTER BUFFER

VoIP Chip Device Driver

UDP

IP

ETHERNET Device Driver

BUFFER MANAGER

SCHEDULER

VOCODERs (G.’s)

SPORT Driver

VoIP TEST CHIP

HOST ARC

RTOS KERNEL

VoIP Chip Device

Driver

SPORT Driver

VOIP TEST CHIP

IP NETWORK

PCM

VoIP API

MGCP

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VOCODERs (G.’s)

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VoIP TEST CHIP

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VoIP Chip Device

Driver

SPORT Driver

VOIP TEST CHIP

IP NETWORK

PCM
VoIP Evaluation System – Home Gateway

VoIP Evaluation System

- Power Input
- Debug
- AFE
- FPGA
  - ARC-3
  - Arbiter
  - Memory Sequencer
- SDRAM
- FLASH
- Ethernet
- RS232C

IP NETWORK

HOST

PC Interface

4-Channel Voice

4-Channel Voice
Bluetooth Software Architecture

Bluetooth Host Controller
- Host Drivers and Applications
  - Middle-Ware
  - IrMC
  - Middle-Ware
  - OBEX
  - Middle-Ware
- SDP
- RFCOMM
- TCP/UDP
- IP
- PPP
- L2CAP
- HCI-Upper

Transport Bus
- HCI-Lower
- Link Manager Protocol
- Bluetooth Link Controller

Embedded System
- Host Drivers and Applications
  - Middle-Ware
  - IrMC
  - Middle-Ware
  - OBEX
  - Middle-Ware
- SDP
- RFCOMM
- TCP/UDP
- IP
- PPP
- L2CAP
- HCI-Lower
- Link Manager Protocol
- Bluetooth Link Controller

Bluetooth Radio
Pistachio

• Mainly designed for enabling the ASIC/ASSP designer to design ARM core blocks efficiently for fast time to market
• Flexible RTL source codes are integrated in order to meet custom design requirements
• Based on single-chip microcontroller “ARMONDE”
• Peripheral modules have already been evaluated in ARMONDE
• Verification program for the ARMONDE chip can be run on the PISTACHIO design without any changes
• ARMONDE: a header board mounted on the “Nuts Farm” board for evaluation of the ARM core and micro functions.
• Nuts Farm: a general-purpose evaluation board to evaluate the functions of the ARM core and micros, including ARM7TDMI core (ARMONDE)
Fujitsu ARM Reference Platform

Pistachio Block Diagram

- ARM7TDMI + Cache
- Arbiter
- External Bus I/F
- Default Slave
- Dummy Master

- AHB-APB Bridge
- Decoder
- DMAC 8ch
- Internal Memory
- Dummy Slave

- IRC
- External IRC 4ch
- 16-bit Timer 2ch
- Config. Register
- Clock Control

AHB

APB
Fujitsu ARM Reference Platform

ARMONDE Test Chip

- **TAP cont**
  - ARM7TDMI

- **ICE I/F**
  - Unified 16KB
  - Cache Controller
  - AHB repeater

- **Arbiter**
  - Decoder

- **AHB Wrapper**

- **AHB (ARM High speed Bus)**
  - AHB-APB bridge
  - Interrupt Control
  - Remap
  - Clock Control
  - AHB-APBW Bridge

- **APB (Advanced Peripheral Bus)**
  - Timer
  - UART

- **128KB SRAM**

- **External Bus I/F**

- **DMAC 8ch**

- **AHB (ARM High speed Bus)**

- **APBW**

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Nuts Farm Option

ACT725 ARM7TDMI Test chip

FPGA A

ARM dummy + Cache

Arbiter

External Bus I/F

Default Slave

AHB Repeater

AHB-APB Bridge

Decoder

DMAC dummy

Internal Memory

FPGA B

Repeater I/F

DMAC 2ch

AHB-APB Bridge

Decoder

UART 2ch

Config. Register

IRC

External IRC 4ch

16-bit Timer 2ch

Config. Register

Clock Control

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The possibilities are infinite