High-Performance ASIC Solutions for the Metro & Long Haul Markets

“Growth through Innovation”
Overview – High-end ASICs

• Business Strategy
• Target Markets
• Products
  • Process Technology
  • Packaging Roadmap
  • High-Speed I/O Offerings
  • Current Advanced ASICs
• Case Study
Fujitsu Limited Business Strategy

Value Chain

Platforms

Service (Products)

Technologies (Electronic Devices)

Integration

Customers

Fujitsu Microelectronics America, Inc.

July 2002
Target Markets – High-end ASICs

Metropolitan Area Network

High-end Access

Long Haul
The Fujitsu Advantage – High-end ASICs

• **Technology**
  • Robust process technologies like 0.09µm, 0.11µm and 0.18µm to support high-end ASICs
  • Wide array of high-performance packages like 2116 FCBGA or 892 EBGA
  • Key high-speed I/O macros in the range of 2.5Gbps-10Gbps (CMOS)

• **Manufacturing**
  • Cutting-edge wafer-fabrication facilities (200mm) all done in house in Japan
  • Modern facilities (also in house) for assembly and testing for high-performance Flip-Chip packaging
  • Quick turn-around time available to meet customers’ time-to-market needs
  • Special services like burn-in, load boards, test boards also available
The Fujitsu Advantage (Cont’d)

• **Sales/Services**
  - Strong sales force with six U.S.-based sales offices from coast to coast
  - Fully staffed U.S. design centers in California, Texas and North Carolina
  - Key support for ASICs via Customer Response Centers

• **Employees**
  - Unsurpassed experience in supporting key ASIC designs
  - Rich engineering skill-sets to execute complex, next-generation ASIC designs
  - Multi-disciplined teams providing class “A” support
Why Fujitsu?

Leading-edge Process & Packaging Technology
- 0.11µm & 0.18µm processes
- High-speed FCBGA with >2000 pins
- 256Mb FCRAM interface & other high-speed SRAM
- 250-300MHz clock frequency

High-speed I/Os as per OIF Standards
- 2.5Gbps-3.125Gbps
- SPI-4 & SPI-5 interfaces
- SFI-4 & SFI-5 interfaces
- HSTL & SSTL I/Os

Robust Design & Manufacturing Capabilities
- Timing-driven hierarchical design methodology
- Multiple design center locations
- In-house wafer, assembly and test operations

Build a high performance ASIC with leading-edge technology
Ensure interoperability as per industry standards
Obtain a successful working ASIC first time around
ASIC Product Road Map

- **R & D**: CE200/CS200 (1.0V)
- **Development**: CE100/CS100 (1.2V)
- **Introduced**: CE91/CS91 (1.2V)
- **Volume Production**: CE81/CS81 (1.8V)
- **Volume Production**: CE77 (2.5V)
- **Volume Production**: CE71/CS71 (2.5V)

Gates

- 0.09µm
- 0.11µm
- 0.18µm
- 0.25µm

- 10K
- 100K
- 1M
- 10M
- 100M
90nm-node Technology Features

- 40, 65, 85nm Gate Length with Advanced ArF Lithography
- Advanced Multilevel Interconnect with Cu Dual Damascene and Low k dielectric (Effective k = 3.0)
- High-performance Tr (Low Leakage, High Speed, Low Voltage)
- Mixed Signal, RF and I/O Options
- Small SRAM Cell Size = 1.27um²
90nm-node Interconnect Technology

Cu Dual Damascene (9 Cu Layer + 1 Al Layer)
Full Low k Material

Fujitsu Microelectronics America, Inc.
ASIC High Pin-Count Packages
Fujitsu holds the number-one position in package technology

Leadership position enables Fujitsu to define packaging trends

Fujitsu’s packages are found in many high-end ASICs & FPGA solutions

Current
- Pin count (~2116)
- On board C1k 3.2Gbps

Future
- Various process die on the package

2003-2004
- Pin count (~3000)
- On board C1k 10Gbps

- Substrate with integrated passive (LCR)
- Low-K substrate

- Low-K substrate
High-Speed Interface CMOS Macros

Data Rate per channel (Gbps)

- 622Mbps
- 2.5Gbps
- 5.0Gbps
- 10.0Gbps
- 20.0Gbps
- 40.0Gbps

- 0.25µm (CS70, 1997-99)
- 0.18µm (CS80A, 2000-01)
- 0.13µm (0.11) (CS90A, 2002-03)
- 0.09µm (0.09) (CS100A, 2003-04)

Technology Node (TN) and Gate Length (LG)

- 0.25µm
- 0.18µm
- 0.13µm (0.11)
- 0.09µm (0.09)

*TN: technology node  
LG: gate length on Si

40G Async
10-12.8G Async
5-6.4G Async
3.125G XAUI (10G Ethernet)
2.5-3.125G OIF (SFI-5, SPI-5)
2.5-3.125G Async with 622M/1.25G mode
622-780M OIF (SFI-4, SPI-4p2)

Fujitsu Microelectronics America, Inc.
Current Advanced ASICs

• Large-scale integration
  >12M gates
• High-speed performance core
  >250MHz
• Large pin-count package
  >2000 pins
Success Story – Foundry Networks, Inc.

- Complex, high-density, high-speed ASIC designs for network applications
- 5 months from project kick-off to delivery of all prototypes
- Keys to success
  - Advanced process and packaging technologies
  - Advanced design methodology for critical timing closure
  - Strong design support
  - Quick fabrication of prototype