System Prototyping Kit with Android™/Linux®/μITRON MB8AC0300EVA

The main chip equipped with high-function IPs that is essential to the recent LSI development in addition to the ARM® Cortex™-A/R/M Series CPU core has been embedded on the board along with various high-speed interfaces and a touch panel. Equipped with full performance, functions, expandability, and operability, it is the third-generation prototyping kit and it can be utilized more widely than conventional products.

Overview

As our proprietary ASIC development environment, the System Prototyping Kit enables our customers who adopt LSIs with built-in ARM CPU cores to achieve excellent time to market. It has been very well received, especially because it enables software development before completion of the actual LSI chip.

This product, which is the third generation of the Series, can be used in the development of high-function LSIs and system applications thanks to the various embedded high-speed interfaces and high-function IPs, in addition to the latest Cortex Series CPU core.

Figure 1 depicts the transitions in our provision of evaluation boards, and Figure 2 the evaluation board.

Product Features and Applications

This product has been developed for the following applications:

- **Advance evaluation of the CPU/IP**
  Tests on the performance evaluation of CPUs including multi-
core CPUs, evaluation of various IP functions, connectivity checks, and so forth, which are extremely important to determine the actual operation, can be conducted in advance.

- CPU selection evaluation
  - Cortex-A9MPCore/R4F/M3
- IP function/connectivity evaluation (high-speed I/F)
  - USB 3.0/USB 2.0/PCIe Gen2/SATA2
  - GbE/NoE/SDXC
- Third-party IP evaluation
  - GPU/DDR controller

**Prototype development**

It is also possible to evaluate the development and connection of customer circuits (LSI prototyping) through system expansion utilizing PCI Express.

**Figure 3** presents the evaluation board configuration for this product.

The two PCI Express systems support the Root Complex/Endpoint. Connection can be selected to suit the application environment or the existing assets of the customer. An optional board with built-in FPGA on which customer circuits can be embedded is also currently being prepared for release.

**Software development in advance**

A Board Support Package (BSP) for this product that supports Android/Linux/μITRON (μT-Kernel) is being prepared.

- OS/driver development
  - Application development
  - Demonstration software provision

**Hardware Specifications**

**Main chip specifications**

**Table 1** presents the list of embedded function IPs on the main chip “MB8AC0300.”

**CPU**

This product has the built-in CPU core of the future mainstream ARM Cortex Series, including a Cortex-A9MPCore that enables multimedia applications, Cortex-R4F that achieves high-reliability real-time operation, and Cortex-M3 for 32-bit microcontrollers. It enables both selection of the proper CPU and various developments suited to the intended application or load.
High-speed interface
This product has various built-in IPs, including USB 3.0/USB 2.0/SATA2/PCIe Gen2/GbE. It can be used for embedded trials, interoperability tests, and actual performance evaluations with various applications from digital home systems to industrial applications.

Broadband memory and bus architecture
This product adopts a DDR3 memory to ensure the performance of the high-performance CPU and high-speed IPs as well as the basic platform composed of the high-efficiency bus architecture that only FUJITSU can provide. It can also be used as the reference design for LSI development.

Media/security functions
This GPU supports OpenGL ES2.0/1.1 and OpenVG 1.1 and LCD controllers for image processing. Tests on media-processing functions in combination with a touch panel interface are possible. As communication and security functions, this product has a built-in Network Offload Engine (NoE) that supports GbE, and can be used in various types of evaluations.

Board configuration
The board is configured with consideration given to the basics so that the main chip performance and functions can be utilized effectively. The pursuit of simplicity and the usefulness of debugging were considered in its development.

It is equipped with all interfaces related to embedded functions (touch panel + LCD, DVI-IF, voice input/output, various switches, JTAG, and CPU debugging interface).

Prototyping

Hardware
With the assumption of utilization as the base platform for ASIC development, it can provide master and subsystem operation by utilizing the Root Complex/Endpoint of the PCI Express that is embedded in this product.

Embedding in various systems is simplified and the utilization and high-performance development of the existing assets can be addressed.

Figure 4 presents the evaluation board interface.

This board controls the FPGA board with a PCI Express connection during master operation. It operates by receiving commands from the host system via PCI Express during T

Table 1 List of Embedded IPs on Main Chip

<table>
<thead>
<tr>
<th>Category</th>
<th>IP</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>Cortex-A9 MPcore</td>
<td>2 cores, 500 MHz, L1 cache I/D=32Kbytes/32Kbytes, L2 cache=512Kbytes, ACP-DMA</td>
</tr>
<tr>
<td></td>
<td>Cortex-R4F</td>
<td>250MHz, L1 cache=16Kbytes/16Kbytes, TCM_A=64Kbytes, TCM_B0=32Kbytes, TCM_B1=32Kbytes</td>
</tr>
<tr>
<td></td>
<td>Cortex-M3</td>
<td>125 MHz</td>
</tr>
<tr>
<td></td>
<td>GPU</td>
<td>OpenGL ES1.1 /OpenGL ES2.0 /OpenVG1.1, LCD controller (2 channels)</td>
</tr>
<tr>
<td>Interface macro</td>
<td>PCI Express Gen2</td>
<td>PCI Express Gen2, Root/Endpoint, 4 lanes (2 channels/SoC IF + FPGA extension)</td>
</tr>
<tr>
<td></td>
<td>Serial ATA Host Gen2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>USB</td>
<td>USB 3.0 Function, USB 2.0 Host/Function</td>
</tr>
<tr>
<td></td>
<td>SD</td>
<td>SDIO, SDXC (UHS-1) supported</td>
</tr>
<tr>
<td></td>
<td>NoE</td>
<td>IPsec Network Offload engine with 1000/100 BASE GMAC (700Mbps half duplex IPsec) × 2 channels</td>
</tr>
<tr>
<td></td>
<td>GbE</td>
<td>Ethernet MAC 1000/100 BASE-T, 802.3az (LPI), GMII, IEEE1588</td>
</tr>
<tr>
<td></td>
<td>Touch panel I/F</td>
<td>Touch panel interface (multi detection)</td>
</tr>
<tr>
<td>Memory I/F</td>
<td>DDR controller</td>
<td>DDR3-600 Mbps 32-bit</td>
</tr>
<tr>
<td></td>
<td>MEMCIS</td>
<td>Flash memory/SRAM controller</td>
</tr>
<tr>
<td></td>
<td>SPI</td>
<td>Quad serial Flash memory controller</td>
</tr>
</tbody>
</table>
It also enables LSI prototyping equivalent to an actual device by connecting a USB 3.0/SATA2 or similar device. This product delivers ASIC development with fewer risks than the conventional systems.

### Software

We provide a Board Support Package (BSP) for this product. It can be utilized as the basic package for application programs to be installed in the LSIs to be developed. Software packages supporting Android, Linux, and μITRON (μ T-Kernel) that are optimal for the subject CPU cores are being prepared for release.

**Table 2** presents the list of software packages, and **Figure 5** the software package configuration.

Since the drivers for the IPs to be embedded on the main chip are included, the work required as part of conventional LSI development to prepare the development environment and software platform can be minimized. Our customers can commence application development immediately.

<table>
<thead>
<tr>
<th>Name of BSP</th>
<th>Applicable Cortex</th>
<th>Platform</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A9 SMP Linux BSP</td>
<td>Cortex-A9 MP Core (2 cores)</td>
<td>SMP Linux</td>
<td>BSP for developers of Linux applications that operate on Cortex-A9. For Linux application development. A Linux driver for a high-speed I/F macro is also included.</td>
</tr>
<tr>
<td>A9 Android BSP</td>
<td>Cortex-A9 MP Core (2 cores)</td>
<td>Android</td>
<td>BSP for developers of Android applications that operate on Cortex-A9. For Linux/Android application development. A Linux driver for a high-speed I/F macro is also included.</td>
</tr>
<tr>
<td>R4F μT-Kernel BSP</td>
<td>Cortex-R4F</td>
<td>μT-Kernel</td>
<td>BSP for developers of μT-Kernel applications that operate on Cortex-R4F. For μITRON application development.</td>
</tr>
<tr>
<td>M3 μT-Kernel BSP</td>
<td>Cortex-M3</td>
<td>μT-Kernel</td>
<td>BSP for developers of μT-Kernel applications that operate on Cortex-M3. For μITRON application development.</td>
</tr>
</tbody>
</table>

**Figure 5** Software Package Configuration

- **Cortex-A9 Linux (SMP) BSP**
  - Target ARM core: Cortex-A9 MP Core (2 cores)
  - OS: SMP-Linux Ver.2.6.32
  - Driver: USB2.0 Host/Func, USB3.0 Func, GbE, SPI/I²C, I²S

- **Cortex-R4F / M3 μT-Kernel BSP**
  - Target ARM core: Cortex-R4F / Cortex-M3
  - OS: μT-Kernel
  - Driver: SPI/I²C, I²S

- **Cortex-A9 Android BSP**
  - Target ARM core: Cortex-A9 MP Core (2 cores)
  - Library & application: Android Runtime, WebKit etc., Application Framework
  - OS: SMP-Linux Ver.2.6.32
  - Driver: USB2.0 Host/Func, USB3.0 Func, GbE, SPI/I²C, I²S
In addition to the built-in LCD/touch panel API on this product, acceleration of SSL secure communication by hardware, a function to store files in USB memories, and so forth have been addressed. These functions will eventually be included in the software package.

Software Development in Advance

To support the development of software programs that are closer to applications besides BSP, this product includes the following demonstration software programs that focus on specific systems (Figure 6):

- Built-in browser demonstration software
- Android demonstration software
- Handwritten signature verification/voice synthesis demonstration software → Built-in FUJITSU Inspirium™
- Multi-OS demonstration software → Simultaneous operation of Linux and ITRON-type OS

By utilizing these demonstration software programs, users can begin application development immediately. We plan to successively expand both the types of demonstration software programs and those included in the product and offer them to our customers. We also offer an electronic system level (ESL, a virtual environment) to enable advance development as an environment to support software development. With its flexibility, ESL not only realizes the advance development of software programs that is optimized for customer applications, but also enables architecture optimization.

Future Developments

The high-performance and high-function development of hardware continues to advance in recent LSIs. So, the requirement for developing software to fully utilize those fruits is also extremely growing.

Figure 7 presents the roadmap for ARM cores.

In the future, FUJITSU will continue to support the leading-edge ARM technologies with software-driven design services, including the system prototyping introduced in this article and Cedar™-ESL and will also expand their functions. In this way, we will realize the optimal functions and performance of our customer applications in a good time-to-market manner.

NOTES
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