256M-bit Consumer FCRAM™
64-bit I/O, Low-Power DDR SDRAM Interface, enabling SiP Solutions
MB81EDS256545

This FCRAM is a low-power consumption memory for digital consumer electronics. The new FCRAM features a 64-bit I/O and a low-power DDR SDRAM interface, enabling maximum data transfer capabilities of 3.46Gbytes/s, while consuming minimum power.

Introduction

The new 256M-bit Consumer FCRAM (Fast Cycle RAM), the MB81EDS256545, is designed for digital consumer electronics. The new FCRAM runs on low power consumption and is optimal for system-in-package (SiP) designs. Since it is possible to replace multiple DDR SDRAM devices with one new FCRAM, this memory is ideal for digital television and camcorder that require multiple DDR SDRAMs with video-processing engine. The FCRAM enables SiP solutions featuring ideal product performance and cost.

Benefit of New FCRAM

The new FCRAM uses a wide 64-bit I/O, so wider data bus realizes high data bandwidth at a lower operating frequency without termination resistors. MB81EDS256545 achieves lower power consumption than conventional DRAMs.

The low power consumption helps reduce the thermal management risk and cost that become most significant issue. In addition, low power feature reduces the emission of carbon dioxide (CO2), helping customers develop environment-friendly consumer electronics.
Background of Development

In recent years, digital consumer electronics have become multifunctional, requiring diverse semiconductor devices to be mounted in small packages on the printed circuit boards. This complexity increases design risk, complicates development, and increases the costs of both development and components.

In addition to the above concerns, for example, digital television has the thermal management risk because of heat generation occurred by high-speed operating components.

While digital still camera and camcorder have the other concerns. The product design is restricted by the PCB space and number of components.

To resolve these issues, FUJITSU developed the new 256M-bit Consumer FCRAM optimized for SiP. Figure 1 shows the requirements for the development of digital consumer electronics.

Issues of Digital Consumer Electronics Development
- Costs increase because diverse components are used for multiple functionalities.
- Costs increase because extra parts, such as the heat spreader and heat sink, are used for heat radiation.
- Development increases to optimize the complicated PCB design and countermeasures against heat generation.

Requirements for the Electronic Components and the Expected Effect
- Components featuring integrated multiple functionalities
  - Reducing the number of components, the amount of design required, and overall costs
- Components with low power consumption
  - Environment-friendly, power-efficient products with simplified design for heat radiation, reducing CO₂ emission

Applications

MB81EDS256545 is ideal for digital consumer electronics such as digital televisions and camcorders that require low power consumption. Figure 2 shows suitable applications for MB81EDS256545.

Features

The new 256M-bit FCRAM features a 64-bit I/O, low-power DDR SDRAM interface, enabling maximum data transfer capabilities of 3.46Gbytes/s while keeping power consumption low.

![Figure 1 Requirements for Development of Digital Consumer Electronics](image1)

![Figure 2 Suitable Applications for MB81EDS256545](image2)

<table>
<thead>
<tr>
<th>Digital Consumer Electronics</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Digital Television</td>
</tr>
<tr>
<td>- Digital Still Camera</td>
</tr>
<tr>
<td>- Camcorder</td>
</tr>
<tr>
<td>- Set Top Box</td>
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<tr>
<td>- Portable Media Player (PMP)</td>
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</tbody>
</table>

Table 1 Feature Comparison between Competitive RAM and New FCRAM

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>DDR2</th>
<th>DDR1</th>
<th>LPDDR</th>
<th>256M-bit FCRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus I/O</td>
<td>x16</td>
<td>x32</td>
<td>x32</td>
<td>x64</td>
</tr>
<tr>
<td>VDD/VDDQ</td>
<td>1.8V</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1.8V</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>400MHz (800Mbps)</td>
<td>200MHz (400Mbps)</td>
<td>166MHz (333Mbps)</td>
<td>216MHz (432Mbps)</td>
<td></td>
</tr>
<tr>
<td>Data Transfer Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.6Gbytes/s</td>
<td>1.6Gbytes/s</td>
<td>1.3Gbytes/s</td>
<td>3.46Gbytes/s</td>
<td></td>
</tr>
<tr>
<td>DLL on RAM</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Interface</td>
<td>SSTL</td>
<td>CMOS</td>
<td>CMOS</td>
<td></td>
</tr>
<tr>
<td>Resistors</td>
<td>ODT</td>
<td>Damping Resistors</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
Low. This product is designed to be integrated with logic chips into a SiP, which provides design and cost benefits. In addition to being offered in a wafer form for SiP integration, the FCRAM is also available as a wafer level package (WLP).

**Low Power Consumption**

DDR2 SDRAM and other high-speed memories require termination resistors (on-board or ODT: On Die Termination) to maintain stable signal quality. However, termination resistors consume a lot of power. The new FCRAM uses a wide 64-bit I/O, so wider data bus realize high data bandwidth at a lower operating frequency without termination resistors.

One new FCRAM enables data transfer capabilities equivalent to two DDR2 SDRAMs with 16-bit I/O, while reducing power consumption up to about 1W (approximately 70%) compared to DDR2 SDRAMs.

Figure 3 compares the power consumption of a DDR2 SDRAM and the new FCRAM.

**High-Speed Data Transfer Rate**

With a 64-bit I/O and operating frequencies up to 216MHz, this FCRAM provides maximum data transfer rate of 3.46 Gbytes/s, twice that of the typical DDR2 SDRAM with a 16-bit I/O and 400MHz operating frequency.

Table 1 shows the feature comparison between a competitive RAM and the new FCRAM. The table shows how the new FCRAM enables data transfer capabilities equivalent to two units of low-power DDR, DDR1 or DDR2 SDRAM.

**Memory Designed for SiP**

This product is ideal for SiP because the pad assignment has been optimized for the chip stack and the CMOS interface design lowers power consumption. SiP

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**Table 2** Factor Comparison between DDR SDRAM on board and FCRAM in SiP

<table>
<thead>
<tr>
<th>Factor</th>
<th>Conv. DDRs on Board</th>
<th>x64 FCRAM SiP</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Cost</td>
<td>NG (High)</td>
<td>Multiple Memories</td>
</tr>
<tr>
<td>PCB Cost</td>
<td>NG (High)</td>
<td>• Termination Resistors</td>
</tr>
<tr>
<td>PCB Design Risk</td>
<td>NG (High)</td>
<td>• Yield loss by EMI &amp; SI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Development Delay</td>
</tr>
</tbody>
</table>
helps conserve mounting space on the printed circuit board, reducing costs for components and the board material itself. Figure 4 shows the benefits of using the new FCRAM with SiP, and Table 2 shows factor comparison between DDR SDRAMs on board and FCRAM in SiP.

**Main Specifications**

The following are the key specifications of MB81EDS256545.

- Organization: 1M-word \(\times\) 64-bit \(\times\) 4-bank
- Interface: JEDEC standard Low Power DDR
- Power Supply Voltage: 1.7V to 1.95V
- Junction Temperature: \(-10^\circ\text{C}\) to \(+105^\circ\text{C}\)
- Burst Operating Frequency: 216MHz (Max.)
- Data Transfer Rate: 3.46Gbytes/s (Max.)
- Clock Access Time: 4.6ns (Min.)
- Operating Current (Burst Read): 300mA (Max.)

**Special Functions**

MB81EDS256545 has some special functions to improve memory access efficiency.

- **Multi-Bank Active**
  
  The Multi-Bank Active function enables the FCRAM to simultaneously activate two banks by issuing a Multi-Bank Activate (MACT) command. The MACT command is more efficient than the ACT command issued to access each bank, therefore MACT contribute to resolve potential issue of the lack of command bandwidths.

- **Background Refresh**
  
  Background refresh allows the FCRAM to execute internal refresh operation for one bank group and read/write operation to the other bank group simultaneously. One background refresh command (BREF) controls the start or stop of the internal refresh operation to selected bank group during the selected refresh cycles. Although refresh operation and read/write operation must be performed exclusively, the background refresh command help to avoid confliction between refresh and read/write operation resulting in the smooth refresh arbitration.

- **Start Address Shift**
  
  The Start Address Shift (SAS) function is used with the read or write operation. When the SAS function is enabled, the start address of 64-bit (8-byte) data can be shifted to the arbitral 8-bit (1-byte), decreasing unnecessary access.

- **Additional RDQS Toggle**
  
  The additional RDQS Toggle (ART) is to set the RDQS toggle count after the last pair of data output.
  
  In case of JEDEC standard DDR spec, the strobe signal toggling terminates the same time as the data output, while the RDQS toggle can be added after the last data output by the mode register. This function can extend the timing margin of switching the data from DQS domain to the internal clock domain in the SoC when the SoC latches output data from the memory (FCRAM). ART function possibly simplifies SoC PHY design. Figure 5 shows the additional RDQS toggle timing.

**Technical Support**

FUJITSU offers technical support tools such as simulation models for memory verification, memory controller for interface
support running, and the optional FPGA evaluation board, to help customers’ product developments.

FUJITSU has various simulation models such as the IBIS model, the Verilog model, the SOMA model (supported by Denali Software, Inc.) and the Bus Function Model (BFM) for Emulator. The optional FPGA evaluation board can be used to verify if the existing memory controller resource can be effective for the new FCRAM at the SoC development stage. The board can be easily connected to the existing FPGA prototype evaluation board (platform) so customers can easily introduce the FCRAM trial environment. Figure 6 shows an example of the configuration of the optional FPGA evaluation board.

**Figure 6** shows an example of the configuration of the optional FPGA evaluation board.

**Table 3** 256M-bit Consumer FCRAM Product Family

<table>
<thead>
<tr>
<th>Density (bit)</th>
<th>Interface</th>
<th>I/O (bit)</th>
<th>Supply Voltage (V)</th>
<th>Operating Frequency (MHz)</th>
<th>Junction Temp. Tj (°C)</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>256M SDR</td>
<td>x32</td>
<td>1.7 to 1.95</td>
<td>166</td>
<td>-10 to +105</td>
<td></td>
<td>MB81ES253245</td>
</tr>
<tr>
<td></td>
<td>x64</td>
<td>1.7 to 1.95</td>
<td>166</td>
<td>-10 to +105</td>
<td></td>
<td>MB81ES256445</td>
</tr>
<tr>
<td>DDR</td>
<td>x32</td>
<td>1.7 to 1.95</td>
<td>216</td>
<td>-10 to +105</td>
<td></td>
<td>MB81ES253245</td>
</tr>
<tr>
<td></td>
<td>x64</td>
<td>1.7 to 1.95</td>
<td>216</td>
<td>-10 to +105</td>
<td></td>
<td>MB81ES256445</td>
</tr>
</tbody>
</table>

* with special function