Low Power Consumption
H.264 Format Codec LSI Supporting HD Video
MB86H50

Appropriate for applications in digital AV devices and network transmission systems that compress and decompress high-definition (HD) video in real time.

Overview

As high-definition (HD) video media are becoming increasingly popular, digital AV devices including digital TVs and next-generation game machines are required to deliver functions to record, play, and transmit the HD video. To address such demands, FUJITSU has developed the LSI “MB86H50” that supports the H.264 high profile format video codec. This product has higher compression performance compared to the conventional MEPG-2 format. It also has four audio formats: Dolby Digital (AC-3), Linear PCM, MPEG-1 Audio Layer2 and MPEG-2 AAC. MB86H50 reduces the required amount of processing using FUJITSU’s proprietary high image compression technique. As a result of our memory incorporation technology and 90nm production processes, it is small in size and achieves low power consumption.

Product Features

Table 1 shows the main specifications and Fig.1 presents a block diagram of this product.

- High compression and image enhancement technology

For this product, we developed a self-tuning algorithm to control the compression with sharpness. Specifically, it automatically applies a weaker compression method to high-action zones where compression artifacts are most noticeable, such as human faces or slow-moving objects, and a stronger compression method in other zones. This enables image data size to be reduced by one-half to one-third that of the MPEG-2 format (standard for digital broadcasting systems) at an equivalent level of image quality.

This product is also capable of compressing and decompressing the full HD specification images (1,920×1,080) using the built-in scalar function.
**Miniature package**
A logic chip and two 256M-bit memories (FCRAMs) are incorporated in one small package. In addition to a reduction in the number of mounted parts, this eliminates the necessity of providing wiring to the high-speed operation memory, leading to a reduction in EMI noise and stable operation.

**Low power consumption**
In addition to the minute power control and optimal design in the logic chip and memory, our advanced image compression algorithm realizes low power consumption of 600mW (standard: 1.2V in encoding operation), including the memory.

**Development Environment**
We offer the evaluation board shown in Fig.2 for evaluation of this product as well as software development. The MB86H50 evaluation board mounts A/V input/output, stream input/output, host interface FPGA, and ARM926 as the host controller. In addition, it mounts a special stream input/output connector and is capable of simultaneous evaluation with opposed encoding and decoding sides through the connection of two evaluation boards with a cable.

Fig.3 shows the software configuration for the evaluation board.

The host controller operates on Linux. FUJITSU provides sample drivers and source codes for sample applications and so forth to help the customer reduce their software development load.

**Future Development**
FUJITSU will continue to develop higher functions in the future to address full HD (1,920-dot×1,080-line). We will also continue adding to our image-processing LSI
products including a multidecoder supporting multiple formats such as H.264 and MPEG-2 and MPEG-2 transcoders.

**NOTES**

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**Figure 2** MB86H50 Evaluation Board and Development Environment

**Figure 3** Software Configuration for Evaluation Board