Necessity for High-speed Signal Transmission in Consumer Products

High-speed interfaces have conventionally been used in backbone or enterprise equipment that handles large amounts of data such as telecommunication equipment and servers. However, the amount of data required for the input/output of consumer products that handle image data has recently been increasing.

For example, digital still cameras (DSCs) and digital video cameras (DVCs) now require higher speed in the interface due to the drastic increase in the amount of data from the image capture device to the image-processing LSI chip. For digital still cameras (DSCs) with over 10 million pixels, the amount of data exceeds 1Gbps when the continuous shooting speed (the number of images that can be shot per second) increases. The data bandwidth is expected to be 5Gbps or larger, especially for high-class single-lens reflex (SLR) digital still cameras in which a large number of pixels and high continuous shooting speed are required. Furthermore, the amount of data exceeds 1Gbps for digital video cameras due to the adoption of digital HDTV such as 1080i/1080p, the increased number of frames, and the increased number of bits per pixel for image quality improvement. A large amount of data flows from the processing chip to the display panel of digital TVs (Fig.1).

Processing of these data can be conducted on a different chip; data processing is not integrated on a chip due to the chip to chip distance within an equipment and/or physical placement of LSI devices. As such, an interface is required between them. Conventionally, CMOS interfaces of up to 50MHz have been adopted for this purpose. However, the number of wires increased as the amount of data increased, which made it difficult to adjust the skew between signals and arrange the trace routing is an increasing need for high-speed transmission in order to drastically reduce the number of wires.

Advantages of High-speed Signal Transmission

Cost reduction
For example, to transmit 8.1Gbps data,
- For a CMOS interface, 67.5Mbps×120 lines=8.1Gbps (single end)
- For a high-speed interface, 810Mbps×20 lines/2=8.1Gbps (differential)
and as many as 100 signal lines can be reduced. In concurrence, the number of power supplies and grounds can be reduced for the interface.

With the reduction in the number of signal lines, power supplies, and grounds, cost reduction is possible for the transmission lines between LSIs (printed circuit board, cable, and connector) as well as for the LSI itself (package and chip).

Measures against noise
When many signals change simultaneously, switching noise occurs due to fluctuations in the current and the package inductance, it leads to data error (noise due to simultaneous switching output). Reinforcement of the power supply and the ground is necessary to mitigate this problem. Thus, high-speed interfaces use differential signals and adopt circuit configurations

LVDS Interface Hard Macro for Image Applications

This article presents general information on the LVDS interface hard macro for image applications.

* LVDS: Low Voltage Differential Signaling
with small changes in the current from the power supply. Furthermore, the differential signal transmits in “normal” and “reverse” phases, it is also effective as a measure against EMI since the radiation noise to external parts is eliminated.

**Reduction in power consumption**

For high-speed signal transmission, power consumption can be reduced compared to transmission by CMOS. For example, it can be calculated as follows:

- CMOS: 120 lines×3mW (3.3V, 67.5MHz, 10pF)=360mW
- LVDS: 10 lines×6.4mW (100Ω, 200mV)=64mW

It is possible to reduce the power consumption for ASSP and the CMOS interface block of the processing chip by replacing the external CMOS-LVDS conversion ASSP with a built-in LVDS interface macro.

**Lower Power Consumption LVDS Interface for Mobile Devices**

In mobile devices, power consumption needs to be suppressed to equivalent or lower levels as conventional devices even when the amount of data increases. Since LVDS, which is specified in EIA644 and IEEE1596.3, is designed for “large” telecommunication equipment, etc., it is not directly suitable for mobile products. Therefore, various measures are required to reduce power consumption.

Specifically, power consumption reduction has been realized through the following restrictions and measures:

- The maximum transmission distance for transmission within the mobile device is about 20cm
- Compatibility to the interface with a 3.3V power-supply LVDS is abandoned
- Power-supply voltage is reduced
- Minimize the current of circuit with 90nm process technology, the LVDS receiver macro (Rx) developed for image-processing LSI chips has realized 6.4mW, max. (3.2mW, typ.) @650Mbps, per channel. As such, this is suitable as an interface of the image data input from the analog front end (AFE) for mobile products.

**Figs. 2 and 3** present examples of 90nm low-power LVDS receiver macros.

Using this interface, a low power receiver macro can be realized for an image-processing LSI chip, at 8×6.4mW=51.2mW (worst) in 5.2Gbps data transmission, for example.

For DEMUX (serial-parallel conversion) circuit, ether fixed or flexible DEMUX ration can be applicable. Integrating DEMUX circuit into user logic will allow more flexibility in design.
LVDS Interface for Displays

High-speed LVDS has been used as the interface from image-processing LSI chips to FPD panels such as LCDs and PDPs. At present, external ASSPs are widely adopted and CMOS is used as the interface between the image-processing LSI chip and ASSPs. To reduce the number of signal lines between them, the integration of high-speed LVDS interfaces into image-processing LSI chips is now widely adopting.

Fig. 4 presents an example of interfaces between chips using FPD Link in DTV (digital TV).

The amount of data handled in DTV has been growing with digital HDTV adoption, increased number of bits, and increased number of pixels. Thus, the number of signal lines may become excessive in the previously described CMOS interfaces. Furthermore, the number of pins for an image-processing LSI chip itself does not change and the cost of the LSI (chip and package) does not decrease even when an external ASSP is adopted. It is possible to reduce the costs of the LSI, ASSP, and transmission paths (printed circuit board, cable, and connector) simultaneously by integrating an equivalent function of this ASSP to the image-processing LSI chip as a macro (Figs. 5 and 6). In this case, the number of data channels, etc. can be optimized for suitable applications. It is also possible to adopt a method to integrate the ASSP used in the system gradually into the image-processing LSI chip since compatibility and interoperability of the ASSP has been considered for signal levels and timings.

Figure 2 Example of 90nm Low Power LVDS Receiver Macro

- **Timing chart**
  - Data Setup Hold Setup Hold
  - Clock

- **Features**
  - Configuration: 1 clock + 1 frame + 8 data
  - Data rate: 650Mbps/channel (DDR clock)
  - VDDE: 1.8 V ± 0.15 V
  - VDDI: 1.2 V ± 0.10 V
  - VCM: VDDE/2 ± 0.10 V
  - VID: 100 mV to 300 mV
  - RIN: 100 Ω ± 20 % (Built-in termination resistor)
  - Pw: 3.2mW/channel (Typ.), 6.4mW or less/channel (Max.)

Figure 3 Example of 90nm Low Power LVDS Receiver Macro Layout

- **Features**
  - 8 data + 1 frame + 1 clock
  - DEMUX ratio: 1:4
  - Serial data rate: 650Mbps (Max.)
  - Size: 2.35mmX0.70mm (50μm pad pitch)
Summary

The LVDS interfaces that have been used in telecommunication equipment are beginning to be widely adopted in consumer products. By integrating LVDS interfaces into LSIs, it is possible to reduce the total cost and utilizing their high-speed, low power consumption, and low noise features.

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**Figure 4** Example of an Interface between Chips by FPD Link for DTV

**Figure 5** Example of 90nm FPD Link Transmitter Macro
Figure 6  Example of 90nm FPD Link Transmitter Macro Layout

Data: 140Mbps to 945Mbps × 5 channels × 2
Clock: 20MHz to 135MHz × 2 channels

Features
(5 data + 1 clock) × 2
DEMUX ratio 1 : 7
Serial data rate: 945Mbps (Max.)

Parallel data
20MHz to 135MHz × 7bits × 5 channels × 2