CMOS Multi-Gigabit High-Speed Interface

The CMOS multi-gigabit high-speed interface has come into widespread use with its ability to markedly improve the speed of information input/output circuits. This article introduces this high-speed interface, which caters to general consumers through to high-end professionals, enabling higher bandwidth connections and more densely integrated system designs, as well as to introduce its support services.

Overview

High-speed interfaces, which have been developed with an emphasis on improving system performance, can now be managed at relatively low cost as a result of technological improvement.

Until recently, the CMOS multi-gigabit high-speed interface was intended for high-end applications such as communications and server systems. However, with the establishment of standards such as PCI Express*1 & Serial ATA (SATA)*2, technological progress in signal integrity compensation, and decreased costs, it is now being used in personal computers as
well as in various low cost consumer and industrial devices.

In high-speed data transmission, it is essential to take a comprehensive look at all transmission lines—not just the device itself, but at the package, the connectors, the circuit board, and the cables as well. In order to develop products and systems that use high-speed interfaces without any reworking, it is necessary to take signal integrity (signal quality) into account. In addition, optimization of the entire system, including the device and the transmission lines, is necessary to achieve a reduction in total system costs.

Recently, with the establishment of high-speed interface industrial standards, interfaces that comply with these standards are considered to be best suited to interdevice connections. When the data transmission is closed within a system, it is also possible to optimize the speed, power consumption, cost, etc. based on individual system requirements.

FUJITSU offers a wide range of high-speed interfaces as IP for ASICs. We also provide a high-speed transmission support service that improves the optimization of cost and performance.

**Figure 1** presents the lineup of our main high-speed interfaces.

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**Typical Interfaces and the Technology behind them**

**Interfaces for Image Signals**

The volume of image data, even that of consumer products, is dramatically increasing due to the increased use of video and the increase of pixels. As a result, it has become necessary to select high-speed interfaces that are suitable to these applications.

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**Figure 2** 0.18μm TMDS Tx (HDMI) Macro

**Figure 3** 0.18μm TMDS Tx (HDMI) Differential Eye-Pattern

**Figure 4** Examples of Chip-to-Chip Interfaces
HDMI/DVI (Figs. 2, 3)

HDMIs and DVIs are available as box-to-box interfaces for flat panel displays, etc. It is expected that HDMIs will be widely used in devices with video functions from now on. A wide bandwidth corresponding to a bandwidth of 1.6 Gbps per channel for a 1080p-resolution HDTV will be necessary in order for the uncompressed digital image data to be transmitted.

Link using clock synchronous-type LVDS

A link using clock synchronous-type LVDS is suitable for interfaces within a box such as chip-to-chip or board-to-board interfaces. Fig.4 presents examples of chip-to-chip interfaces.

Clock synchronous-type interfaces that use frame signals to eliminate troublesome initialization and data alignment are also available for chip-to-chip interfaces (Figs.5, 6). They are designed to limit the data rate to 1 Gbps or less in order to minimize possible signal integrity problems. They can change the serial-to-parallel ratio and therefore may be substituted for any existing discrete LVDS Link LSIs, etc. to constitute a general-purpose high-speed chip-to-chip interface.

subLVDS Link

The subLVDS Link, with its low voltage, low current, and low amplitude settings, is suitable for applications in which the transmission distance is short and the power consumption must be kept to a minimum, like mobile equipment.
5 to 6.4 Gbps Interface (Fig.7)

Achieving a reduction in transmission costs for the whole system would be difficult solely by raising the transfer speed for each channel; with higher speed comes higher power consumption, presenting a significant problem.

Through the development of equalizer circuitry at the receiver side, high-frequency losses brought about at the backplane and/or through cable transmission can be compensated for by over 1m, or over 20 dB (approx.) in backplane transmission.

Fig.8 presents the equalizer characteristic of 6.4 Gbps interface.

In addition, although raising transmission amplitudes at 1.2 V was difficult, by using the LVDS type (Fig.9), it was possible to achieve an amplitude of over 500 mV even with an AC coupled connection (Fig.10). With the decreased voltage, power consumption was cut by approximately 50%. This technology can be applicable for PCI Express-2, SATA-3, double XAUI, etc.—standards that are currently under discussion.

Interfaces that conform to Industrial Standards

PCI Express, Serial ATA, etc. are interfaces that conform to industrial standards. They are suitable for applications in which several different devices, various add-on boards, or external storage systems are to be connected. Being widely used standards, they can be used at low cost including the connectors and cables.

FUJITSU conducts complete verification of these interfaces that conform to industrial standards together with upper layers (LINK, TRANSACTION, etc.), offering them as ASIC macros.

Intersymbol Interference Compensation Technology

High-frequency signals can deteriorate at the receiver side, due to dielectric losses, conductor losses, reflection, crosstalk, etc. within the transmission line.

Fig.11 outlines the high-speed transmission problem.

Through the stable use of compensation technology (Intersymbol Interference Compensation Technology) as well as long-distance transmission and low-cost packages, PCBs,
connectors, and cables, a reduced-cost, high-performance system can be realized. Intersymbol Interference Compensation Technology includes a pre-emphasis on the compensation of losses in transmission lines by emphasizing, at the transmitter side, the high-frequency component of the signals. In addition, an equalizer at the receiver side amplifies the high-frequency components. Appropriate technology can be employed to fit the characteristics of the transmission lines, the power consumption, the characteristics of the devices at the opposite end, etc.

**Fig.12** presents the effectiveness of the Intersymbol Interference Compensation Circuit.

### High-Speed Transmission Support Service

As signal transition time becomes faster, the frequency component of the signals becomes higher. This results in high-frequency losses such as dielectric losses, skin effects, crosstalk, and sensitive reflections as a result of impedance mismatch along transmission lines. High-frequency losses result in the deterioration of the waveforms of transmitted signals at the receiver end. This can result in signal transmission difficulty.

In order to achieve reliable signal transmission, care is needed in system design, in terms of the quality of waveforms along transmission lines. This is called “Signal Integrity”, which can be categorized into improvement of the LSI chip circuit design and improvement of the transmission line including PCBs.
FUJITSU is currently providing a High-Speed Transmission Support Service as an approach to the “first pass success” idea for customers who particularly utilize the high-speed interface. This service contributes to our customers’ system designs and is supported by FUJITSU’s accumulated know-how on PCB design and transmission evaluation for multi-gigabit transmission based on our extensive experience in the development of high-speed interfaces.

We will be offering the following four services:

**Evaluation Environment Support Service**
- Evaluation kit rental with an incorporated high-speed interface

**Measurement Service**
- Characteristic impedance measurement of transmission lines with TDR (Time Domain Reflectometry)
- Measurement of the S parameter in transmission lines using a VNA (Vector Network Analyzer)
- Evaluation of transmission waveforms through a high-speed interface (Fig.13)
- Contract measurement/evaluation targeting industrial standards such as PCI-Express or DVI

**Modeling/Analysis Service**
- Creation of a transmission line model (Fig.14)
- Transmission waveform analysis
- Analysis of electromagnetic fields in transmission lines

**PCB Design Consulting**
- Provision of PCB design guidelines for high-speed transmission
- Circuit board design consulting

Evaluation kit rental (with an incorporated high-speed interface) is intended for customers who are thinking about adopting a high-speed interface. This will enable them to see the actual device in operation. The kit is also intended to allow customers to assess the connection between the interface and their transmission line.

We also offer a service for ES evaluation, which includes circuit board design consulting and measurement based on the customer’s evaluation board design; this service is highly regarded by our customers. We have also been receiving positive responses.
to system improvements carried out using transmission line modeling and analysis results based on measurement result feedback.

**NOTES**

*1: PCI Express: A general-purpose interface for PCs based on the 2.5 Gbps CDR (Clock Data Recovery). Also starting to be used in consumer products and industrial devices.

*2: Serial ATA: An interface for hard disks and DVDs. In the SATA-II, 3.0 Gbps has been prescribed in addition to the 1.5 Gbps. A standard for long-distance transmission is also provided.

*3: PCI Express-2: A standard is now under discussion as the next-generation PCI Express. We may gain twofold higher speed than that of the existing PCI Express with the speed of 5Gbps/lane.

*4: SATA-3: A standard is now planning as the next-generation Serial ATA. We may gain twofold higher speed than that of the existing SATA-2 with the speed of 6Gbps/lane.

*5: double XAUI: A standard is now planning as the next-generation XAUI. We may gain twofold higher speed than that of the existing XAUI with the speed of 6.25Gbps/lane.