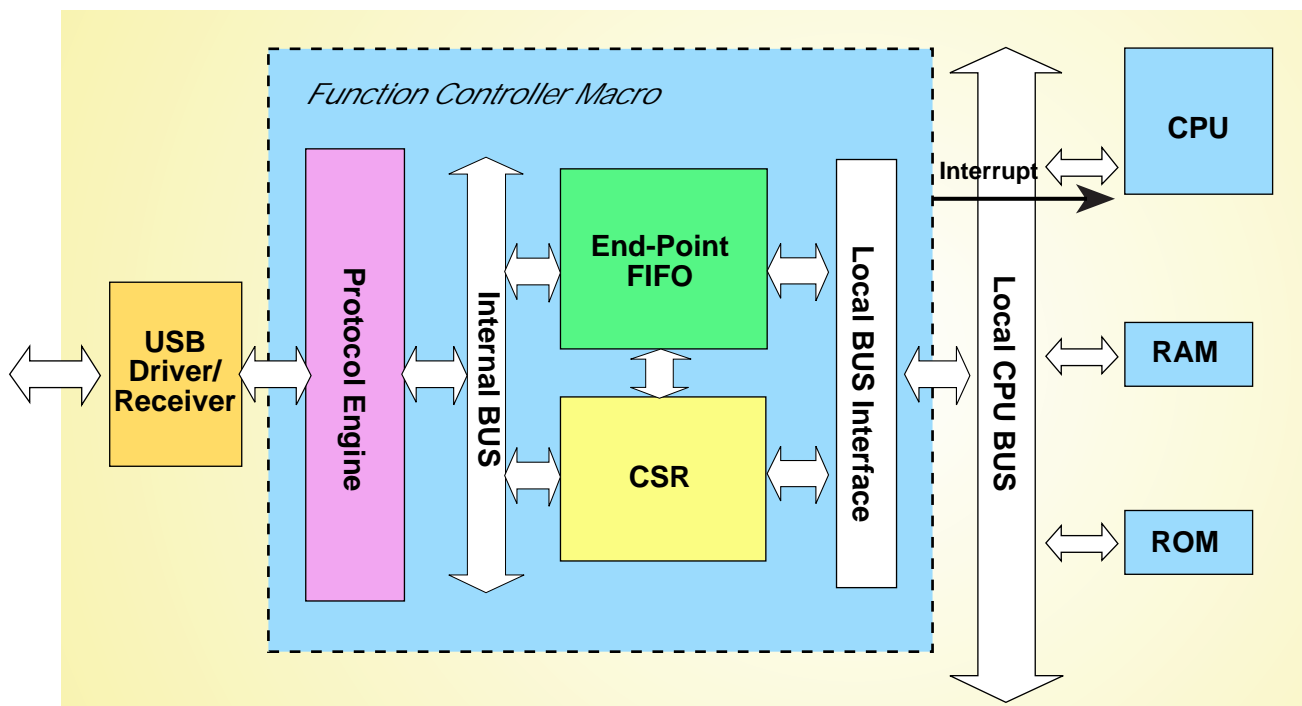


Standard Bus IP: USB 1.1 Device Controller



Features

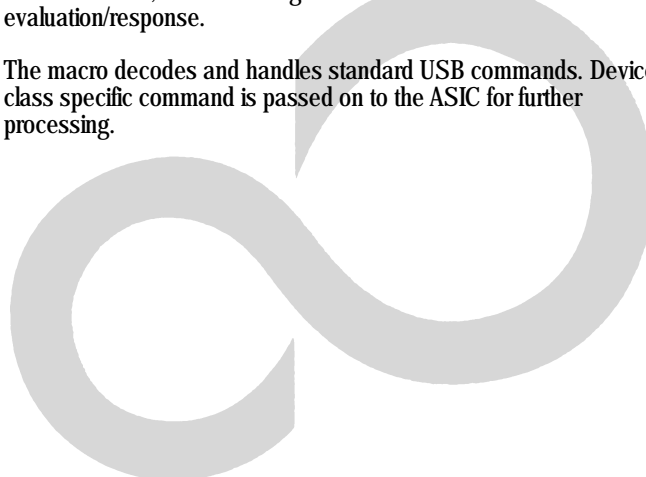
- Compliant to USB specifications 1.1 (Function Controller)
- Configurable endpoint for various application requirements
- Supports Control, Bulk, Interrupt and Isochronous transfer
- Built-in FIFO for all endpoints
- Digital phase lock loop for clock and data recovery
- Low speed (1.5Mbps) and High Speed (12Mbps) operations
- Generic 16bit/32bit CPU interface for ASIC integration
- Various control and status registers available
- Optional physical layer also available for ASIC integration

Overview

Fujitsu USB device controller is a synthesizable core suitable for different process. Corresponding physical interface in 0.25 μ m and 0.35 μ m technology (supporting high and low speed operation) also available for integration.

Generic CPU interface makes it easy to be integrated into overall ASIC. Different endpoints are available for application such as printer, scanner, digital still camera, bluetooth devices etc. Integrated SIE performs synchronization pattern recognition, bit stuffing/stripping, CRC check/generation, serial/parallel conversion, PID verification, address recognition and handshake evaluation/response.

The macro decodes and handles standard USB commands. Device class specific command is passed on to the ASIC for further processing.



Endpoint, Control and Status Registers

Fujitsu has pre-configured the following popular configurations. Additional configurations are available on request.

Configuration 1: Control EP, 1 (EP0)
Bulk IN EP, 1
Bulk Out EP, 1
Interrupt EP, 1

Configuration 2: Control EP, 1 (EP0)
Bulk In/Interrupt EP, 4
Bulk Out/Interrupt EP, 4

Configuration 3: Control EP, 1 (EP0)
Bulk Out EP, 1
Bulk In EP, 1
Interrupt EP, 1
Isochronous Out EP, 1
Isochronous In EP, 1

The array of control and status registers accessible by ASIC eases customer's firmware development. These registers allow customer to:

- enable/disable an Endpoint (EP)
- check data transmission status to and from EP
- check transfer size
- check class/device specific commands reception
- enable/disable generation of interrupt
- put an EP into stall status

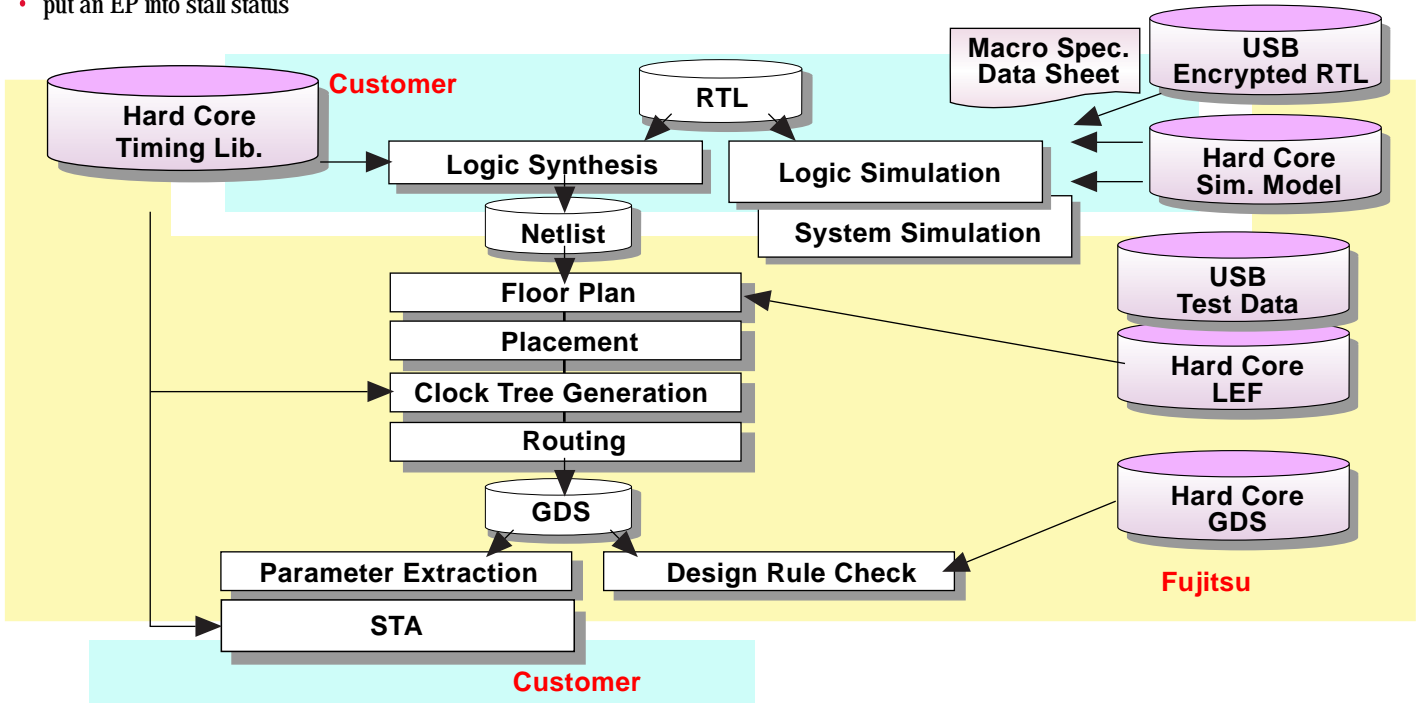
ASIC Development Support

Fujitsu provide analog macro to supplement ASIC development, such as USB transceiver, and APLL (various speed combinations). Accurate timing model is provided for synthesis, simulation and Static Timing Analysis (STA).

Small gate count and soft coach approach makes it efficient to integrate into an ASIC. Fujitsu provides a set of functional vectors to customer for module hand-shake and full chip verification. Our application engineer works with you on full chip design for testability (DfT) consultation.

Deliverables:

- USB test chip with selectable configurations,
- Test chip and macro specifications
- Encrypted RTL for top level simulation
- Application notes and testability guide
- Test benches for standalone IP verifications



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