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shaping tomorrow with you

Fujitsu Next UNIX Server

Fujitsu M10

Servers for Big Data Era

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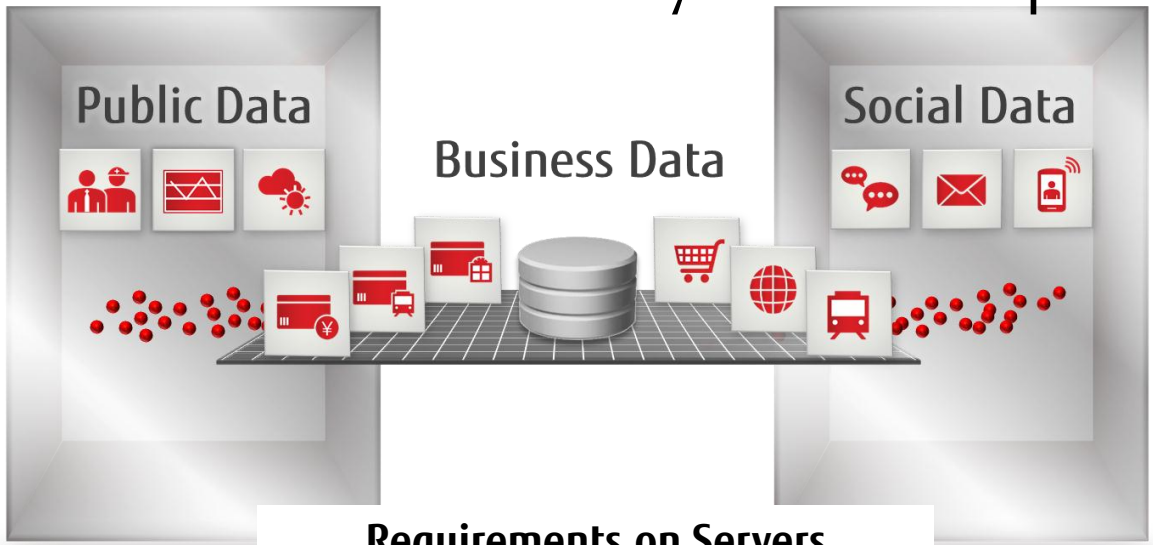
- Insight with Big Data Analysis + Real Time Processing
  - Strive to survive and thrive beyond the competition



Requirements on Servers

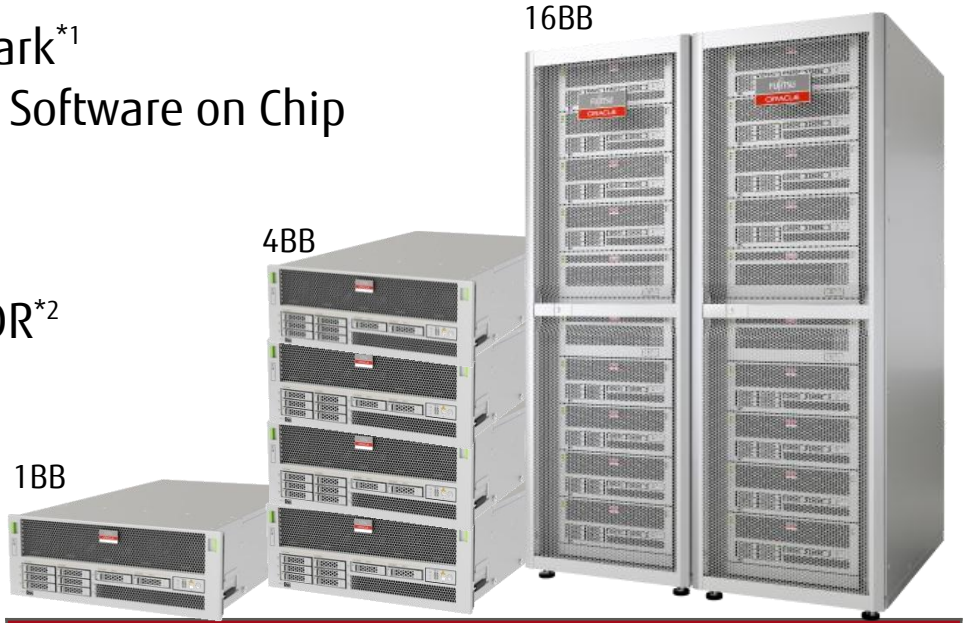
High Performance

Flexibility and Expandability

Data Integrity

Fujitsu M10 Meets Any Business Needs
–SPARC/Solaris Based SMP Server-

- **High Performance**
  - 14 World Records in Standard Benchmark*1
  - OS/DB Performance Improvement with Software on Chip
- **Flexibility and Expandability**
  - Max 1024 core / 32TB Memory
  - CPU Core Activation / Building Block / DR*2
- **Data Integrity**
  - Mainframe RAS



Fujitsu M10-1	Fujitsu M10-4	Fujitsu M10-4S
1 socket (Max: 16 cores)	4 sockets (Max: 64 cores)	4-socket Building Block can scale up to 64 sockets (Max: 1,024 cores)

*1: Except supercomputing, *2 DR: Dynamic Reconfiguration

Fujitsu M10 Benchmark Test Results

- **STREAM TRIAD**[*1]
- **SPECint_rate2006**[*1]
- **SPECfp_rate2006**[*1]
- **SPECjbb2005**
- **SPECjbb2013**
  - Max
  - Critical
- **SAP 2-tier SD standard application**

*1:Except supercomputing

SAP SD Benchmark

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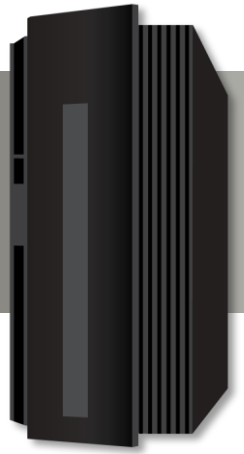
IBM
Power 795



Fujitsu
M10

Performance

126,063 users

153,000 users

WIN!

SPECjbb2013 Benchmark (Response Performance)

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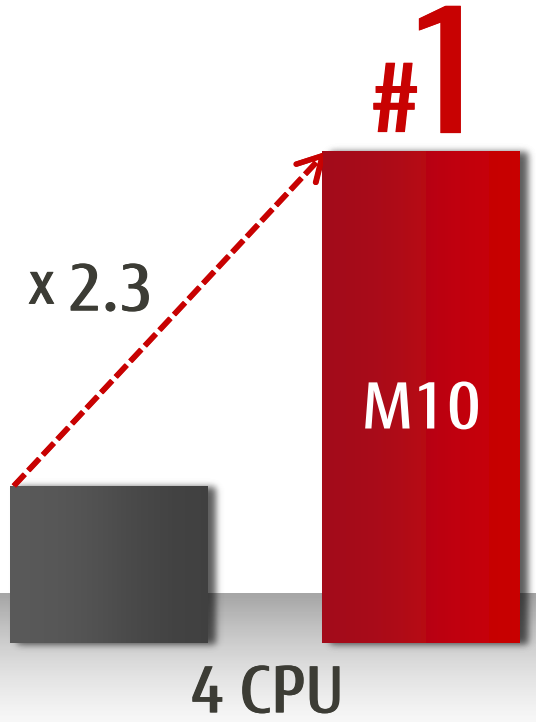

Fujitsu M10: Proven #1 response performance with real applications

SPECjbb2013 Benchmark (Response Performance)

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Fujitsu #1
Among All Computers
(168,127 critical-jOPS, 16CPU)

Fujitsu M10: Proven #1 response performance with real applications

SPARC64™ X

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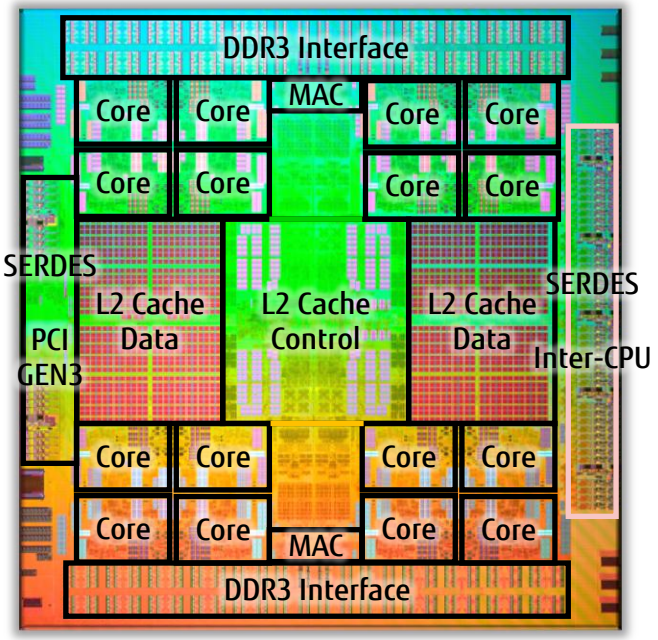
- Facts:
  - High Performance / High Reliability Processor
  - 16 core, 2 thread/core, Max 2,048 threads/system
  - L1$ per core: 64KB (I) + 64KB (D)
  - L2$ per CPU chip: up to 24MB
  - 28nm
  - Rich Software on Chip Features
  - System on Chip: integrated Memory and I/O controllers
  - Oracle VM server for SPARC support (sun4v)
  - Robust RAS
- Important because:
  - High performance, x7.5 faster compared to SPARC64 VII+ (SPECint_rate)
  - Mainframe class high reliability



Software on Chip

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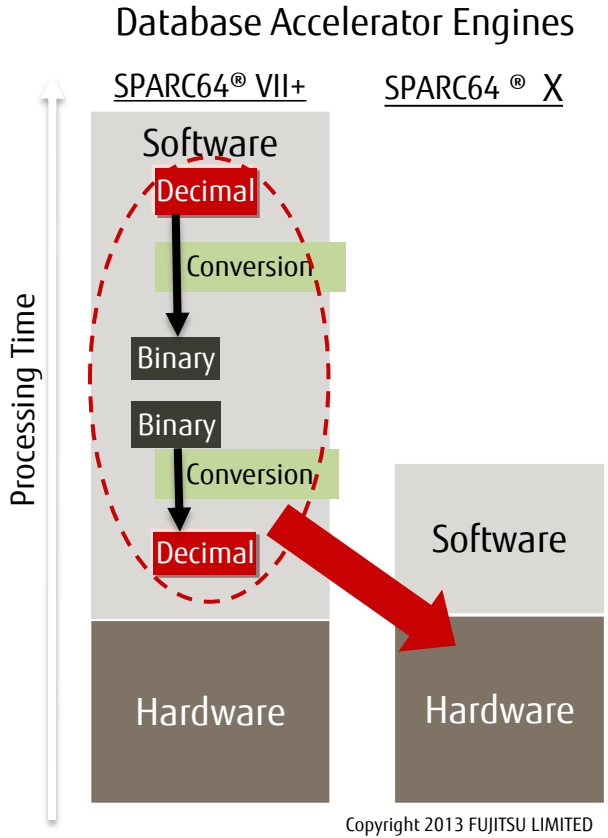
- **Facts:**

  Software operations moved to *specialized* CPU hardware

  - Database Accelerator Engines
    - Supports decimal floating-point processing
    - Direct decimal execution of Oracle NUMBER by hardware
  - SIMD (Single Instruction Multiple Data)
    - High speed data processing
  - Encryption/Decryption Engines
    - Supported algorithms : AES, DES, 3DES, RSA, and SHA

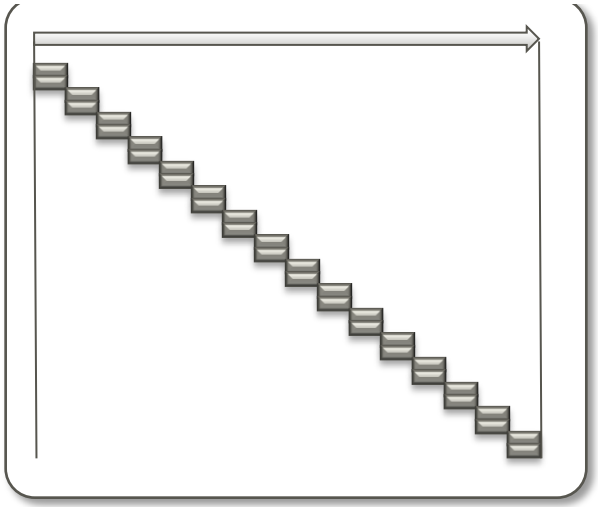
- **Important because:**

  - Large performance gains
    - Up to +25% Performance Improvement
      with DB12c patch and custom Fujitsu benchmark
    - Encrypt: 5x, Decrypt 12x (on Solaris11)



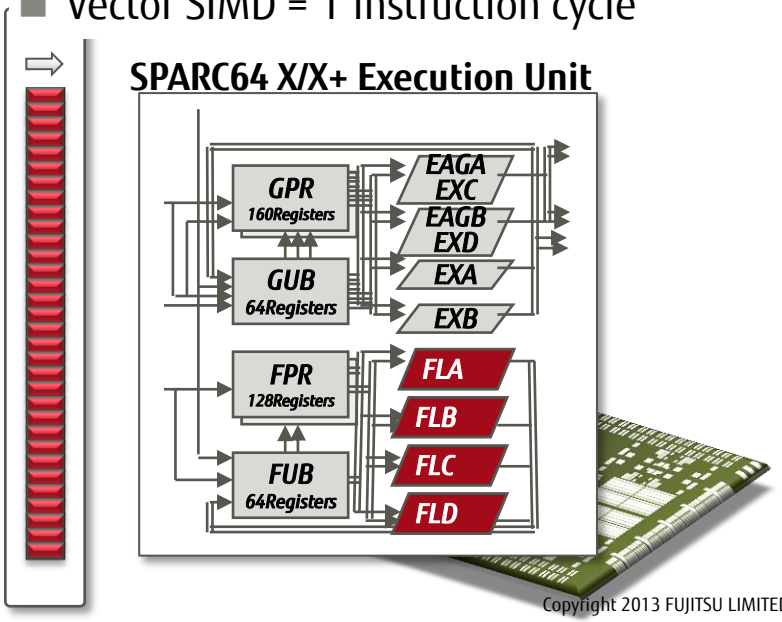
Software on Chip: Performance Acceleration of In-Memory DB

- With focusing on business use, high speed vector operation is enhanced from one for supercomputer
- By hardware, faster processing of columnar in-memory DB, which was announced in OOW2013
  - Non SIMD requires 16 instruction cycles



16x

  - Vector SIMD = 1 instruction cycle



CPU Core Activation

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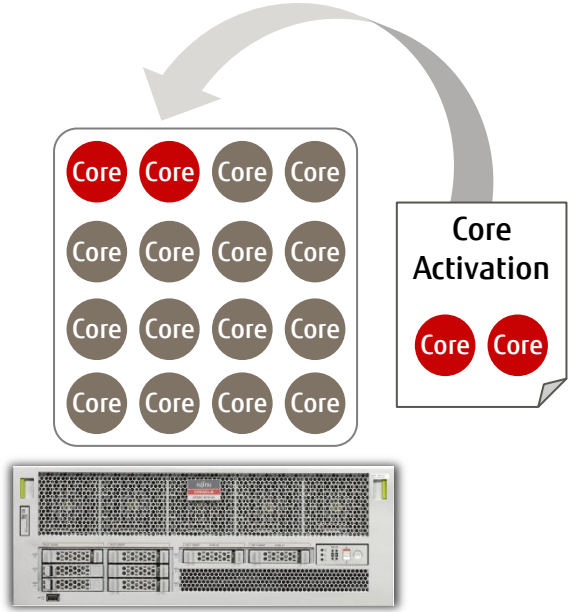
- Facts:
  - Purchase core activations 2-by-2.
  - Expand without interrupting your business
  - Core activations can be moved between M10 systems
  - Core auto-replacement
- Important because:
  - Optimized investment: “start small and grow big”
  - Lower initial cost for hardware and software
  - Buy only what you need with fine granularity for better resource utilization
  - Adapt CPU cores to changes in your business dynamically
  - Inactive cores are hot spare cores



Building Block ("BB") Architecture

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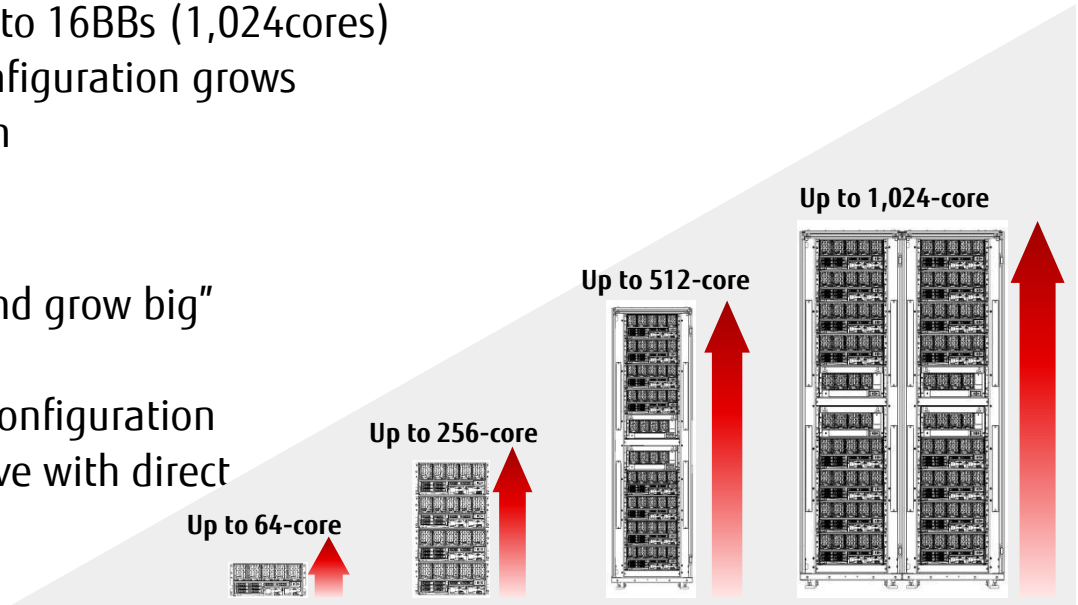
- Facts:
  - One Building Block = 4 CPU sockets, 64 DIMMs
  - Compact 4U BB Chassis
  - Expandability: from 1BB (64cores) to 16BBs (1,024cores)
  - Linear performance gain as the configuration grows
  - XB redundancy in any configuration
- Important because:
  - Efficient investment: "start small and grow big"
  - Space saving
  - High Availability with Dynamic Reconfiguration
  - Mid-size configurations cost effective with direct BB-to-BB cabling



High-Speed Interconnect

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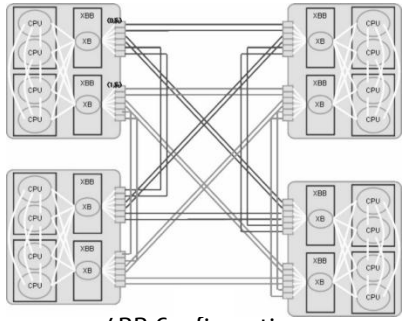
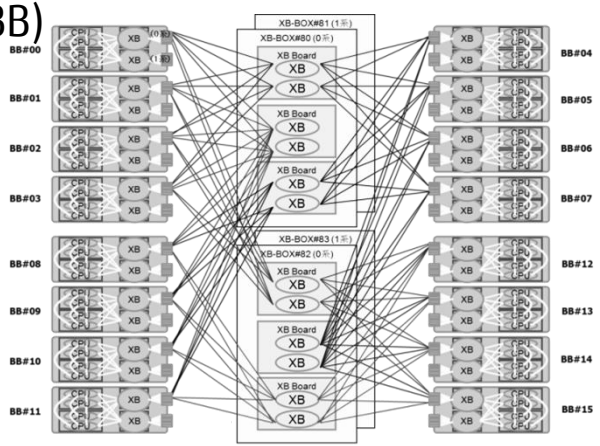
- Facts:
  - Fujitsu's state-of the-art transmission technology
  - High speed 14.5Gbps x 8 lanes Serial Interface
    - 14.5GB/s x 5 ports per SPARC64 X
  - Up to 4 BBs, Interconnects all in-Chassis
  - Low latency data processing
  - Linear performance scalability up to max configuration (16BB)
  - Mainframe RAS: Fujitsu DNA (Mainframe Heritage)
    - Redundancy built-in
- Important because:
  - High performance
  - High availability
  - Invisible to software



4BB Configuration



16BB Configuration

Hybrid Cooling with LLC*1

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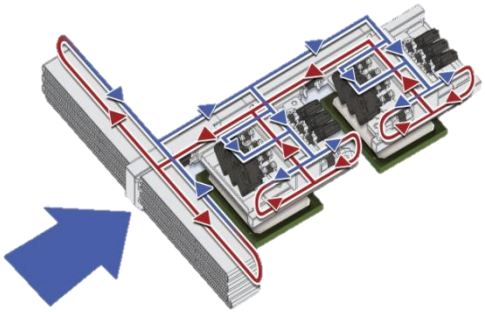
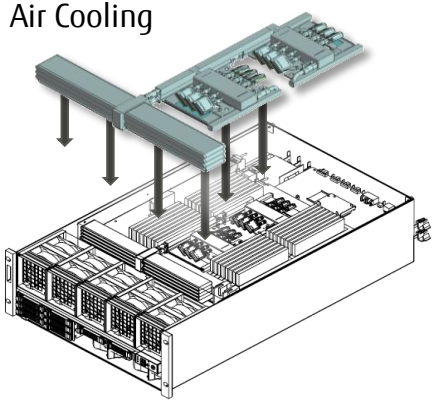
- Facts:
  - Air Cooling + Liquid Cooling
    Coolant circulates heat from CPUs to a radiator to be air-cooled
  - Self-contained liquid cooling for System-on-Chip CPU
  - Anti-freeze-like liquid flows through plates, tubes, tanks, and radiator
  - 4CPU x6 (5+1 redundant) inline micro-pumps per Building Block
  - Shorten distance between CPU and memory

Liquid Cooling



Air Cooling



- Important because:
  - Heatsink-less design allows components to be densely placed
  - Saves 3U of space in each 4-socket Building Block
  - 80% reduction of memory latency → performance improvement
  - Self-contained cooling for the life of the system and no external pipes/hoses enable maintenance free.

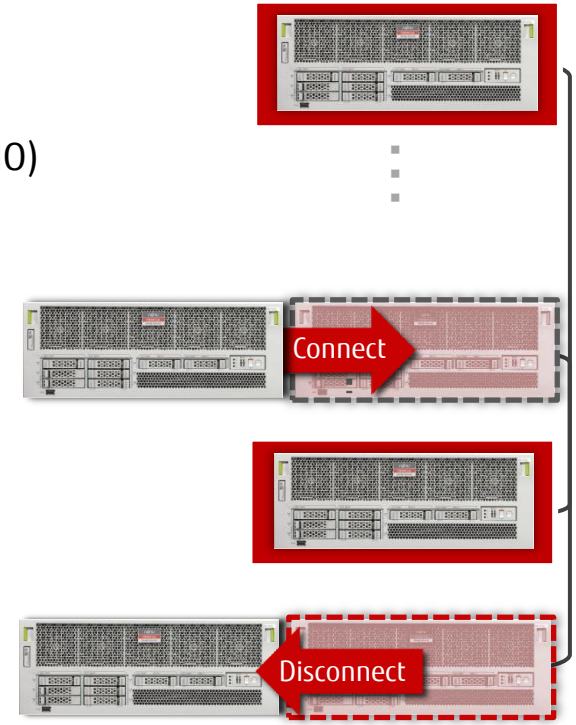
*1 LLC: Liquid Loop Cooling

Dynamic Reconfiguration

- Facts:
  - Building Block add/remove without interrupting your business
  - Expand CPU, Memory and IO* with DR

    (* some restrictions exist for DR of IO)

- Important because:
  - Business demands change and DR allows the M10 to match requirements on the fly.
  - CPU Core Activation + BB + DR provide extreme flexibility
  - Hardware failure impact greatly reduced with hot swappable Building Blocks



ORACLE | FUJITSU

Delivered

2012

Fujitsu M10

SPARC64 X:
3.0GHz, 16core, 32thread
System on Chip
Software on Chip
Fast interconnect
(14.5Gbps)

2013

Enhanced Fujitsu M10

SPARC64 X+:
3.5GHz+, 16core, 32thread
>1.3x Throughput
>1.3x Thread Strength
CMI, Software on Chip+
Faster interconnect(25Gbps)

2014

Next Generation Fujitsu M10

Next Generation SPARC64:
4.5GHz+, 24core, 96thread
>2x Throughput
>1.5x Thread Strength
FAST μArch
Data corruption prevention/
Software on Chip++
Faster Interconnect

2015

Next^2 Generation Fujitsu M10

Next^2 Generation
SPARC64:

2016

SPARC64® X+

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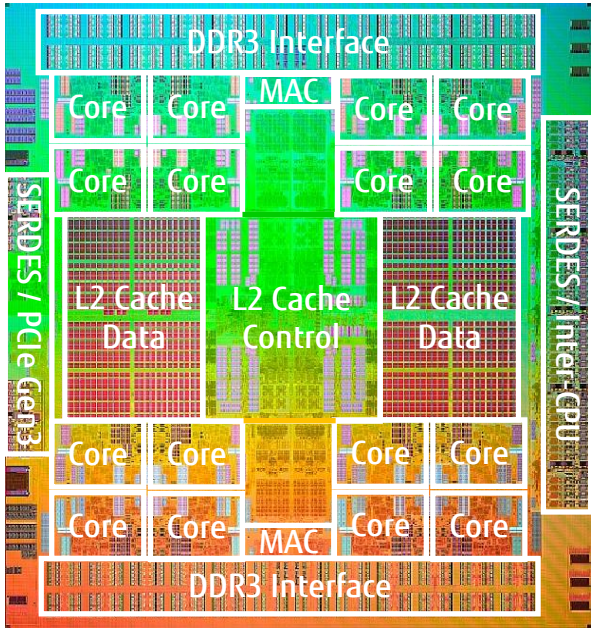
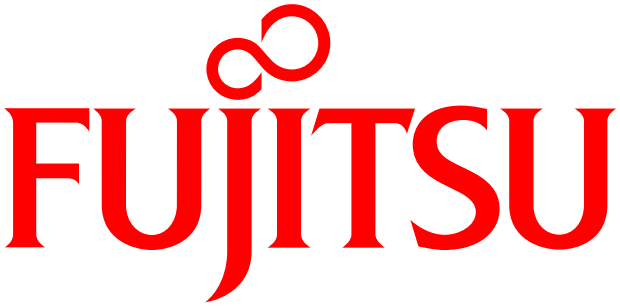
Fujitsu's next SPARC processor for enhanced M10

- Facts:
  - 20% increase in single thread performance and system throughput
  - Higher clock speed : 3.5GHz+
  - Large memory : Max512GB/Socket
  - 32TB memory/System
  - Scalability : from 1 to 64CPU Sockets(1024 cores)
  - Software on Chip+
  - Extensive RAS features
  - High-speed interconnect up to 25Gbps
- Important because:
  - "Next Generation SPARC64" is planned,
    SPARC64 X+ is not the end of SPARC64. Far from it!
  - SWoC enhancements push application performance further





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