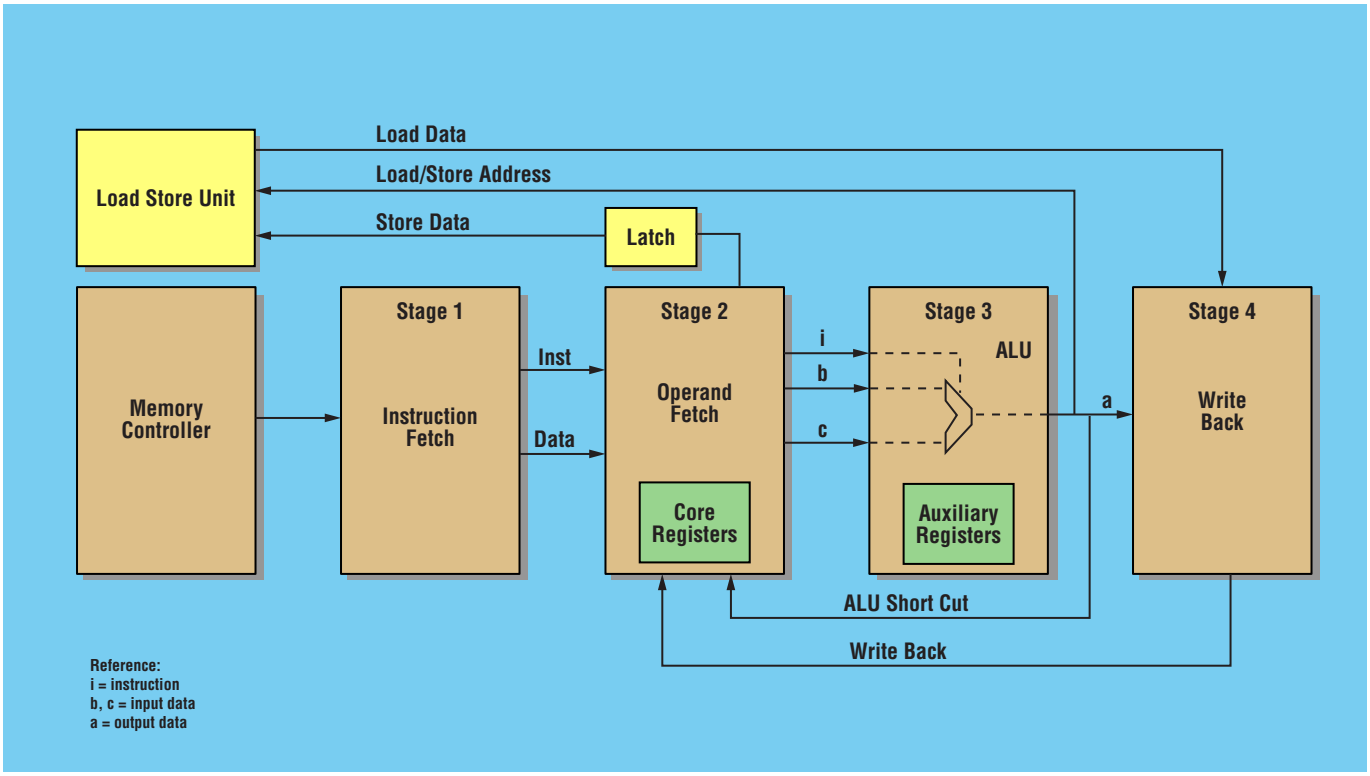
ARC Processor Core

FUJITSU



Features

- Application-specific custom core instruction
- Eliminates the need for separate DSP and processor
- Supports operation of 80 MHz (typical) at 2.5V
- Single hardware and software development environment
- Small die size
- Embedded on-chip debug logic

Benefits

- 50% reduction in power dissipation
- High performance for demanding applications
- Cost effective for ASIC integration
- Embedded system ready for fast time-to-market

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Description

ARC is comprised of a Base RISC Engine, the ARC Extension Library, the Architect, integrated test suites, multi-interface architecture, the ARC Co-design toolset, a complete software development toolchain, and both hardware and software emulators. Provided as a synthesizable "soft macro" with the configuration controlled by the user through the ARC Architect test suite, the ARC architecture can be configured to meet specific performance and cost targets enabling customers to effectively manage their design process at the system level.

The ARC is a 4-stage pipeline processor incorporating full 32-bit instructions, data and addressing. The instruction set is orthogonal with all addressing modes implemented on all arithmetic and logical instructions, as well as optional conditional execution on all instructions. The processor has separate instruction and data buses, and a number of external interrupt signals.

The ARC offers 32 separate instructions; the first 16 instructions are pre-defined in the base case and provide a set of arithmetic and logical instructions as well as load/store and branch/jump instructions. The remaining 16 instructions are available for the customer to add application-specific extensions; these may be instructions from the ARC library or ones that have been developed by the customer. Extension instructions can be single or multi-cycle and can be built with instruction-specific local memory that is separate from any of the other ARC memory systems.

The ARC development environment provides a seamless simulation and testing environment, essentially providing many levels of ARC code simulation and testing. The ARC High C software development toolchain is directly linked into the flow providing detailed information about the ARC at each step in the design flow.

This core is ideally suited for a variety of applications in the consumer space in Global Positioning Systems (GPS), handheld devices, digital cameras, cordless phones, as well as in the networking space in router applications.

Deliverables

A Fujitsu application engineer works with the customer to determine the process technology best suited to the customer's specific need. After the technology is selected, the following deliverables are supplied to the customer:

- RTL source codes written in VHDL
- VHDL Test Bench for functional verification

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Printed in the U.S.A. ASIC-FS-20852-03/2000