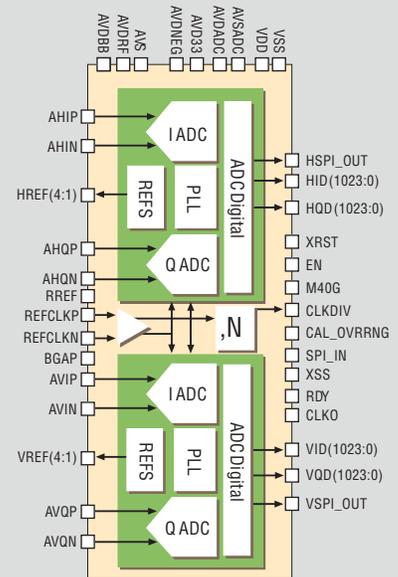


56GSa/s 8-bit Analog-to-Digital Converter



56GSa/s ADC Two-Channel Version Using CHAIS Architecture



56GSa/s ADC Four-Channel Version

Description

The Fujitsu ultra-fast CMOS ADC provides the enabling technology for upcoming telecommunication applications such as 100G Ethernet and OTU-4 transport systems using coherent receivers. The ADC uses Fujitsu’s revolutionary CHARGE-mode Interleaved Sampler technology (CHAIS), which allows the implementation of extremely fast, high-resolution ADCs in CMOS process technology.

Major benefits of the CHAIS ADC are low power consumption and the option to be integrated with millions of gates onto the same die using Fujitsu’s standard 65nm CMOS process technology. In combination with Fujitsu’s leading flip-chip packaging technology, the ultra-fast ADC is ideal for applications that require high-performance analog and digital processing power while maintaining a reliable and proven manufacturing flow.

With an effective resolution bandwidth of >15GHz and a sample rate of 56GSa/s, the ADC is at the leading edge of converter

performance. The macro employs a self-contained background calibration technique for sampler interleave-timing skew as well as linearity and offset. The calibration block also contains an alarm function, which can be used as an interrupt to warn the system when the internal calibration reaches a pre-defined or programmable percentage of its calibration range.

The first customer evaluation silicon (ROBIN) for the CHAIS technology contains a two-channel 56GSa/s version of the ADC. The on-chip RAM of ROBIN stores 16k x 8-bit samples for each ADC. The data can be accessed by reading this memory as there is no external output from the converter. Several storage modes that enable control of the RAMS from external triggers are available.

Other versions of the ADC with lower and higher sampling rates, and different channel configurations, are in development or planned.

Applications

- Fast data conversion
- 40G/100G communications systems
- Test equipment

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► Features

- Fujitsu 65nm CMOS process technology
- Resolution: 8-bit
- Sampling rate: 56GSa/s
- Power supply: -1.2V, 1.2V, 3.3V
- Power consumption: 2W per channel (typical)
- DNL: ± 0.5 LSB, INL : ± 1.0 LSB
- SNDR: 40dBFS @Fin=1GHz 36dBFS @Fin=17GHz
- Differential analog Input: 1.0VPPD
- >15GHz -3dB input bandwidth
- Two's complement data format
- Output rate: 128 samples x 8-bit @ 437.5MHz
- 1.75GHz input reference clock
- Internal 14 GHz VCO/PLL per I/Q ADC pair
- 56GSa/s ADCs configured as two I/Q pairs
- <100fs rms jitter, <500fs I/Q sample time error

► Development Kits

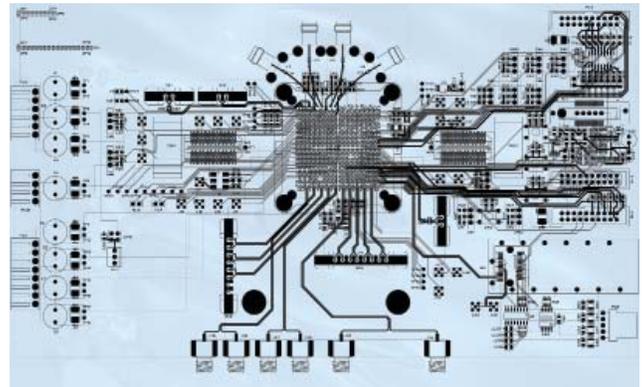
A development kit for the two-channel 56GSa/s ADC evaluation test chip is available in a ceramic package (ROBIN).

Each kit includes everything needed to minimize the time to getting started, including:

- BATBOARD evaluation board with the choice of ROBIN being solder mounted or with a socket
- Calibration board with the device mounted on it
- High-frequency splitter board
- Interconnect boards
- PC programming interface board
- Software

Description of Development Kits

The 56GSa/s ADC evaluation board (BATBOARD) is intended to allow rapid characterization of the ADC. Two variations of the board are available. The first board is mounted with a low inductance socket, which allows rapid replacement of the device under test. The socket incorporates a heat sink for increased heat dissipation. The heat sink can also be used with temperature-forcing systems to precisely control the die temperature. The second board has the device mounted directly



Batboard PCB Layout

- Continuous background calibration for sampler interleaving skew as well as linearity and offset
- Calibration warning and over-range flags
- Designed for flip-chip packages

onto it. Special attention has been given to the connector choice to allow connection to instrumentation, which will perform the design-verification tests. The printed circuit board utilizes high-performance materials to optimize the integrity of the signals. The development kit also includes Fujitsu's serial interface cable (ref DKSERIAL-1), which allows the device to be programmed through a Windows® application running on a host PC.

Key Features of the Development Kits

- Device mounted to a high-performance printed circuit board
- Superior signal integrity by using low-loss PCB materials
- 2-channel 56GSa/s analog to digital converter
- On-chip memory to capture ADC output data
- Software for control of the device from host PC
- Option to mount a low inductance socket to allow the device under test to be replaced

Development kit part numbers

- BATBOARD-DK: This evaluation board is supplied with a device mounted directly on it.
- BATBOARD-DK-SOCKET: This evaluation board is supplied with a low-inductance socket.

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