FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00031-1v1-E

Memory

Data-Processing FRAM
16 K (2 K × 8) Bit Dual SPI

MB85RDP16LX

■ DESCRIPTION

MB85RDP16LX is a Data-Processing FRAM in a configuration of 2,048 words × 8 bits incorporating a 43-bit or 46-bit binary counter, where FRAM (Ferroelectric Random Access Memory) is able to retain data without using a back-up battery, can be used for 10^{13} read/write operations and takes no wait time to write data, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. MB85RDP16LX can be accessed via Serial Peripheral interface (SPI) or Dual SPI.

This Data-Processing FRAM features short power up time, fast memory access and ultra-low power consumption. Together with the 43-bit or 46-bit binary counter function, MB85RDP16LX fits perfectly into energy harvesting and rotary encoder applications.

■ FEATURES

- Non-volatile memory configuration : 2,048 words × 8 bits
- Binary counter bit (for POS0/1/2/3) : 43-bit range (42bit mantissa + sign bit)
- Binary counter bit (for DIBC/DDBC) : 46-bit range (45bit mantissa + sign bit)
- Binary counter operation : Judged by the input position data or directly Increment and Decrement
- Interface : SPI (Serial Peripheral Interface) / Dual SPI
  Corresponding to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 15 MHz (Max for SPI) / 7.5 MHz (Max for Dual SPI)
- High endurance : 10^{13} times / byte
- Data retention : 10 years (+105℃)
- Operating power supply voltage : 1.65 V to 1.95 V
- Low power consumption : Operating power supply current 0.7 mA (Max@15 MHz)
  Standby current 11 µA (Max @+105℃), 1 µA (+25℃)
- Operation ambient temperature : −40℃ to +105℃
- Package : 8-pin plastic SON (LCC-8P-M04)
  RoHS compliant

June 2015

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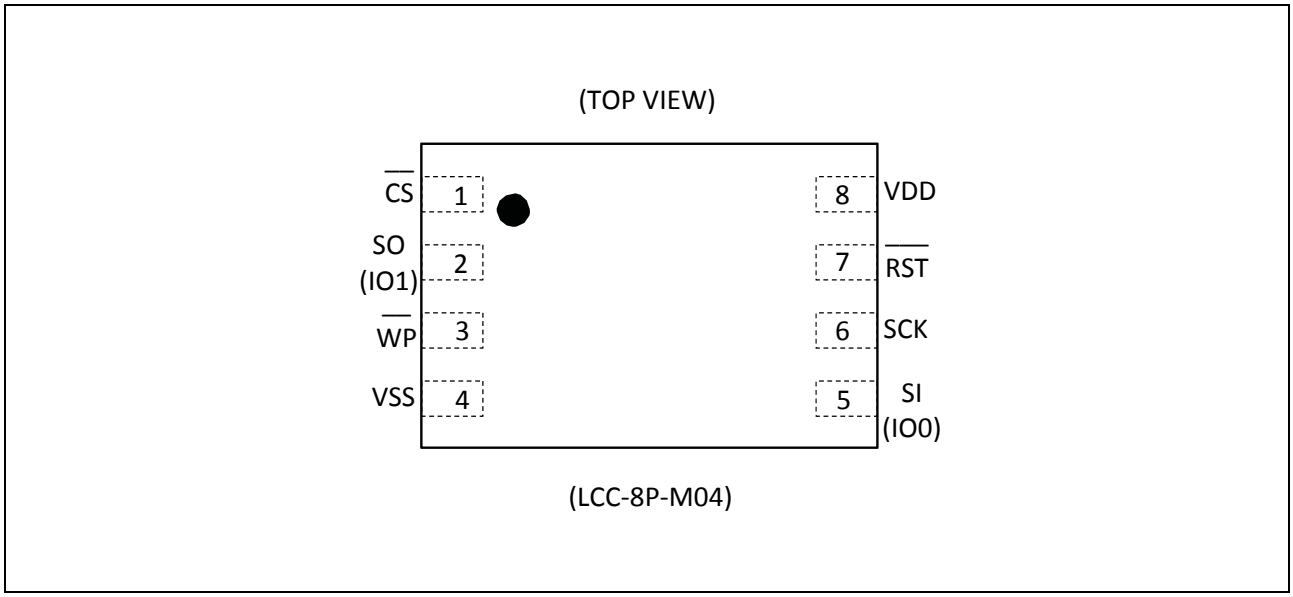
■ PIN ASSIGNMENT

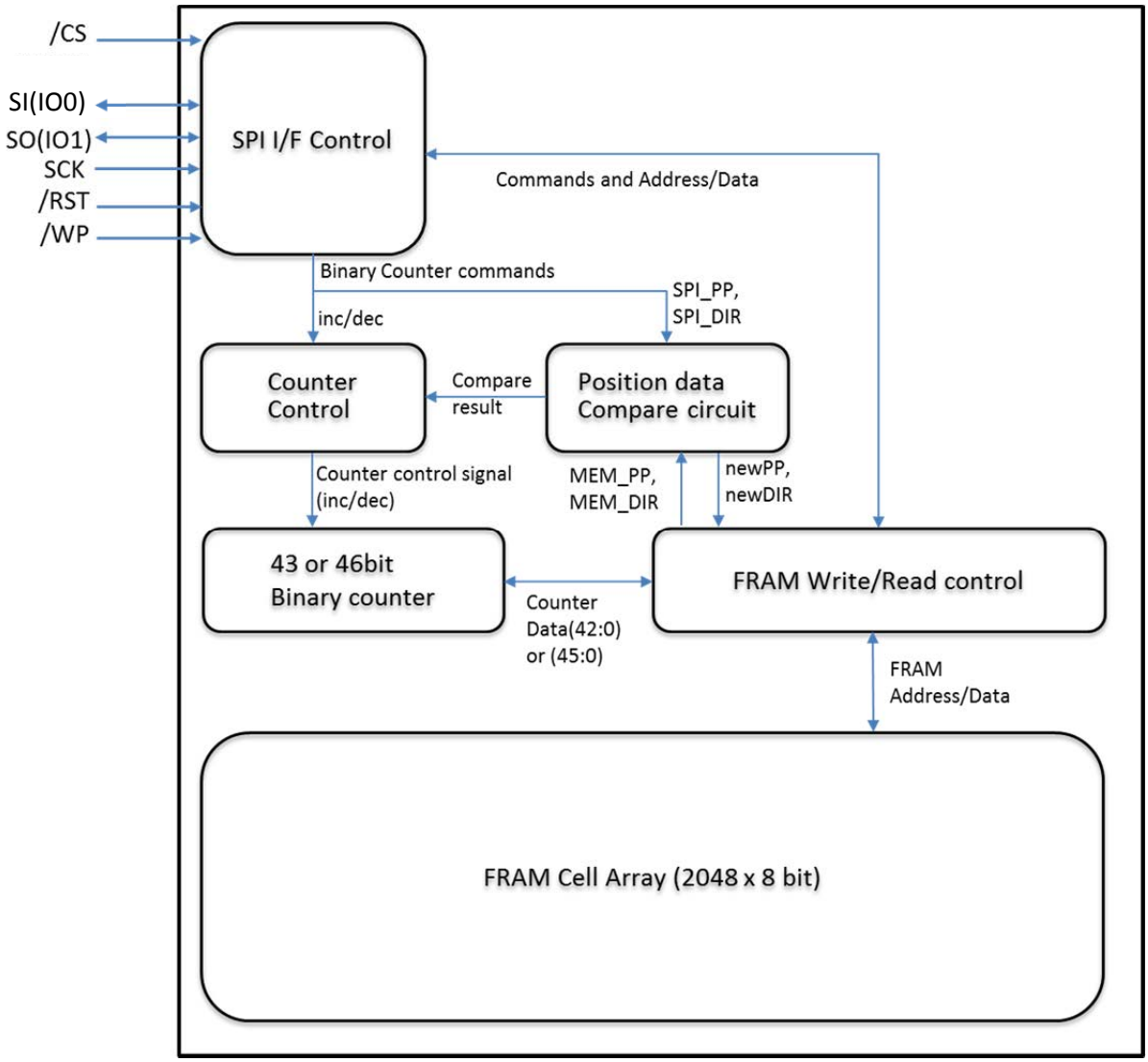


■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to activate the device. When $\overline{CS}$ is the “H” level, device is in deselect (standby) status and SO/SI become High-Z. Inputs from other pins are ignored at this time. When $\overline{CS}$ is the “L” level, device is in select (active) status. $\overline{CS}$ has to be the “L” level before inputting op-code.
3	$\overline{WP}$	Write Protect pin This is an input pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in relation with $\overline{WP}$ and WPEN bit of the status register. See “■WRITING PROTECT” for detail.
7	$\overline{RST}$	Reset pin This is an input pin to reset the device internally. When $\overline{RST}$ is the "L" level, the interface is inactive and the SPI state machine is reset. $\overline{RST}$ pin need to be "L" at power on.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. Inputs are latched synchronously to the rising edge, Outputs occur synchronously to the falling edge.
5	SI (IO0)	Serial Data Input pin (Serial Data Input Output 0) This inputs op-code, addresses or writing data and outputs reading data. This is High-Z during standby.
2	SO (IO1)	Serial Data Output pin (Serial Data Input Output 1) This outputs reading data or status register and inputs addresses or writing data. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

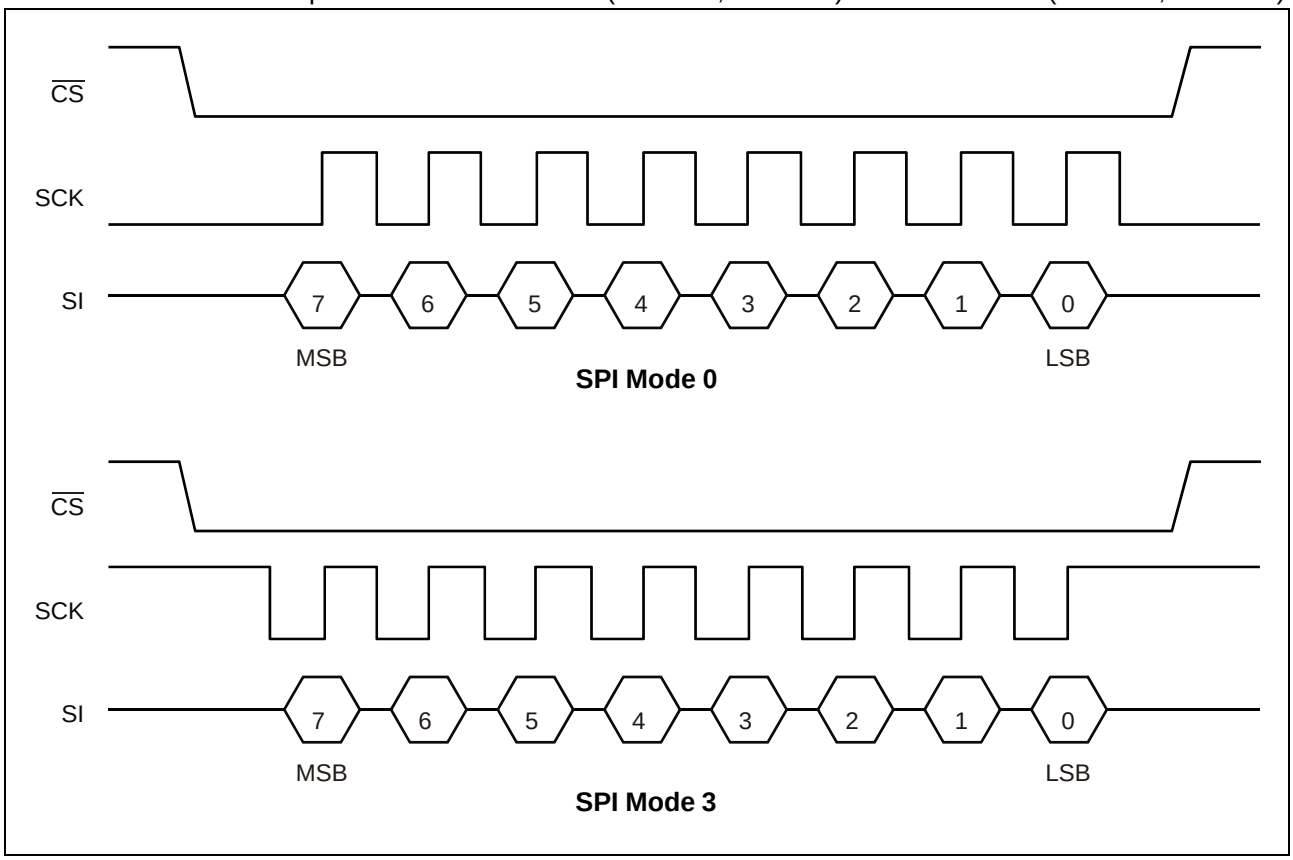
(*)When using Dual SPI instructions, the SI and SO pins become bidirectional IO0 and IO1 pins.

■ BLOCK DIAGRAM



■ SPI MODE

MB85RDP16LX corresponds to the SPI mode 0 (CPOL=0, CPHA=0) and SPI mode 3 (CPOL=1, CPHA=1).



■ SERIAL PERIPHERAL INTERFACE (SPI)

• Standard SPI

MB85RDP16LX works as a slave of SPI. Standard SPI uses the SI serial input pin to write op-code, addresses or data to the device on the rising edge of SCK. The SO serial output pin is used to read data or status register from the device on the falling edge of SCK.

• Dual SPI

MB85RDP16LX supports Dual SPI mode using the “Read Dual I/O (RDIO, B3h)” and “Write Dual I/O (WDIO, B2h)” op-code. When using Dual SPI op-code, the SI and SO pins become bidirectional IO0 and IO1 pins.

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (see "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command and WDIO command (see "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. At the rising edge of $\overline{CS}$ after WRSR command recognition. At the rising edge of $\overline{CS}$ after WRITE command recognition. At the rising edge of $\overline{CS}$ after WDIO command recognition.
0	0	This is a bit fixed to "0".

■ OP-CODE

MB85RDP16LX accepts 7 kinds of conventional command (WREN to RDID) and 12 kinds of enhanced command (RDIO to WRTSd) specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command is not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110B
WRDI	Reset Write Enable Latch	0000 0100B
RDSR	Read Status Register	0000 0101B
WRSR	Write Status Register	0000 0001B
READ	Read Memory Code	0000 0011B
WRITE	Write Memory Code	0000 0010B
RDID	Read Device ID	1001 1111B
RDIO	Read Dual I/O	1011 0011B
WDIO	Write Dual I/O	1011 0010B
POS0	Set SPI_DIR&SPI_PP = 00	0011 0000B
POS1	Set SPI_DIR&SPI_PP = 01	0011 0001B
POS2	Set SPI_DIR&SPI_PP = 10	0011 0010B
POS3	Set SPI_DIR&SPI_PP = 11	0011 0011B
DIBC	Directly Increment Binary Counter (+1)	0011 1100B
DDBC	Directly Decrement Binary Counter (-1)	0011 1110B
RDTSs	Read from address 0x000 decoded by a dedicated function, Single SO	0011 1000B
RDTSd	Read from address 0x000 decoded by a dedicated function, Dual IO	0111 1000B
WRTSs	Write from address 0x000 encoded by a dedicated function, Single SI	0011 1111B
WRTSd	Write from address 0x000 encoded by a dedicated function, Dual IO	0111 1111B

Notes

1-1. Standard SPI Input Address (2bytes)
SI = X, X, X, X, X, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0
(Upper 5bit = any)

1-2. Dual SPI Input Address (2bytes)
IO0 = X, X, A9, A7, A5, A3, A1, X
IO1 = X, X, A10, A8, A6, A4, A2, A0
(Upper 4bit and lower 1bit = any)

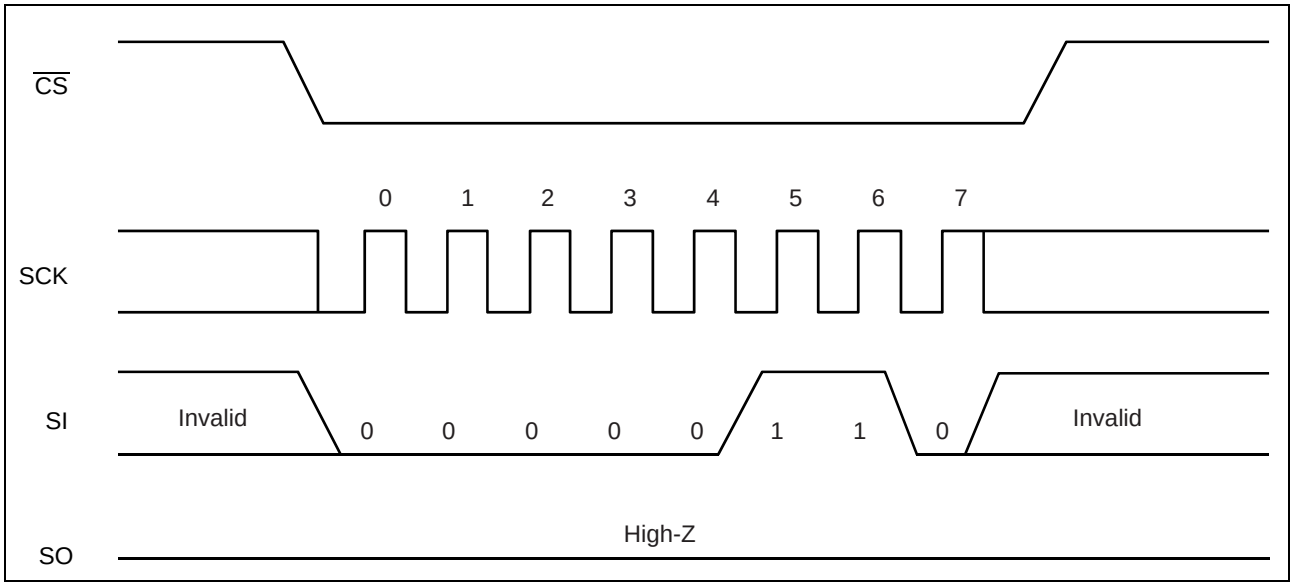
2-1. Standard SPI I/O Data
SI (or SO) = (D7, D6, D5, D4, D3, D2, D1, D0)

2-2. Dual SPI I/O Data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

■ COMMAND

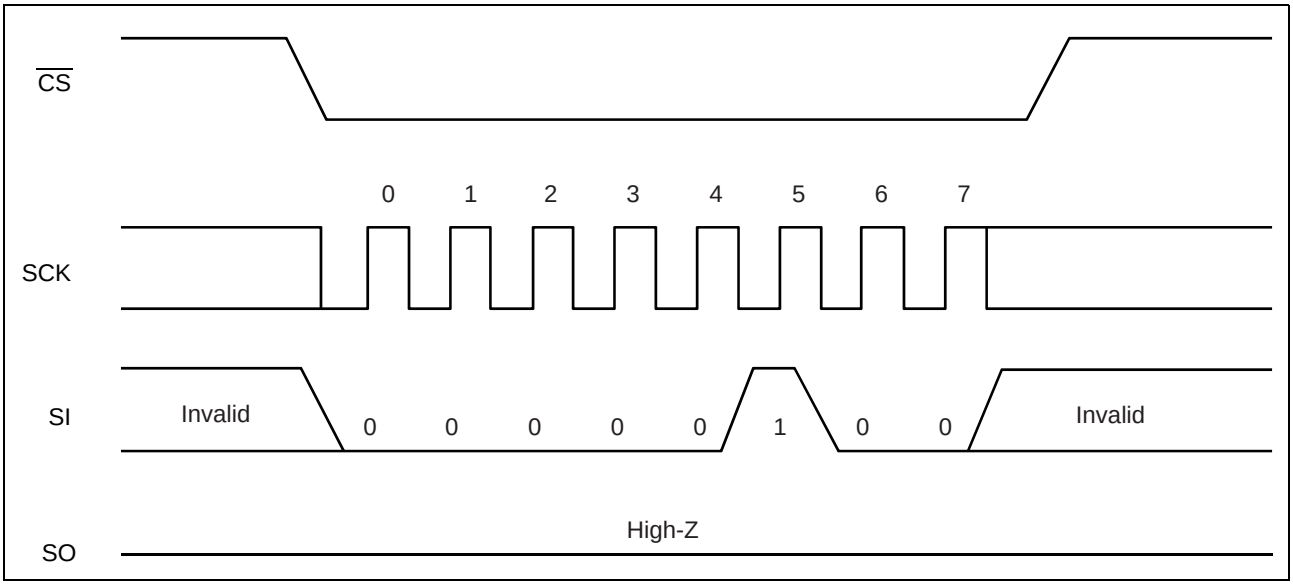
• WREN

The WREN command sets WEL (Write Enable Latch). WEL shall be set with the WREN command before writing operation (WRSR command, WRITE command and WDIO command).



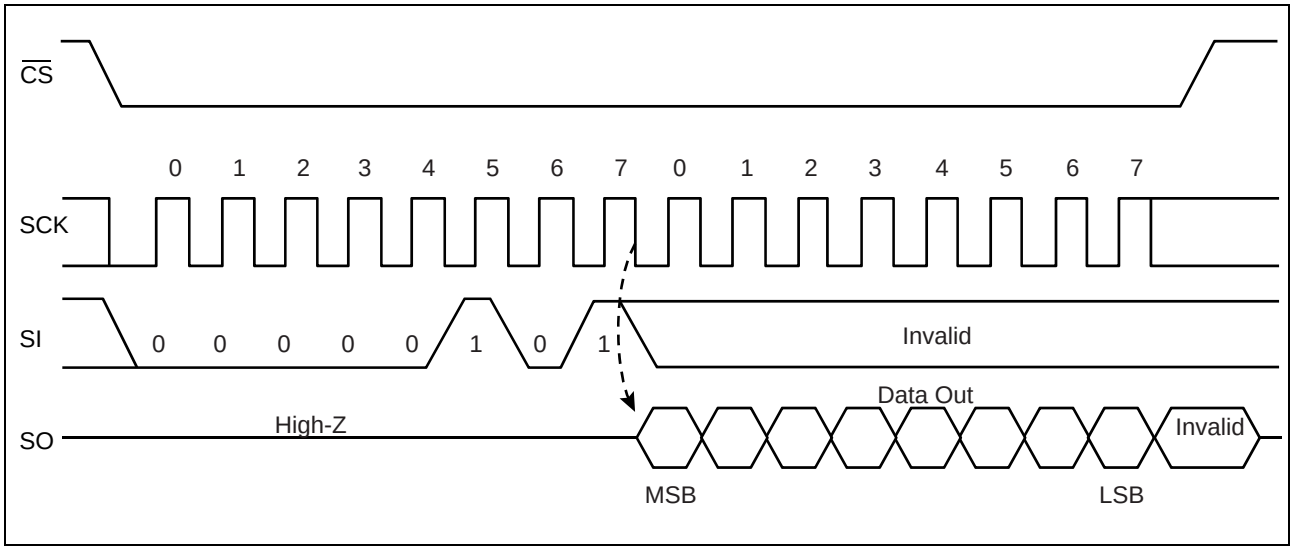
• WRDI

The WRDI command resets WEL (Write Enable Latch). Writing operation (WRITE command, WRSR command and WDIO command) are not performed when WEL is reset.



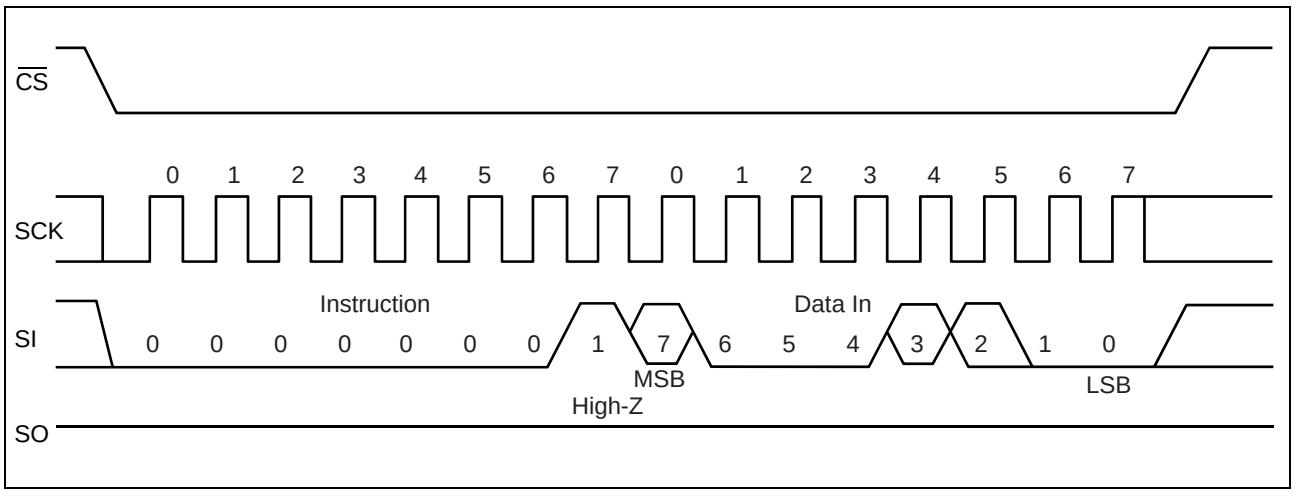
• **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.



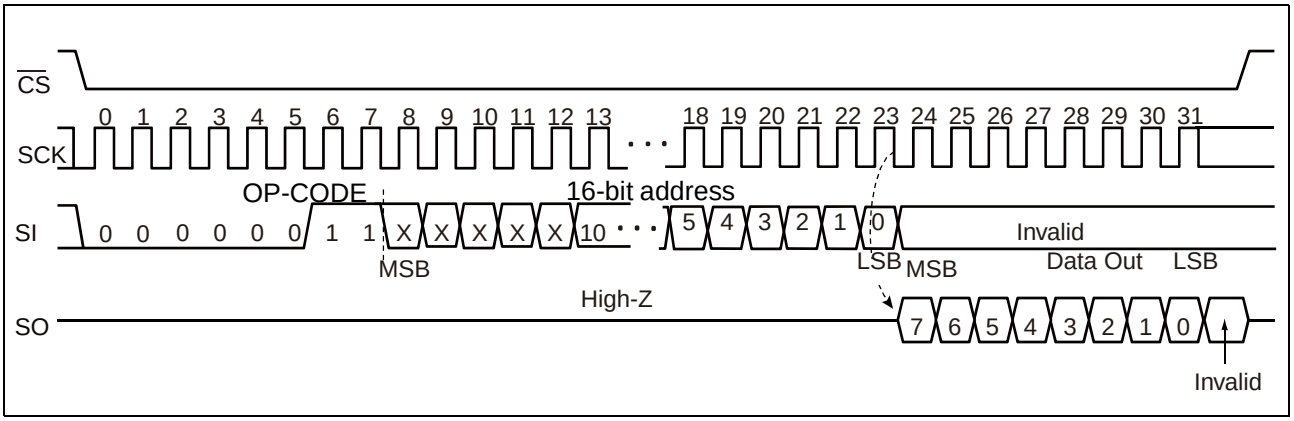
• **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value corresponding to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. The $\overline{WP}$ signal level shall be fixed before performing the WRSR command, and not be changed until the end of command sequence.



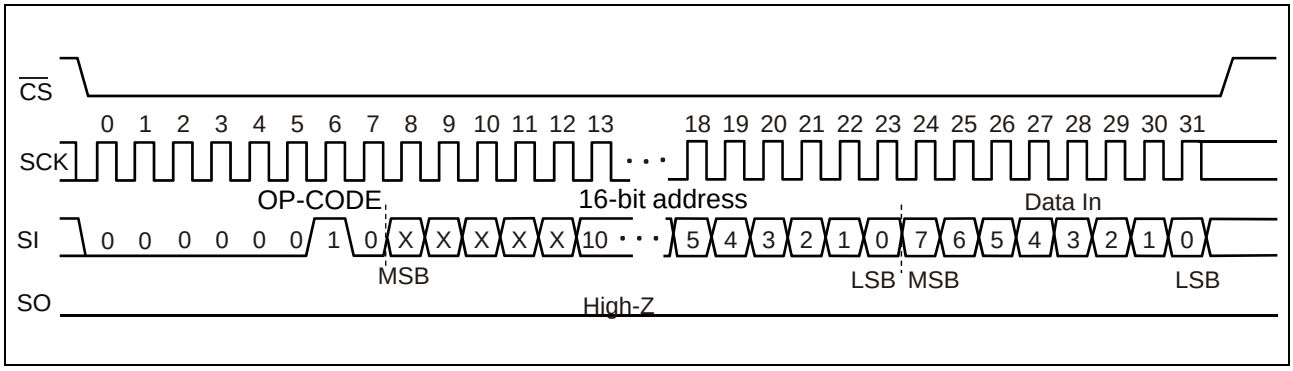
• **READ**

The READ command reads FRAM memory cell array data. READ op-code and arbitrary 16 bits address are input to SI. The 5-bit upper address bits are ignored. Then, 8 clock cycles are input to SCK. SO outputs 8-bit data synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



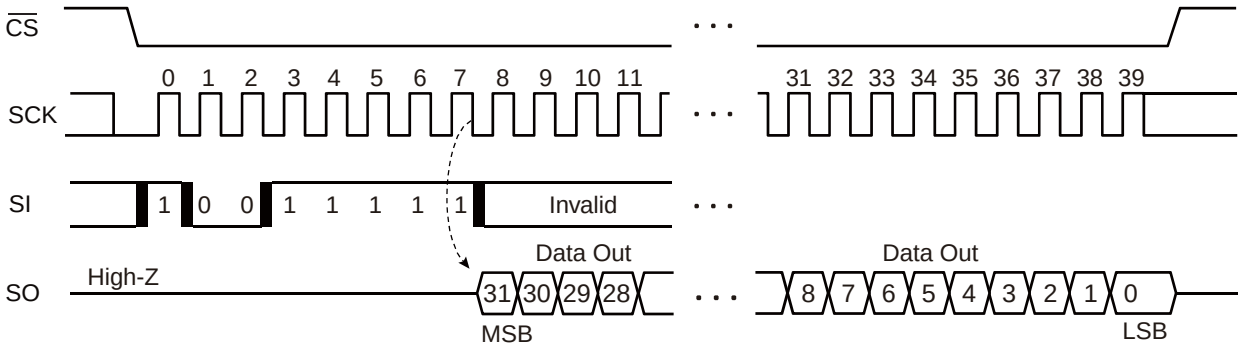
• **WRITE**

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The 5-bit upper address bit is ignored. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.



• **RDID**

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32 clock cycles are input to SCK. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. The output order is Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen.



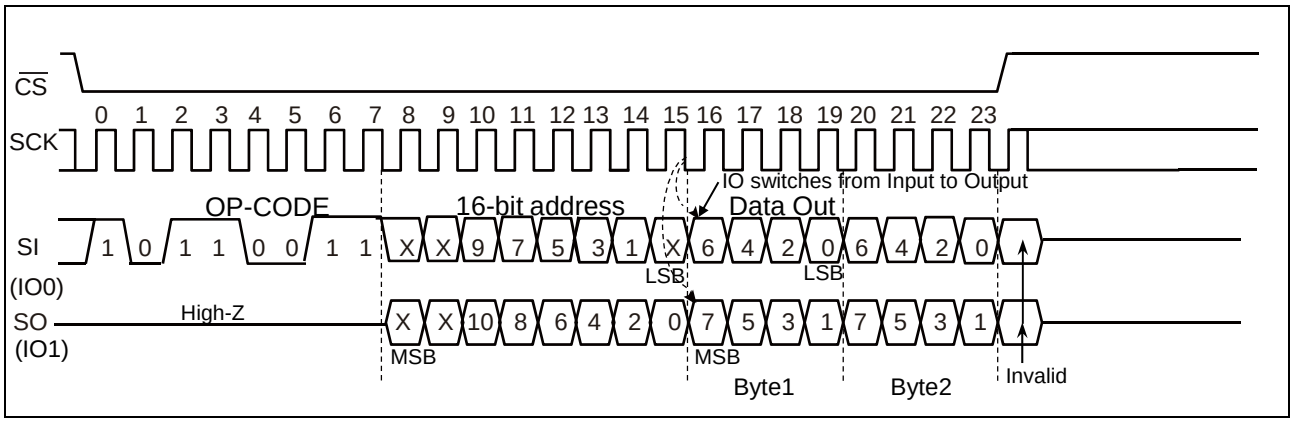
	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	$7F_H$	

	Proprietary use			**Density**					**Hex**	
Product ID (1st Byte)	0	0	1	0	0	0	0	1	21_H	Density: 00001_B = 16kbit

	Proprietary use								**Hex**	
Product ID (2nd Byte)	0	1	0	0	0	1	0	1	45_H	

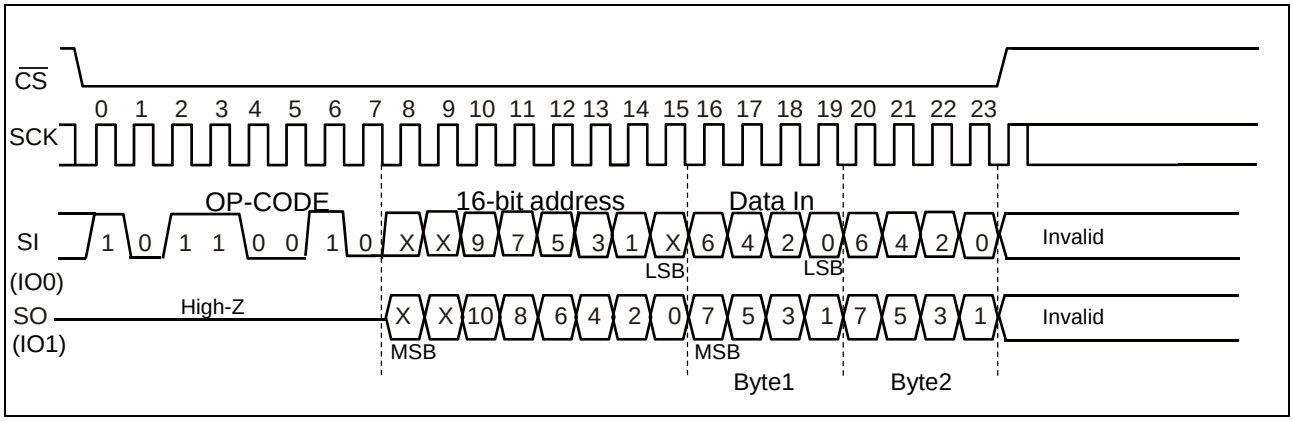
• **RDIO**

The RDIO command reads FRAM memory cell array data. RDIO op-code is input to SI(IO0). The 6 even address bits (A10, A8, A6, A4, A2, A0) of arbitrary 16 bits address are input to SO(IO1) and the 5 odd address bits (A9, A7, A5, A3, A1) are input to SI(IO0). The other address bits are ignored. Then, 4 clock cycles are input to SCK. SO(IO1) outputs 4 odd data bits (D7, D5, D3, D1) synchronously to the falling edge of SCK and SI(IO0) outputs 4 even data bits (D6, D4, D2, D0) as well. When $\overline{CS}$ is risen, the RDIO command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 4 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



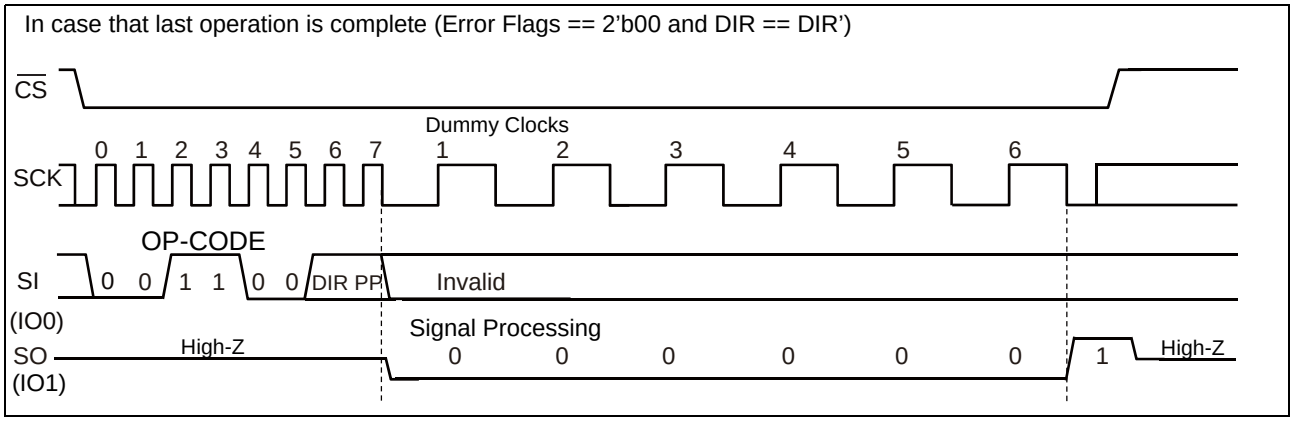
• **WDIO**

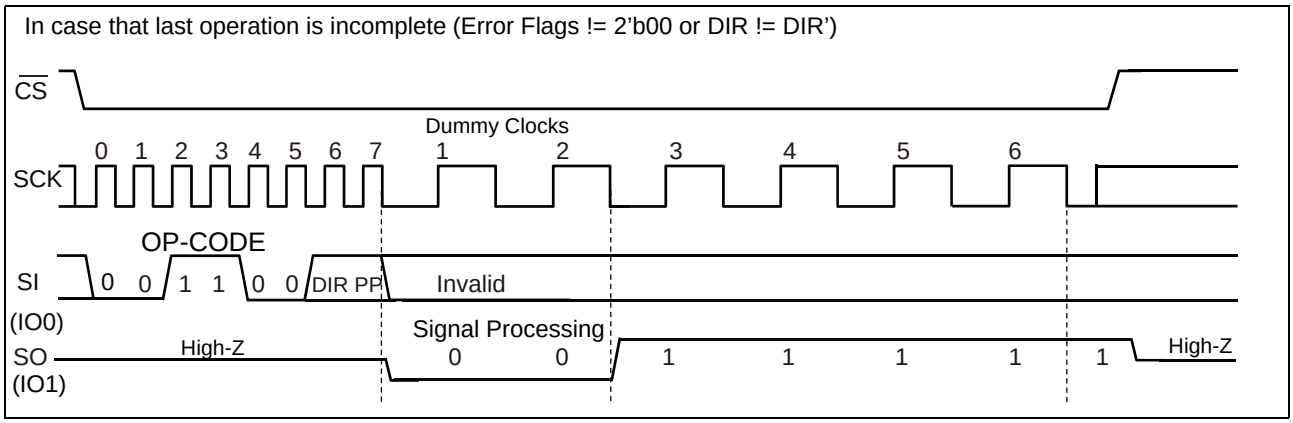
The WDIO command writes data to FRAM memory cell array. WDIO op-code is input to SI(IO0). The 6 even address bits (A10, A8, A6, A4, A2, A0) of arbitrary 16 bits address are input to SO(IO1) and the 5 odd address bits (A9, A7, A5, A3, A1) are input to SI(IO0). The other address bits are ignored. When the 4 odd writing data bits (D7, D5, D3, D1) are input to SO(IO1) and the 4 even writing data bits (D6, D4, D2, D0) are input to SI(IO0), they are written to FRAM memory cell array. Risen $\overline{CS}$ will terminate the WDIO command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.



• **POS0/POS1/POS2/POS3**

The POS0, POS1, POS2 and POS3 commands compare the old position data, which is stored in FRAM, with the new position data, which is input as the lowest 2 bits of the op-code. The comparing result decides if the 43-bit binary counter is incremented or decremented. The binary counter operation is accomplished by adding 6 dummy clocks after the 8-bit op-code. The frequency of the dummy clocks needs less than f_{DCK} (see “2. AC Characteristics”). These commands automatically read 48-bit FRAM cell array data containing position data, binary counter data and error flags from the address “000_H” (see “■ MEMORY MAP for POS0/1/2/3”), calculate them by the 43-bit binary counter and overwrite them to the address “000_H” during the 6 dummy clocks. These 48-bit data are encoded by a dedicated function and stored in FRAM cell array, therefore the specified commands (RDTSs/RDTSd/WRTSs/WRTSd) are necessary to read/write the 48-bit data related to the binary counter. SO continues to output low level during the binary counter operation and turns the output to high level after 6th dummy clock falls. It judges if last operation is complete or not at 2nd dummy clock using 2-bit Error Flags and 2 copies of the DIR bit. If last operation is incomplete, SO continues to output low level only until the 2nd dummy clock falls because the operation stops at the 2nd dummy clock.



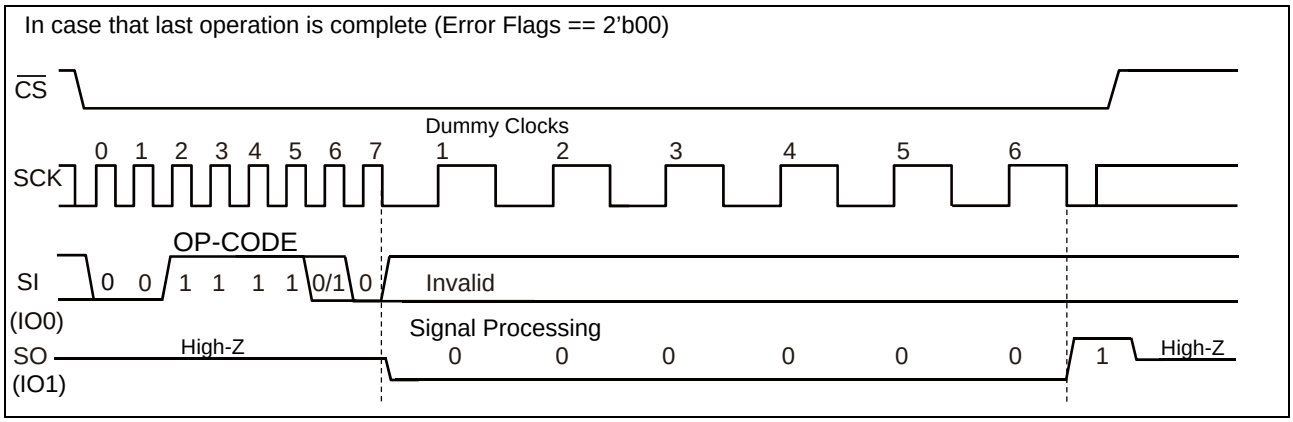


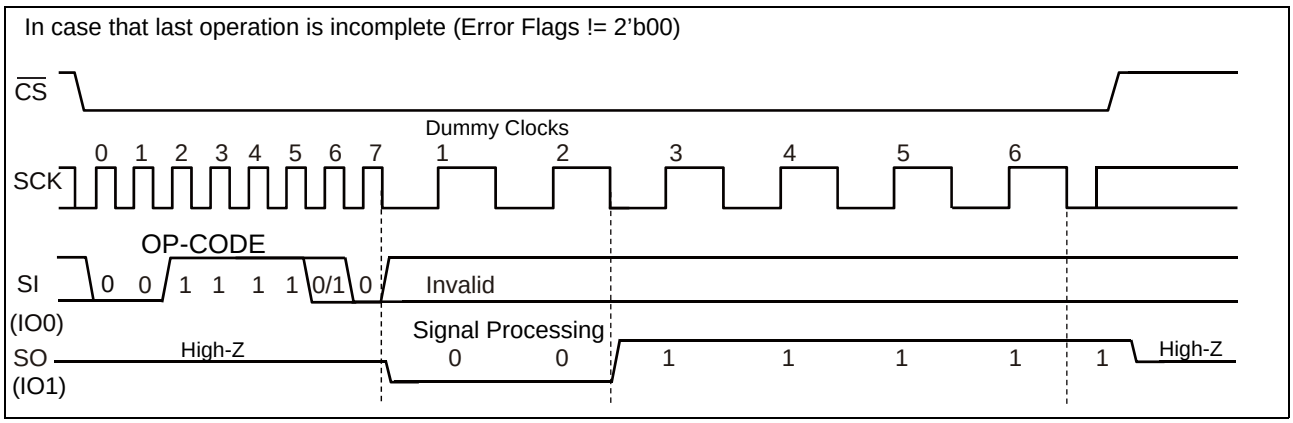
Position data comparison table

old (DIR, PP)	new (DIR, PP)	Binary counter operation
0, 1	0, 0	+1
1, 1	0, 0	+1
1, 0	0, 0	+1
1, 1	0, 1	+1
1, 0	1, 1	-1
0, 0	1, 1	-1
0, 1	1, 1	-1
0, 0	1, 0	-1
others	others	0

• **DIBC/DDBC**

The DIBC command increments the 46-bit binary counter by 1 and the DDBC command decrements it by 1. The binary counter operation is accomplished by adding 6 dummy clocks after the 8-bit op-code. The frequency of the dummy clocks needs less than f_{DCK} (see “2. AC Characteristics”). These commands automatically read 48-bit FRAM cell array data containing binary counter data and error flags from the address “000_H” (see “■ MEMORY MAP for DIBC/DDBC”), calculate them by the 46-bit binary counter and overwrite them to the address “000_H” during 6 dummy clocks. These 48-bit data are encoded by a dedicated function and stored in FRAM cell array, therefore the specified commands (RDTSs/RDTSd/WRTSs/WRTSd) are necessary to read/write the 48-bit data related to the binary counter. SO continues to output low level during the binary counter operation and turns the output to high level after the 6th dummy clock falls. It judges if last operation is complete or not at the 2nd dummy clock using 2-bit Error Flags. If last operation is incomplete, SO continues to output low level only until the 2nd dummy clock falls because the operation stops at the 2nd dummy clock.



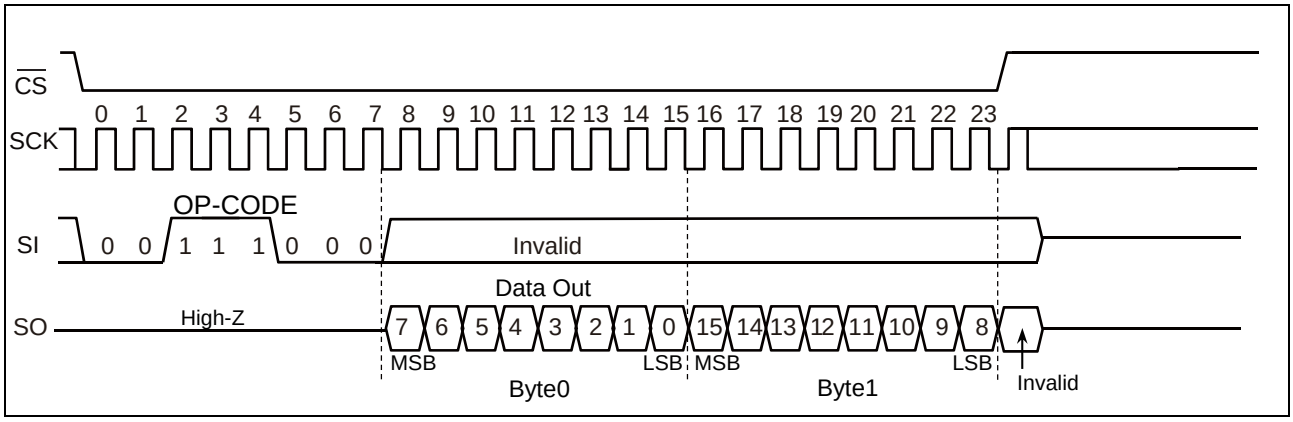


OP-CODE table for direct binary counter operation

Name	OP-CODE (8-bit)	Binary counter operation
DIBC	$0011\ 1100_B$	+1
DDBC	$0011\ 1110_B$	-1

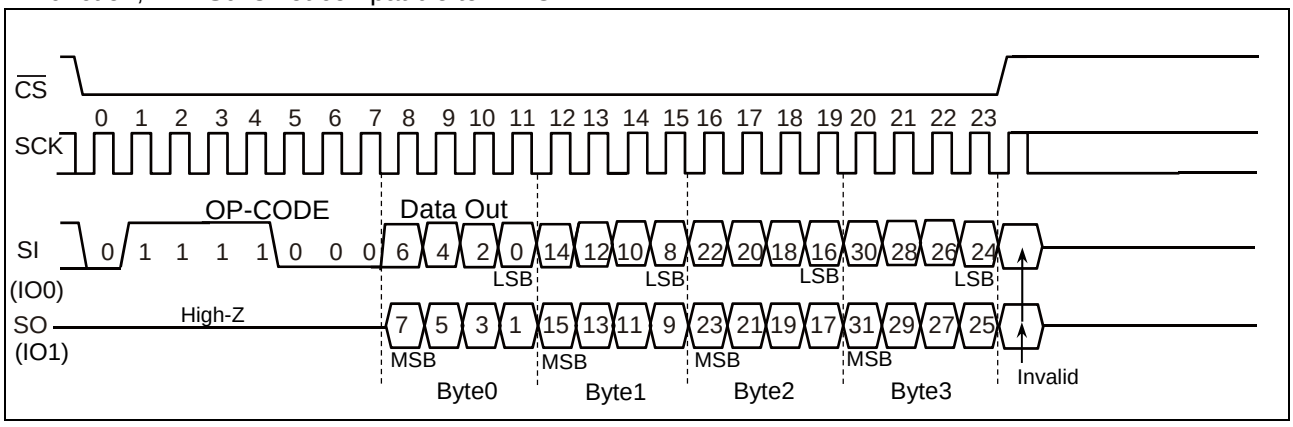
• **RDTSs** (Single SO)

The RDTSs command can read the data related to the binary counter from FRAM memory cell array (see "■ MEMORY MAP"). RDTSs op-code is input to SI. No address bits are input. 8 clock cycles are input to SCK after 8-bit op-code. SO outputs 8-bit data decoded by a dedicated function from the starting address "000_H" synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the RDTSs command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. Because of the dedicated function, RDTSs is not compatible to READ.



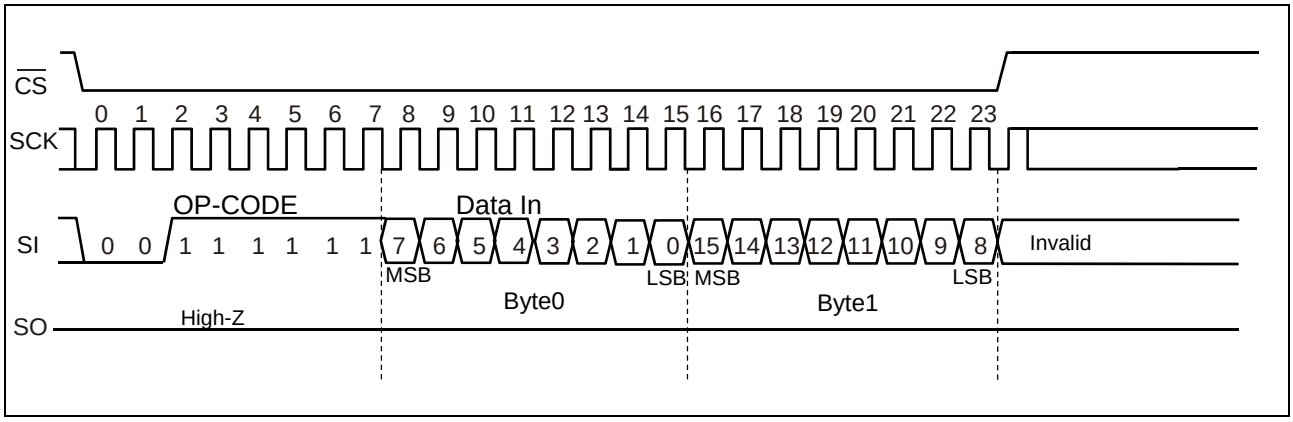
• **RDTSd** (Dual IO)

The RDTSd command can read the data related to the binary counter from FRAM memory cell array (see "■ MEMORY MAP"). RDTSd op-code is input to SI(IO0). No address bits are input. 4 clock cycles are input to SCK after 8-bit op-code. SO(IO1) outputs the 4 odd data bits (D7, D5, D3, D1) and SI(IO0) outputs the 4 even data bits (D6, D4, D2, D0) decoded by a dedicated function from the starting address "000_H" synchronously to the falling edge of SCK. When $\overline{CS}$ is risen, the RDTSd command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 4 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. Because of the dedicated function, RDTSd is not compatible to RDIO.



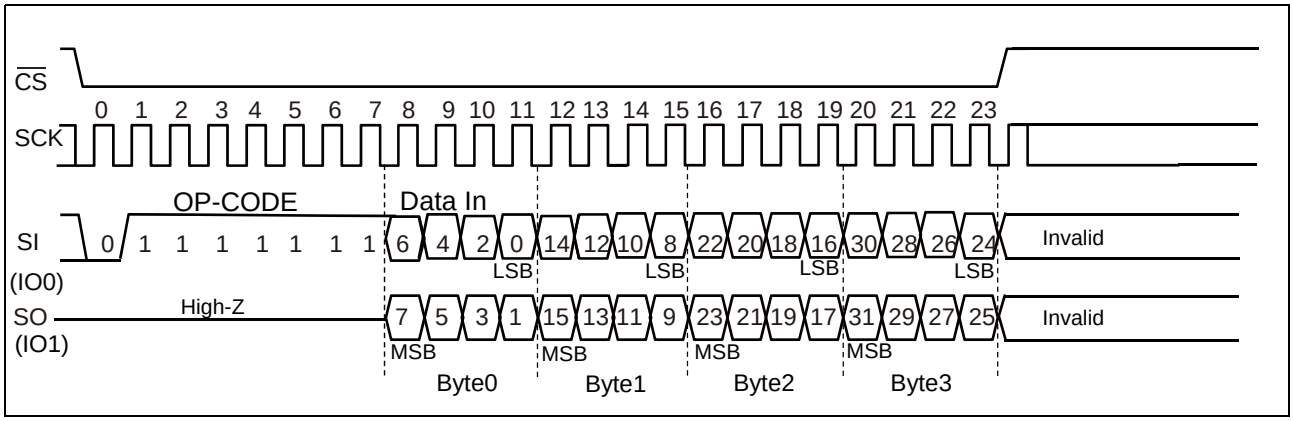
• **WRTSs** (Single SO)

The WRTSs command can write the data related to the binary counter to FRAM memory cell array (see "■ MEMORY MAP"). WRTSs op-code is input to SI. No address bits are input. When 8 writing data bits are input after the 8-bit op-code, data is encoded by a dedicated function and written to FRAM memory cell array from the starting address "000H". Risen $\overline{CS}$ will terminate the WRTSs command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely. Because of the dedicated function, WRTSs is not compatible to WRITE.



• **WRTSd** (Dual IO)

The WRTSd command can write the data related to the binary counter to FRAM memory cell array (see "■ MEMORY MAP"). WRTSd op-code is input to SI(IO0). No address bits are input. When the 4 odd writing data bits (D7, D5, D3, D1) are input to SO(IO1) and 4 even writing data bits (D6, D4, D2, D0) are input to SI(IO0) after the 8-bit op-code, they are encoded by a dedicated function and written to FRAM memory cell array from the starting address "000H". Risen $\overline{CS}$ will terminate the WRTSd command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely. Because of the dedicated function, WRTSd is not compatible to WDIO.



■ BLOCK PROTECT

Writing protect block for WRITE and WDIO commands are configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	600_H to $7FF_H$ (upper 1/4)
1	0	400_H to $7FF_H$ (upper 1/2)
1	1	000_H to $7FF_H$ (all)

■ WRITING PROTECT

Writing operation of WRITE, WDIO and WRSR commands are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Note: writing operation of POS0/1/2/3, DIBC/DDBC and WRTSs/WRTSd commands are not protected.

■ MEMORY MAP for POS0/1/2/3

In case of using POS0/1/2/3 commands, 43-bit binary counter data (Counter(0) to Counter(42)), 3-bit position data (PP, DIR and DIR') and 2-bit error flag (Eflag(0) and Eflag(1)) are written to FRAM memory cell array from the address "000H" to the address "005H".

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
000H	Counter(5)	Counter(4)	Counter(3)	Counter(2)	Counter(1)	Counter(0)	DIR	PP
001H	Counter(13)	Counter(12)	Counter(11)	Counter(10)	Counter(9)	Counter(8)	Counter(7)	Counter(6)
002H	Counter(21)	Counter(20)	Counter(19)	Counter(18)	Counter(17)	Counter(16)	Counter(15)	Counter(14)
003H	Counter(29)	Counter(28)	Counter(27)	Counter(26)	Counter(25)	Counter(24)	Counter(23)	Counter(22)
004H	Counter(37)	Counter(36)	Counter(35)	Counter(34)	Counter(33)	Counter(32)	Counter(31)	Counter(30)
005H	Eflag(1)	Eflag(0)	DIR'	Counter(42)	Counter(41)	Counter(40)	Counter(39)	Counter(38)

Note: the data of this memory map stored in FRAM memory cell array are encoded by a dedicated function and also can be overwritten by WRTSs/WRTSd command and so on.

■ ERROR FLAG for POS0/1/2/3

Unless 2-bit error flag (Eflag(1,0)) is "00", the binary counter operation stops.

Eflag(1,0)	Status
"00"	Last operation normally completed.
"01"	Counter underflow/overflow and binary counter function stopped. if counter(42:0) underflowed from 400_0000_0000H to 3FF_FFFF_FFFFH if counter(42:0) overflowed from 3FF_FFFF_FFFFH to 400_0000_0000H
"10"	ECC error is detected but could not be corrected.
"11"	Last operation did not complete and counter function stopped.

Note: The above values of Eflag(1,0) are logical data. The specified commands (RDTSs/RDTSd) are necessary to read the values because they encoded by a dedicated function.

■ COUNTER VALUE UP/DOWN for POS0/1/2/3

The Eflag(1,0) are set to "01" when the max value 3FF_FFFF_FFFFH is increased by one and then the new value becomes 400_0000_0000H or when the min value 400_0000_0000H is decreased by one and then the new value becomes 3FF_FFFF_FFFFH. Therefore, next binary counter operation stops after the counter overflowed.

Counter Value (hex)	Counter Value (decimal)	
	sign	mantissa
3FF FFFF FFFF	+	$2^{42}-1$
3FF FFFF FFFE	+	$2^{42}-2$
3FF FFFF FFFD	+	$2^{42}-3$
…	+	…
000 0000 0002	+	2
000 0000 0001	+	1
000 0000 0000	+	0
7FF FFFF FFFF	-	1
7FF FFFF FFFE	-	2
…	-	…
400 0000 0002	-	$2^{42}-2$
400 0000 0001	-	$2^{42}-1$
400 0000 0000	-	2^{42}

■ MEMORY MAP for DIBC/DDBC

In case of using DIBC/DDBC commands, 46-bit binary counter data (Counter(0) to Counter(45)) and 2-bit error flag (Eflag(0) and Eflag(1)) are written to FRAM memory cell array from the address "000H" to the address "005H".

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
000H	Counter(7)	Counter(6)	Counter(5)	Counter(4)	Counter(3)	Counter(2)	Counter(1)	Counter(0)
001H	Counter(15)	Counter(14)	Counter(13)	Counter(12)	Counter(11)	Counter(10)	Counter(9)	Counter(8)
002H	Counter(23)	Counter(22)	Counter(21)	Counter(20)	Counter(19)	Counter(18)	Counter(17)	Counter(16)
003H	Counter(31)	Counter(30)	Counter(29)	Counter(28)	Counter(27)	Counter(26)	Counter(25)	Counter(24)
004H	Counter(39)	Counter(38)	Counter(37)	Counter(36)	Counter(35)	Counter(34)	Counter(33)	Counter(32)
005H	Eflag(1)	Eflag(0)	Counter(45)	Counter(44)	Counter(43)	Counter(42)	Counter(41)	Counter(40)

Note: the data of this memory map stored in FRAM memory cell array are encoded by a dedicated function and also can be overwritten by WRTSs/WRTSd command and so on.

■ ERROR FLAG for DIBC/DDBC

Unless 2-bit error flag (Eflag(1,0)) is "00", the binary counter operation stops.

Eflag(1,0)	Status
"00"	Last operation normally completed.
"01"	Counter underflow/overflow and binary counter function stopped. if counter(45:0) underflowed from 2000_0000_0000H to 1FFF_FFFF_FFFFH if counter(45:0) overflowed from 1FFF_FFFF_FFFFH to 2000_0000_0000H
"10"	ECC error is detected but could not be corrected.
"11"	Last operation did not complete and counter function stopped.

Note: The above values of Eflag(1,0) are logical data. The specified commands (RDTSs/RDTSd) are necessary to read the values because they need to be encoded by a dedicated function.

■ COUNTER VALUE UP/DOWN for DIBC/DDBC

The Eflag(1,0) are set to "01" when the max value 1FFF_FFFF_FFFFH is increased by one and then the new value becomes 2000_0000_0000H or when the min value 2000_0000_0000H is decreased by one and then the new value becomes 1FFF_FFFF_FFFFH. Therefore, next binary counter operation stops after the counter overflowed.

Counter Value (hex)	Counter Value (decimal)	
	sign	mantissa
1FFF FFFF FFFF	+	2^{45}-1
1FFF FFFF FFFE	+	2^{45}-2
1FFF FFFF FFFD	+	2^{45}-3
…	+	…
0000 0000 0002	+	2
0000 0000 0001	+	1
0000 0000 0000	+	0
3FFF FFFF FFFF	-	1
3FFF FFFF FFFE	-	2
…	-	…
2000 0000 0002	-	2^{45}-2
2000 0000 0001	-	2^{45}-1
2000 0000 0000	-	2^{45}

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 2.5	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5	V
Operation ambient temperature	T_A	− 40	+ 105	°C
Storage temperature	Tstg	− 55	+ 125	°C

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	1.65	1.8	1.95	V
Operation ambient temperature*2	T_A	− 40	—	+ 105	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	$\|I_{LI}\|$	$\overline{CS}$ = V_{DD}	—	—	1	µA
		$\overline{WP}$, SCK, SI = 0 V to V_{DD}	—	—	1	
Output leakage current	$\|I_{LO}\|$	SO = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{DD}	SCK = 15 MHz	—	—	0.7	mA
Standby current	I_{SB}	SCK = SI = $\overline{CS}$ = V_{DD}	—	1 (25°C)	11 (105°C) 6 (85°C)	µA
Input high voltage	V_{IH}	V_{DD} = 1.65 to 1.95 V	V_{DD} × 0.8	—	V_{DD} + 0.3	V
Input low voltage	V_{IL}	V_{DD} = 1.65 to 1.95 V	− 0.5	—	V_{DD} × 0.2	V
Output high voltage	V_{OH}	I_{OH} = −2 mA	V_{DD} − 0.5	—	V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 2 mA	V_{SS}	—	0.4	V

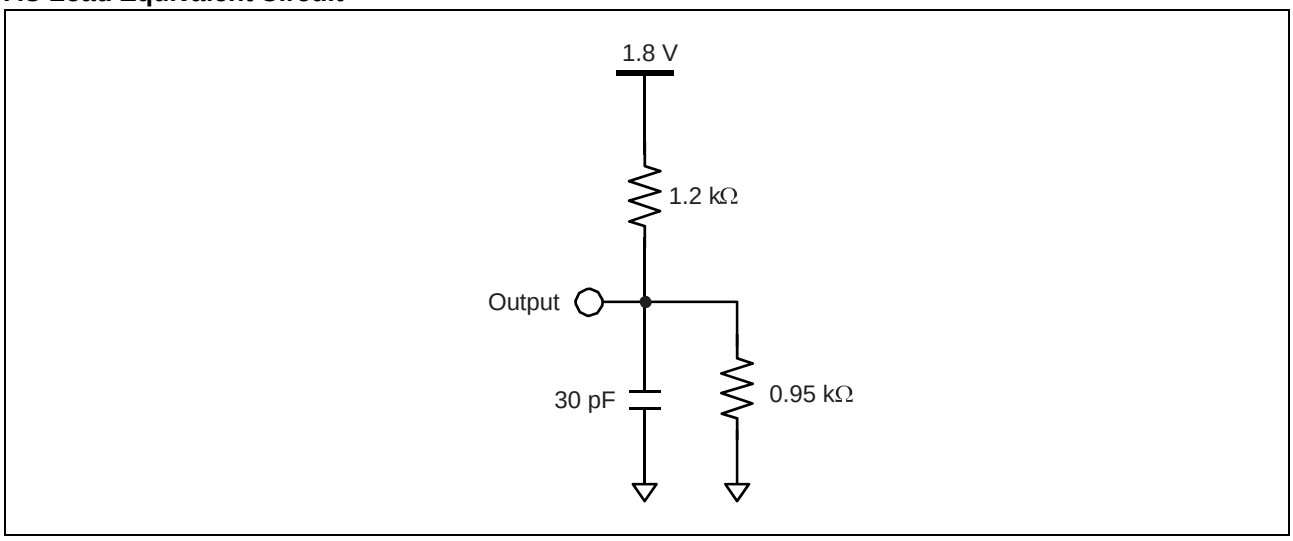
2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency for SPI	f_{CK}	—	15	MHz
Clock high time for SPI	t_{CH}	33	—	ns
Clock low time for SPI	t_{CL}	33	—	ns
SCK clock frequency for Dual SPI	f_{CK}	—	7.5	MHz
Clock high time for Dual SPI	t_{CH}	66	—	ns
Clock low time for Dual SPI	t_{CL}	66	—	ns
SCK clock frequency for the dummy clocks of POS0/1/2/3 or DIBC/DDBC commands (the interval between the commands < 3us)	f_{DCK}	—	2	MHz
SCK clock frequency for the dummy clocks of POS0/1/2/3 or DIBC/DDBC commands (the interval between the commands ≧ 3us)	f_{DCK}	—	5	MHz
Clock high time for the dummy clocks of POS0/1/2/3 or DIBC/DDBC commands	t_{CH}	50	—	ns
Clock low time for the dummy clocks of POS0/1/2/3 or DIBC/DDBC commands	t_{CL}	50	—	ns
Chip select set up time	t_{CSU}	10	—	ns
Chip select hold time	t_{CSH}	10	—	ns
Output disable time	t_{OD}	—	20	ns
Output data valid time	t_{ODV}	—	18	ns
Output hold time	t_{OH}	0	—	ns
Deselect time	t_{D}	30	—	ns
Data rising time	t_{R}	—	50	ns
Data falling time	t_{F}	—	50	ns
Data set up time	t_{SU}	5	—	ns
Data hold time	t_{H}	5	—	ns

AC Test Condition

Power supply voltage : 1.65 V to 1.95 V
Operation ambient temperature : − 40 °C to + 105 °C
Input voltage magnitude : 0.3 V to 1.65 V
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : VDD/2
Output judge level : VDD/2

AC Load Equivalent Circuit

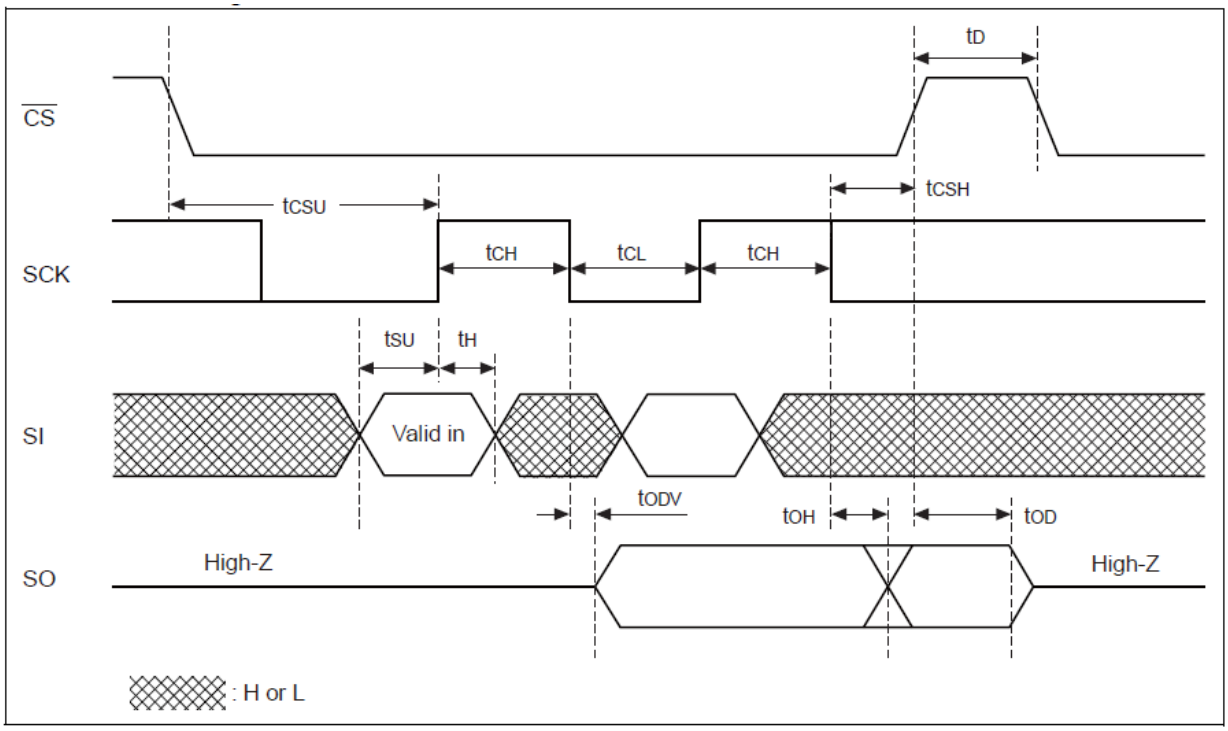


3. Pin Capacitance

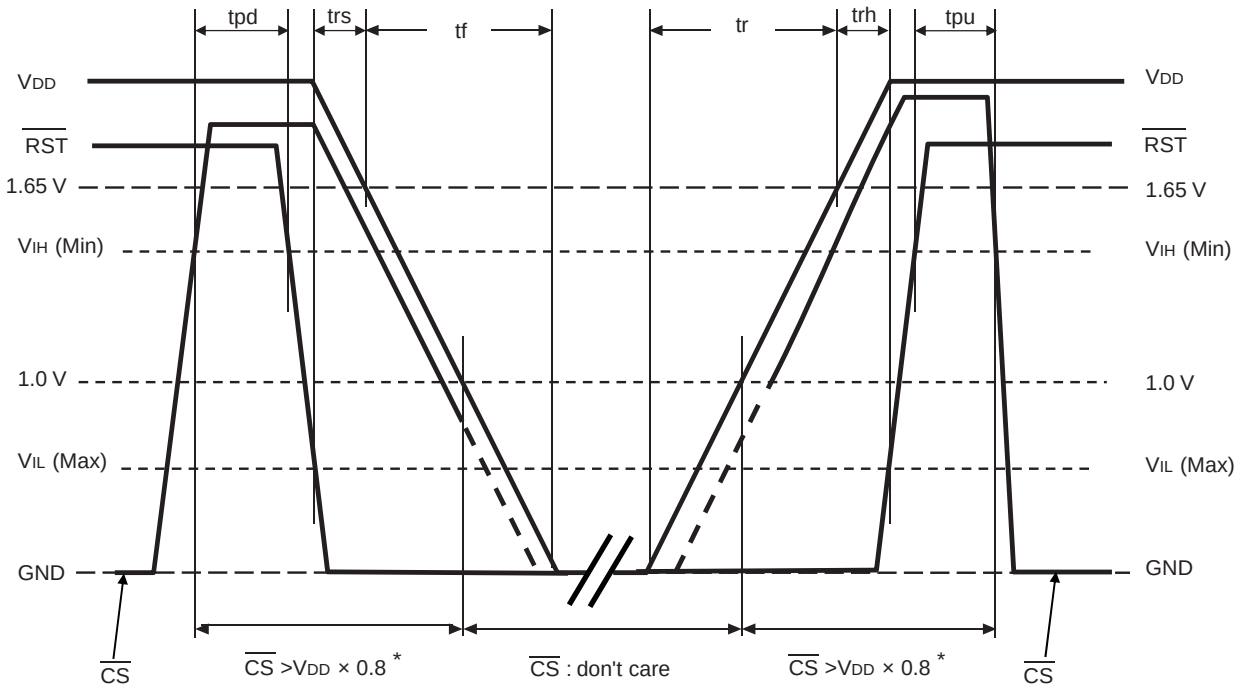
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Output capacitance	C_O	$V_{DD} = V_{IN} = V_{OUT} = 0$ V f = 1 MHz, $T_A = +25$ °C	—	4	pF
Input capacitance	C_I		—	4	pF

■ TIMING DIAGRAM

- **Serial Data Timing**



■ POWER ON/OFF SEQUENCE



* : $\overline{CS}$ (Max) < V_{DD} + 0.3 V

Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ and $\overline{RST}$ level hold time at power OFF	tpd	400	—	ns
$\overline{RST}$ high to first access start	tpu	1	—	µs
Power supply falling time	tf	3	—	µs
Power supply rising time	tr	3	—	µs
$\overline{RST}$ setup time to VDD(min) at power OFF	trs	0		µs
$\overline{RST}$ hold time after VDD(min) at power ON	trh	1		µs

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}	—	Times/byte	Operation Ambient Temperature T_A = + 105 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 105 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

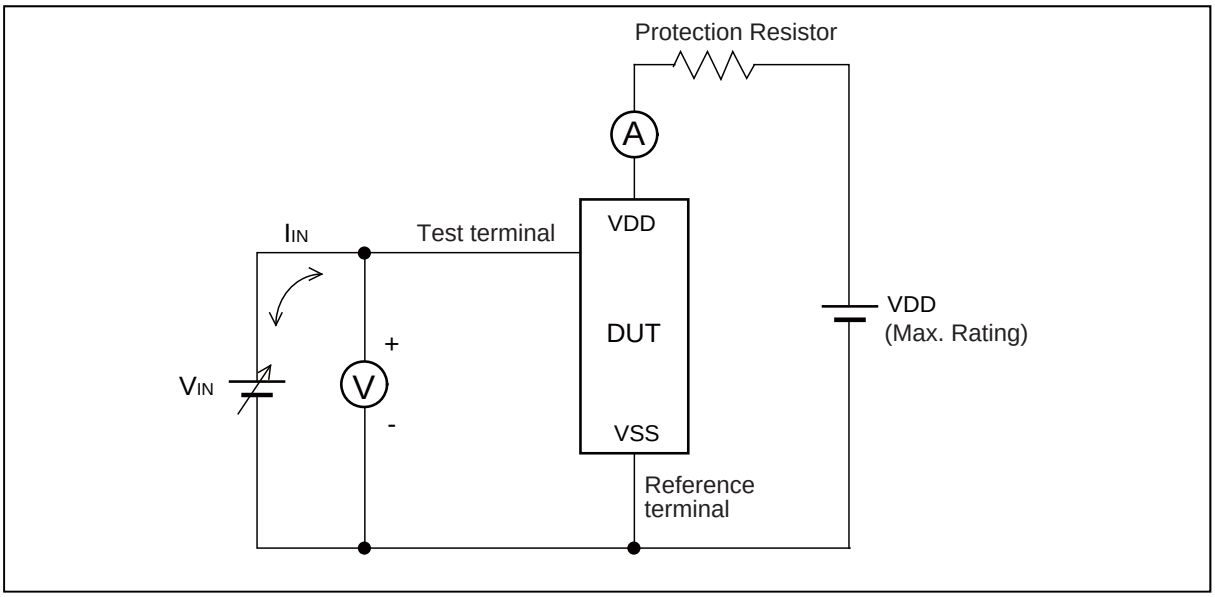
■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

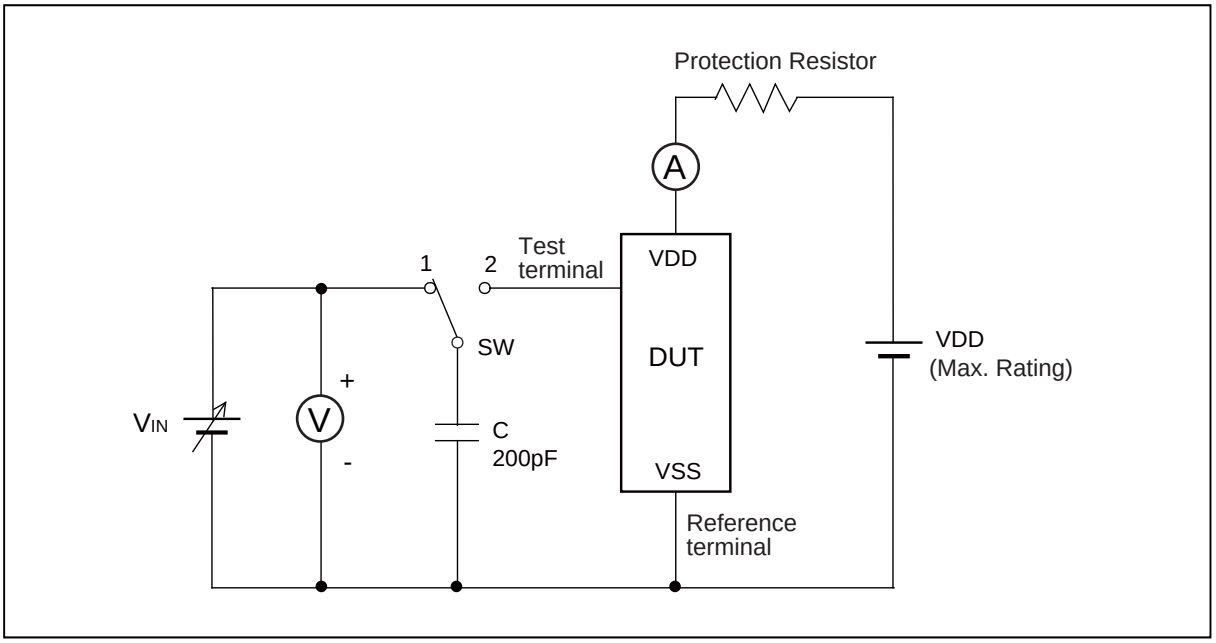
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RDP16LXPN-G-AMEWE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

• Current method of Latch-Up Resistance Test



Note: The voltage VIN is increased gradually and the current I_{IN} of 300 mA at maximum shall flow. Confirm the latch up does not occur under I_{IN} =±300 mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• **C-V method of Latch-Up Resistance Test**



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

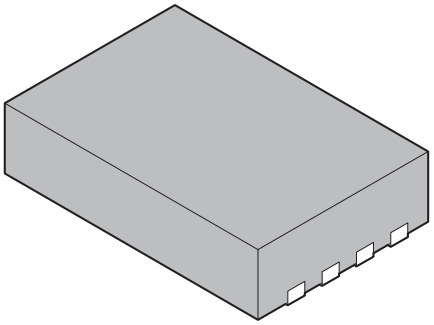
■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

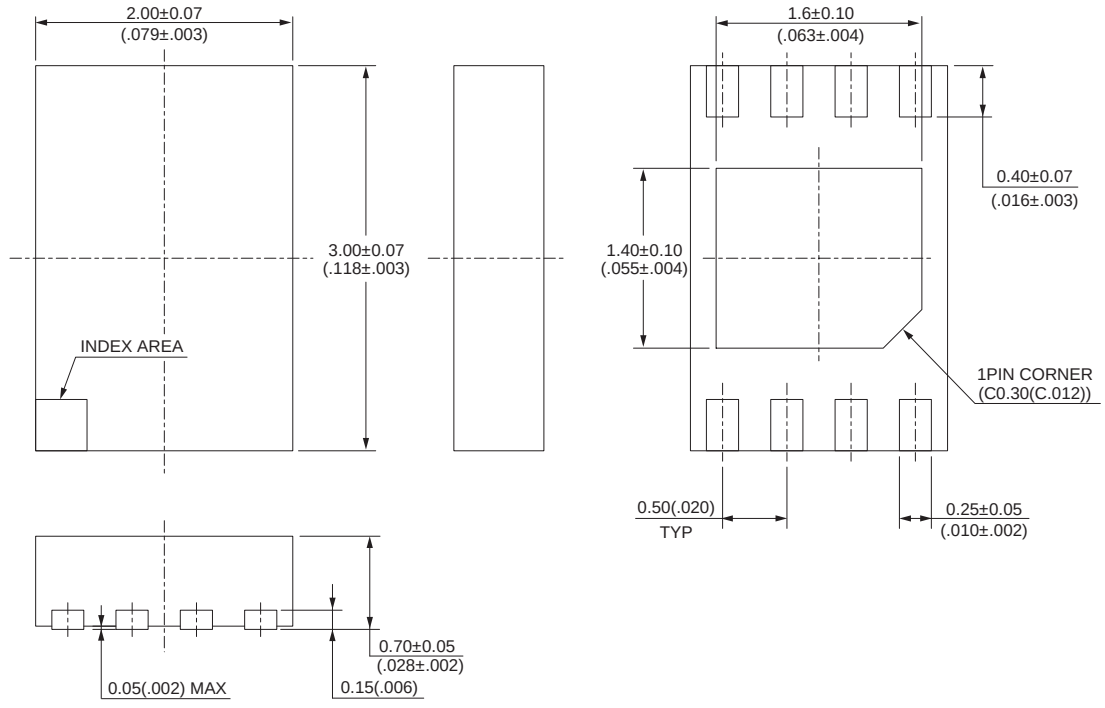
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RDP16LXPN-G-AMEWE1	8-pin, plastic SON (LCC-8P-M04)	Embossed Carrier tape	1500

■ PACKAGE DIMENSION

8-pin plastic SON		
	Lead pitch	0.5 mm
	Package width × package length	2.0 mm × 3.0 mm
	Sealing method	Plastic mold
	Mounting height	0.75 mm MAX
	Weight	0.015g
(LCC-8P-M04)		

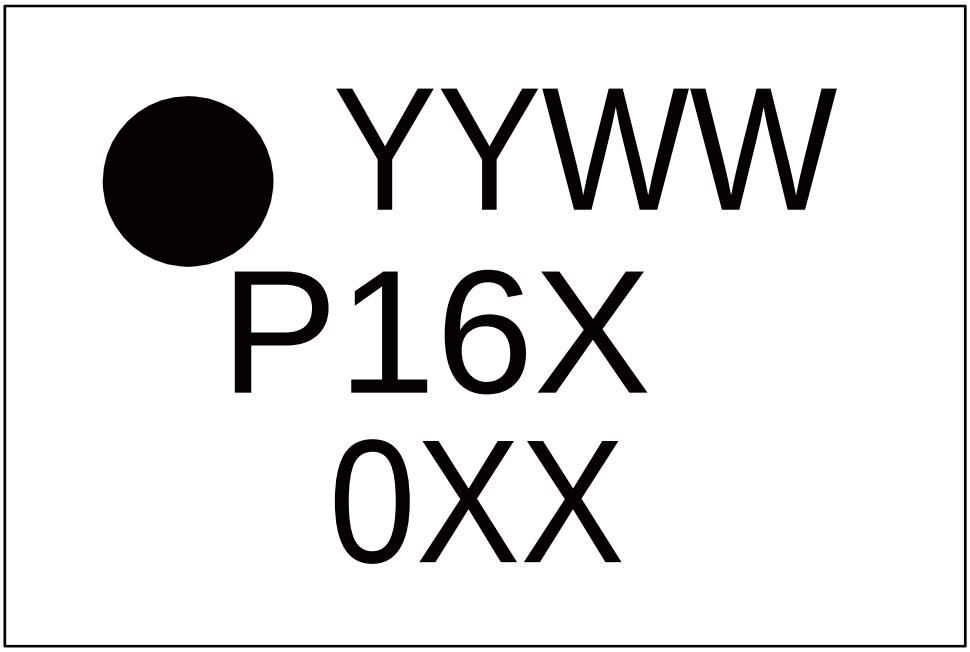
8-pin plastic SON
(LCC-8P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ MARKING

[MB85RDP16LXPN-G-AMEWE1]



[LCC-8P-M04]

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
26	■ **ESD AND LATCH-UP**	Revised part number.
27	■ **CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES**	Deleted the URL info.
29	■ **PACKAGE DIMENSIONS**	Deleted the URL info.

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