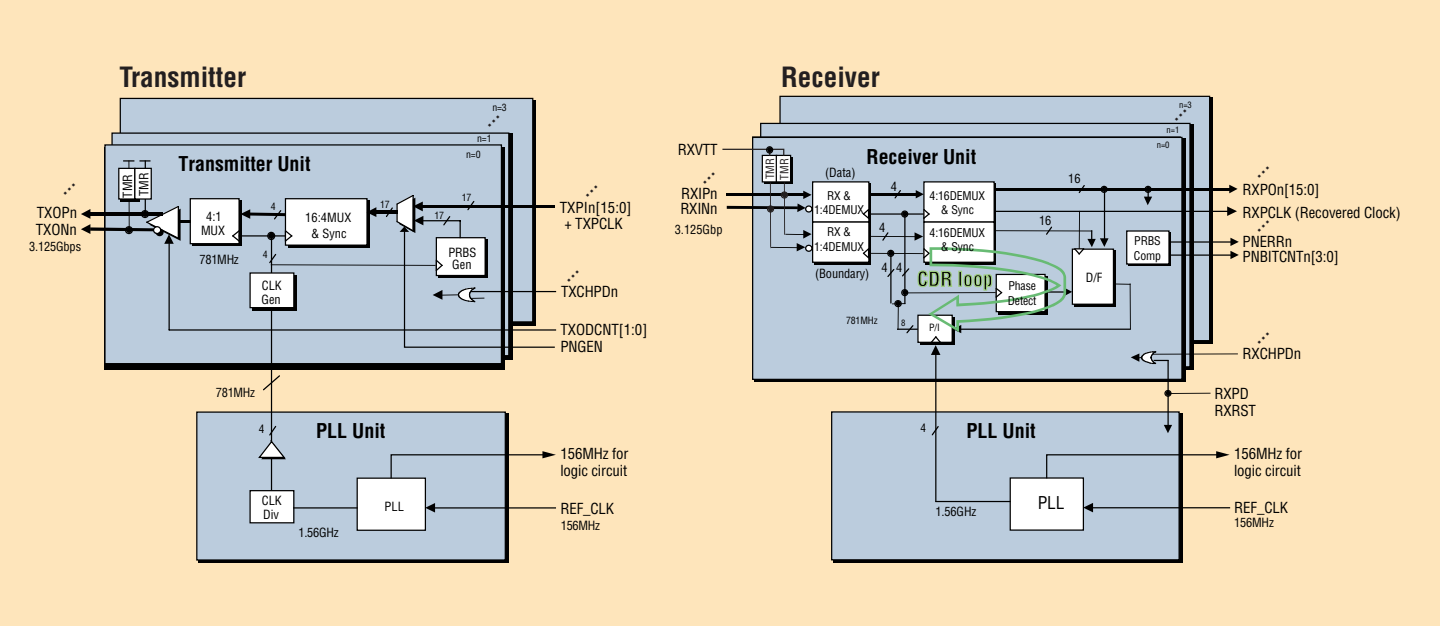
3.125Gbps x4 Parallel Transceiver

Macro for XAUI (0.18µm)



Features

- 3.125Gbps x 4 channel unidirectional data transfer rate for 10G Ethernet physical layer
- IEE802.3ae physical layer compliant
- 156MHz input reference clock and parallel interface
- 4-channel CDR Rx and 4-channel Tx arrays
- Differential PCML
- AC coupled differential interface
- 1:16 SERDES with 16:20 gearbox provided as RTL/netlist
- 8B/10B coding, lane alignment provided as RTL/netlist
- On chip integrated 50-ohm termination resistors
- Independent dual loop PLL and PI(phase interpolator) based CDR on each Rx channel
- Built-in PRBS (2^23-1) generators and comparators for loopback testing
- 1.8V and 3.3V power supply, 0.18µm standard CMOS process

Benefits

- Available as library cell for ASIC designs
- Programmable Tx voltage swing and amount of pre-emphasis
- Pre-emphasis based Tx equalization allows up to 12dB high frequency loss

3.125Gbps x4 Parallel Transceiver

Description

The Fujitsu's XAUI macro is for ASICs that perform at high bandwidth data communication.

The macro meets XAUI jitter specifications as follows:

- jitter generation < 0.35UI (without pre-emphasis)
- jitter tolerance > 0.60UI (peak to peak total jitter)
- meets sinusoidal jitter tolerance mask requirement

The macro has 180mW/ch power dissipation(including Rx, Tx, CDR, bias circuit and PLL, maximum pre-emphasis) and runs under power supply of 1.8V±0.15V, 3.3V±0.30V and junction temperature of -40°C~125°C.

The macro is fabricated in Fujitsu's standard 0.18µm CMOS technology.

The macro can be used in a variety of applications:

- 10G Ethernet
- WAN router or switch backplanes and line card to switch fabric interface
- Any backplane line for 3.125Gbps x4 data rate

Deliverables

The Fujitsu value-added XAUI Transceiver Macro enables our customers to design a variety of complex ASIC designs for high end networking applications.

A Fujitsu application engineer works with the customer to identify the customer's specific IP requirements. Fujitsu will provide the customer with following information to support the 3.125Gbps x4 XAUI Transceiver macro:

- Verilog Model
  - Front-end simulation
  - C model with Verilog wrapper
- Design Compiler Model
  - Timing analysis
- Library Exchange Format (LEF)
  - Floorplanning
  - Place and Route

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